Silicon MOS quantum dots for electron spin qubits

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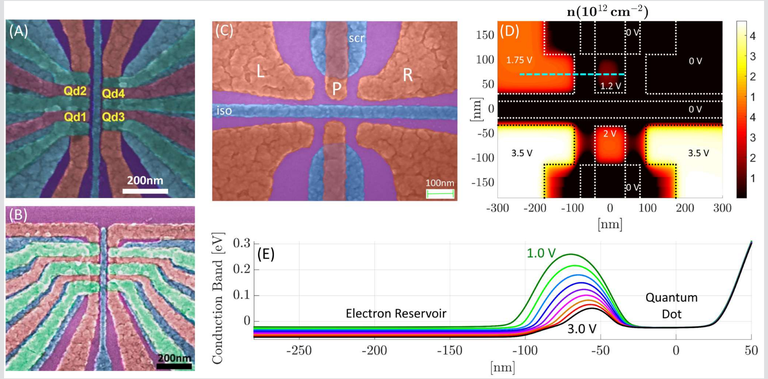
Introduction

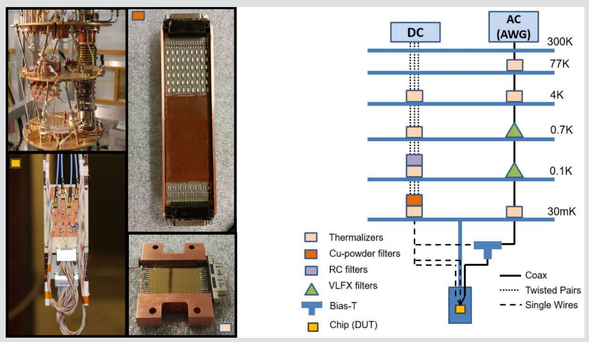
Single electron spins in quantum dots are promising candidates for solid-state, electrically-controlled qubits. Silicon can be isotopically purified to produce a 'magnetic vacuum' free of nuclear spin noise, yielding long electron spin coherence times. With a device structure (MOS) akin to silicon transistors, there is a pathway to scalability based on conventional chip fabrication methods. Here, we explore reducing the number of metal gate electrodes needed to form and control dots in order to improve the prospects for scalability [1].

Few-electrode device geometry



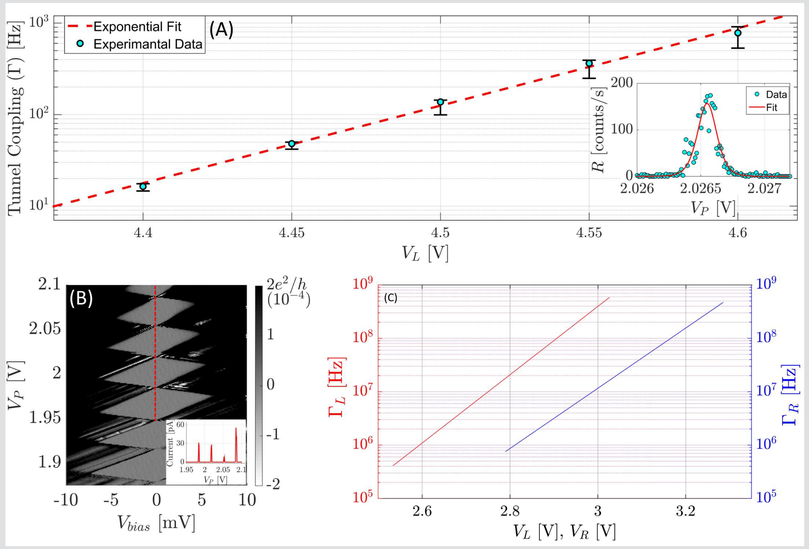
(A,B) False-colored SEM images of previous 3-metal-layer device geometries forming a pair of double quantum dots. **(C)** False-colored SEM image of a 2-metal-layer geometry forming a pair of single quantum dots defined by nanometer gaps. **(D)** Classical electron density simulated at low temperatures using a finite element Poisson solver (nextnano^{++}). **(E)** 1-D plots of the simulated conduction band below the SiO_2/Si interface along the dashed horizontal line in **(D)** for voltages V_L from 1V to 3V.

Experimental setup



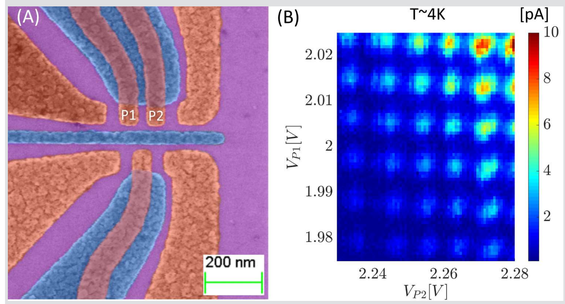
(Left) Dilution refrigerator, sample board, Cu-powder PCB filters, and DC thermalizers. **(Right)** Schematic diagram of the experimental setup outlining the various stages of filtering and thermalization for DC and AC lines.

Single quantum dots

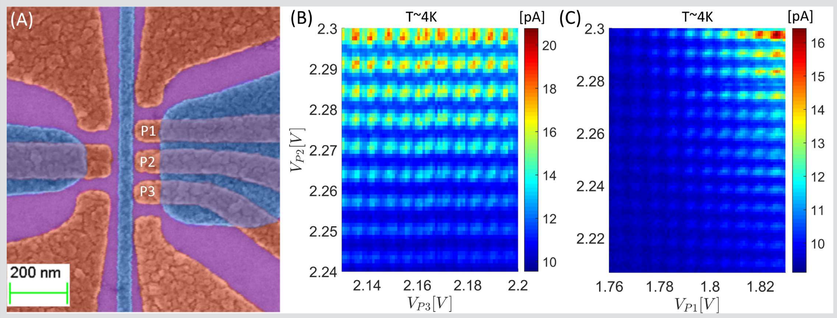


(A) Exponential relationship between tunnel rate Γ and V_L obtained via electron counting experiments at low tunnel rates. Inset shows electron counting data and the fit used to determine Γ. **(B)** Coulomb diamonds measured at T=35 mK. Inset: Coulomb peaks along the vertical red line. **(C)** Exponential relationship between Γ and V_L, V_R obtained via direct transport measurements at high tunnel rates.

Double and triple quantum dots

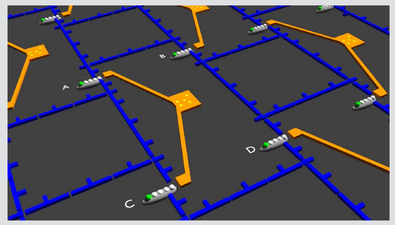


(A) False-colored SEM image of a 2-metal-layer double quantum dot device. **(B)** Charge stability diagram between V_{P1} and V_{P2} measured at T=4K.



(A) False-colored SEM image of a 2-metal-layer triple quantum dot geometry. **(B,[C])** Charge stability diagram between V_{P3} and V_{P2} [V_{P2} and V_{P1}] at 4K.

Network architecture

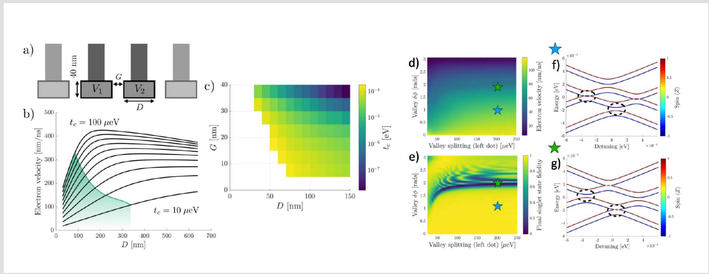


Network of nodes for a surface code quantum computer [2]. Four nodes (A-D) in a larger network, connected by electron shuttling 'highways' (blue electrodes). In each node,the data qubit is a green dot and ancilla qubits are white dots. Orange electrodes denote electron reservoirs.

We envision a network architecture in which few-qubit nodes are connected by distributing pairs of spin singlets via electron shuttling. Such an architecture maps naturally to a surface code [2], and creates useful space for wiring interconnects and realistic MOS scaling.

Coherent spin shuttling simulations

Electron shuttling in our few-electrode device geometry has been investigated numerically as a prelude to experimental tests. We have developed methods to optimize the device geometry for shuttling speed while maintaining adiabaticity, and to include spin-orbit and valley effects on the transport of coherent spin states.



(a) Top view of the gate geometry used in simulations; the lower rectangular parts are metal on thin oxide and induce quantum dot formation. **(b)** Shuttling velocity versus dot size for different values of tunnel coupling t_c. The green shaded region corresponds to a gap size G $\geq$ 10 nm, outside this region requires smaller gaps that would be challenging to fabricate. **(c)** Tunnel coupling versus dot size D and gap size G. **(d-g)** Calculations using an effective double-dot Hamiltonian that includes spin-orbit coupling, valley splitting, valley phase and Zeeman coupling. (e) shows the fidelity of a spin singlet after shuttling one member of the pair.

Acknowledgments and References

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1. E. Barrera et al, https://arxiv.org/abs/1812.09643
2. B. Buonacorsi et al, *Quantum Sci. Technol.* **4**, 025003 (2019)

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