Developing Superconducting Semiconductors for Topological Quantum Computing

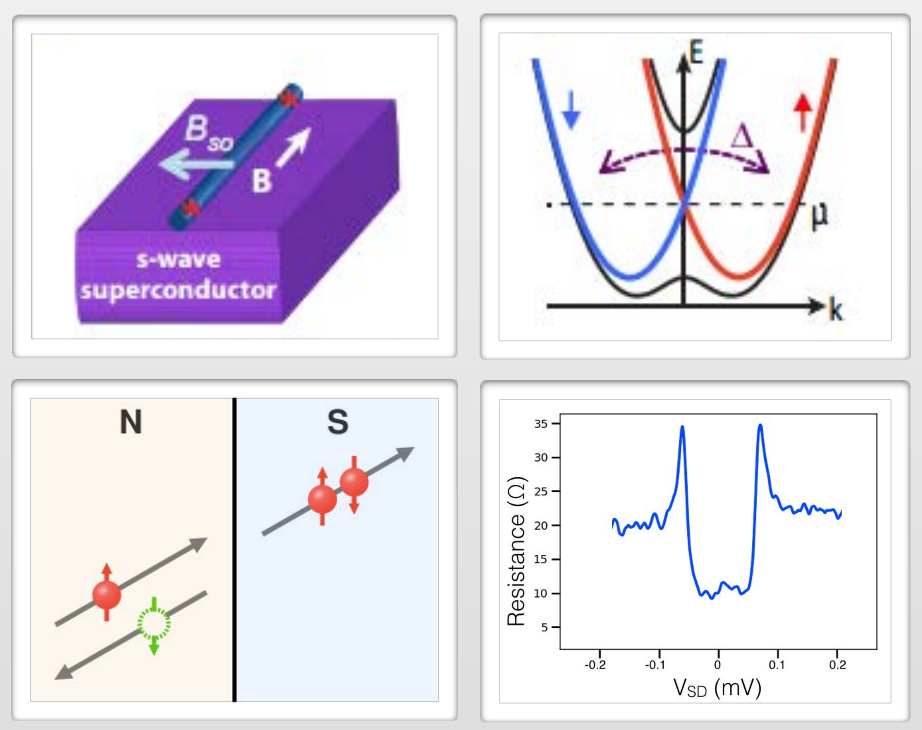
E. Annelise Bergeron, F. Sfigakis, K. Gharavi, Y. Shi, Z.R. Wasilewski, J. Baugh

UNIVERSITY OF WATERLOO

IQC Institute for Quantum Computing

Introduction

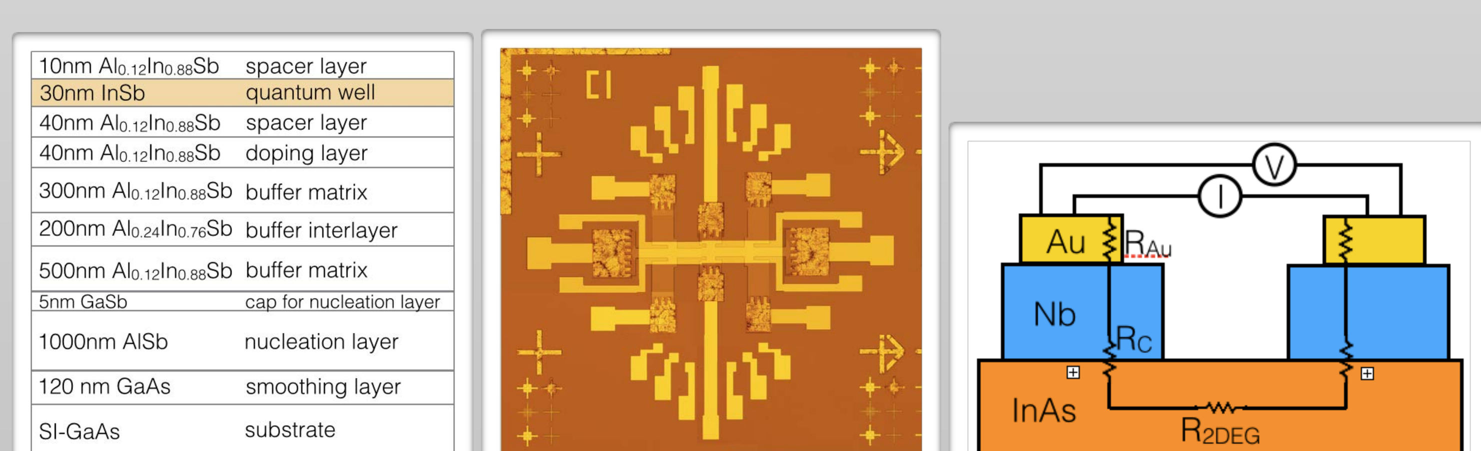
We aim to develop Majorana fermion (MF) devices in 2D electron gases (2DEGs) of InAs and InSb as a scalable approach to topological quantum computing.



(Top left) Conceptual MF device.[1] (Top right) Energy dispersion diagram for a 1D semiconducting wire with Rashba spin orbit interaction (SOI). Magnetic field induces a Zeeman gap at k=0 and superconductivity induces a gap Δ.[1]

(Bottom left) Schematic of Andreev reflection (AR) at an SN interface. (Bottom right) Measurement showing resistance reduced by half due to AR within the superconducting gap.

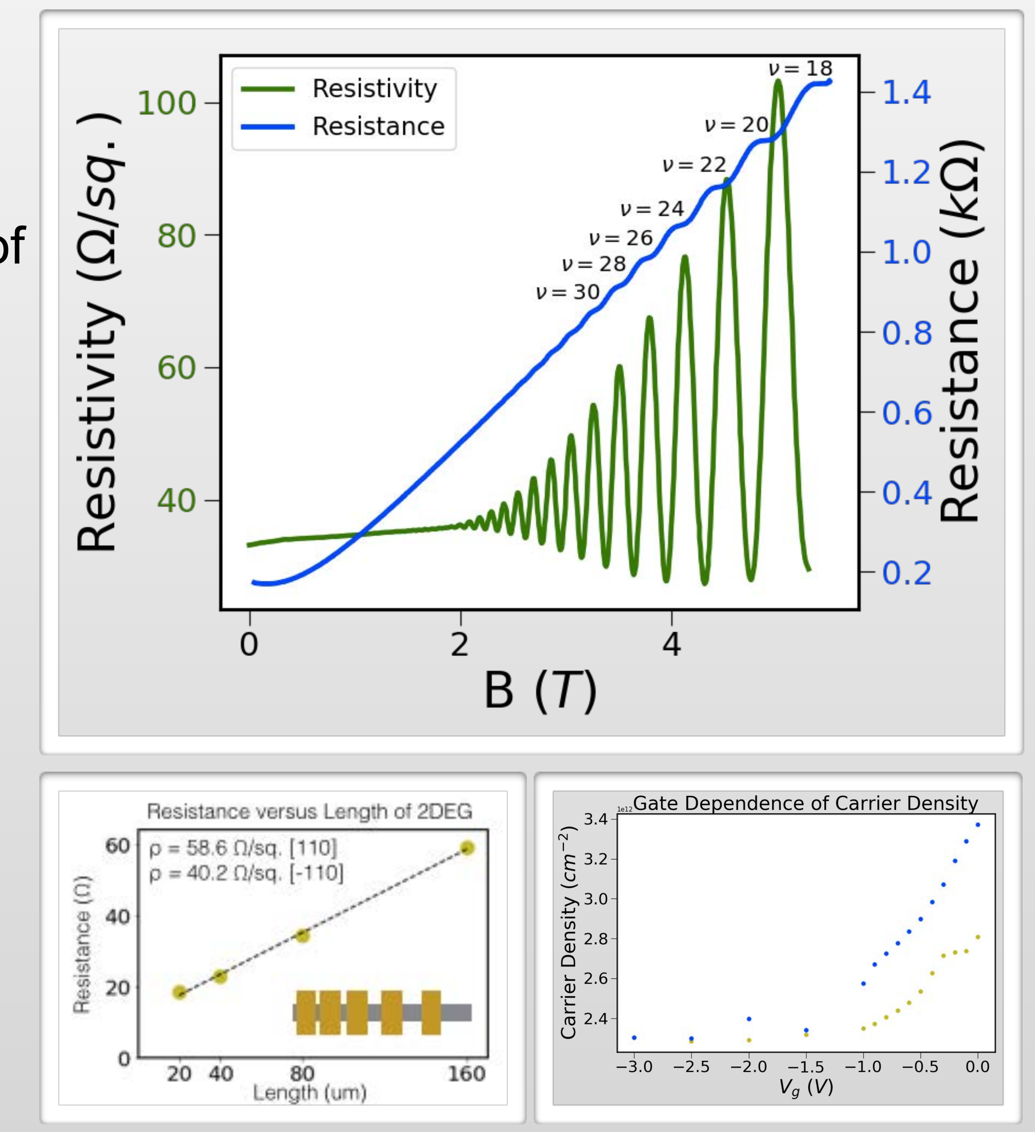
Device Fabrication



(Left) Layer diagram of an InSb quantum well grown on a GaAs substrate. (Center) Optical image of gated Hall bar device (Right) Schematic cross section of transmission line measurement (TLM) device detailing equivalent resistance circuit.

Experiments

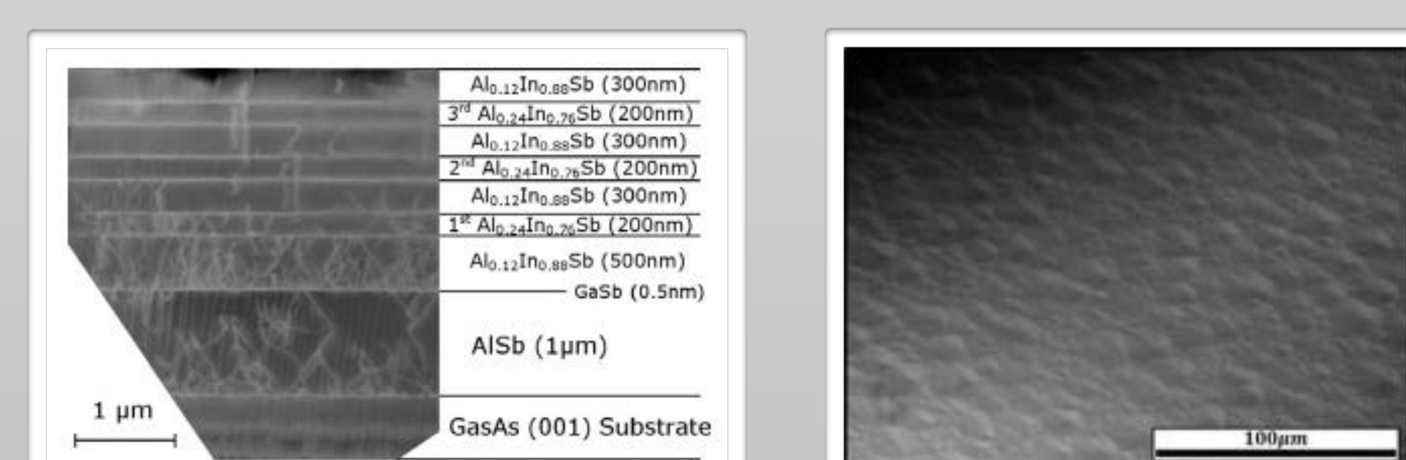
We have carried out characterization of a variety of 2DEG growth heterostructures in InAs and InSb.



(Top) Magnetoresistance measurements reveal Shubnikov de Haas oscillations characteristic of the quantum Hall effect. However, the minima do not reach zero resistance, indicating parallel conduction channels.

(Bottom left) Determination of 2DEG resistivity and ohmic contact resistance from a TLM. Small contact resistances are a result of an optimized surface passivation recipe.

(Bottom right) Measurement of carrier density as a function of gate voltage in a gated Hall bar. Carrier density is shown to plateau at a finite carrier density rather than reaching full depletion. This again suggests parallel conduction channels in the heterostructure.



Screw dislocations[2] (Left) and hillocks[3] (Right) are suspected to be the scattering centers responsible for low electron mobilities in InSb 2DEGs. We found that growth at an optimal offcut angle suppresses hillocks, and work is underway to assess the impact on mobility.

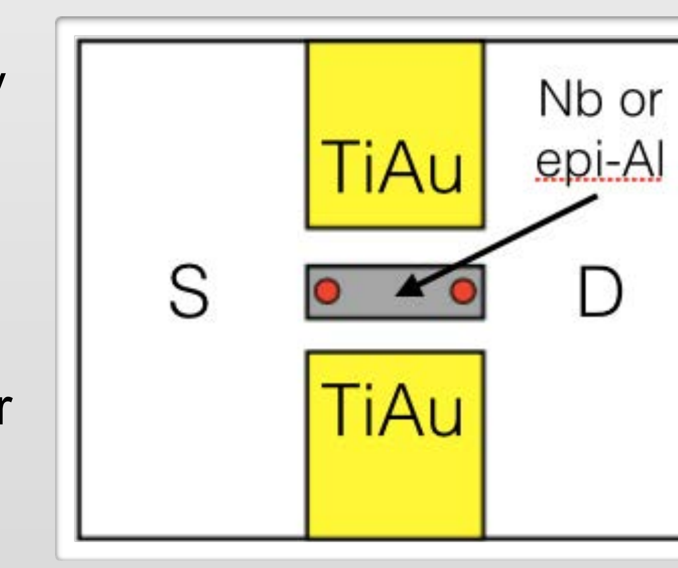
Summary and Outlook

In summary, we have optimized fabrication processes for developing superconducting semiconductors in 2DEGs by:

- Optimizing MBE growths for mobility, carrier density and surface roughness.
- Developing passivation processes for ideal interface resistances.
- Improving gate-ability of the quantum well.

The immediate goal is to achieve gate tunability of the 2DEG density to full depletion to create a Majorana island device (right) with an effective 1D channel

The long term goal is couple these Majorana pairs to quantum dots for readout of Majorana parity qubits.[4]



References

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4. K. Gharavi et al, Physical Review B 94, 155417 (2016).

Acknowledgements

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