Optimizing lateral quantum dot geometries for reduced exchange noise

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Motivation

Electrostatic control of the exchange interaction is the basis for two-qubit logic gates between spin qubits in lateral quantum dots.

- Experimentally, it remains a challenge to realize exchange gates with the fidelities required for fault-tolerant quantum computing, due to the sensitivity of exchange to charge noise.
- Given a theoretical model of a dot network, it is also challenging to *accurately* and *efficiently* calculate pairwise exchange energies computationally.

We address both challenges by developing a modified linear combination of harmonic orbitals configuration interaction (LCHO-CI) method that is more computationally efficient that previous methods [1]. With this new approach, we explore how the geometric parameters of a silicon MOSFET double quantum dot affect the sensitivity of exchange to charge fluctuations in the environment.

LCHO-CI method

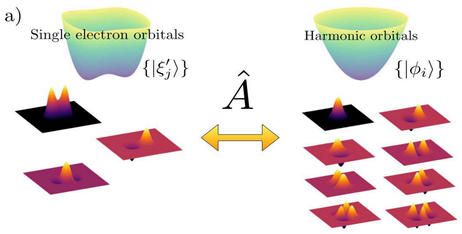


Figure 1: Using harmonic orbitals (HO) to approximate single-electron states. The operator A transforms between the HO basis and the approximate single-electron orbitals. (left) First three single-electron orbitals for a quartic potential, (right) eight lowest energy HO states.

We modify the LCHO-CI method introduced by Gimenez et al [2] by using the orbitals of a single harmonic well, located at the center of a dot network, to approximate single-electron orbital states.

$$H = \sum_i \epsilon_i c_i^\dagger c_i + \frac{1}{2}\sum_{ijkl} \langle ij|\, v\, |kl\rangle\, c_i^\dagger c_j^\dagger c_k c_l. \quad \text{(Eq. 1)}$$

Determining the Coulomb matrix elements (CMEs) in the two-electron interaction terms (Eq. 1) is the computational bottleneck in CI. With our choice of HO basis, the CMEs have an analytical expression, so that a pre-calculated library of integrals can be compiled, significantly improving efficiency.

MOSFET double dot

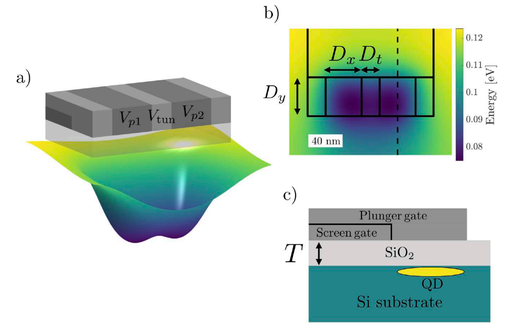
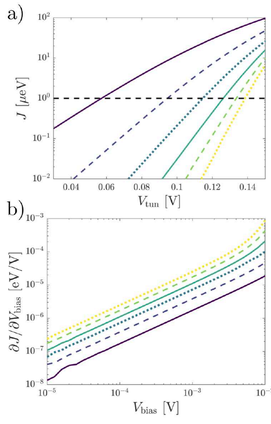


Figure 2: Silicon MOSFET double quantum dot device model and potential landscape determined by a Poisson solver. D_x , D_y denote the lateral dimensions of the plunger gates (D_t refers to tunnel gate width). T (panel c) represents the oxide (SiO_2) thickness.



Color	D_x [nm]	D_y [nm]	U [meV]	α [eV/V]
	30	30	23.15	0.1349
	40	40	21.29	0.1667
	50	50	19.52	0.1861
	60	60	18.06	0.1973
	70	70	16.86	0.2018
	80	80	15.85	0.2022

Figure 3: (a) Exchange strength J for a two-electron double quantum dot versus the tunnel gate voltage, for different plunger gate dimensions. (b,c) Sensitivity of exchange to bias ($V_{p1} - V_{p2}$) and detuning (ϵ) fluctuations.

Results

Figure 3b shows that the sensitivity of exchange to fluctuations in bias voltage ($V_{bias} = V_{p1} - V_{p2}$) increases with the dot size. This is expected, as a larger charging energy (smaller dot) should suppress the noise sensitivity. By calculating the gate lever arms, we obtain the sensitivity to fluctuations in detuning (Fig. 3c). We also varied tunnel gate width, oxide thickness, and dot eccentricity. Generally, we find that small and symmetric plunger gates, narrow tunnel gates, and suitably thick SiO_2 will improve the robustness to charge noise. We envision the modified LCHO-CI method enabling the realistic modeling of two-qubit logic gates in quantum dot networks, such as multi-qubit processor nodes.

References

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2. I. P. Gimenez, M. Korkusinski, P. Hawrylak, Phys. Rev. B **76**, 075336 (2007).

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