Sn Bumping Without Photoresist Mould and Si Dice Stacking for 3-D Packaging

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***Abstract*—Chip stacking with through-silicon-vias (TSV) technology for 3-D packaging of electronic devices was investigated. A new process of direct solder bumping on Si wafers without photoresist (PR) mould was designed and applied in this study. The Cu extrusion process on the via was also omitted for process simplification. This simplified process can be useful for cost reduction and increased productivity. The substrate for the experiments was a p-type $\langle 100 \rangle$ Si wafer of 100 mm diameter. In order to produce the vias, the Si wafer was etched by a deep reactive ion etcher (DRIE) using SF_6 and C_4F_8 plasmas alternately. The produced vias were 40 μm in diameter and 80 μm in depth. On the via side walls, SiO_2, Ti, and Au layers were formed with thicknesses of 1, 0.1, and 0.7μm, respectively. Pulsed direct current (DC) electroplating was used to fill the vias with Cu. Then the Si wafer was back ground to a thickness of 80 μm until the Cu filling in the vias was exposed to the surface without extrusion. Plating current subsequently flowed through the vias to the bumping surface, and Sn was electroplated on the Cu filling directly without a PR mould. To optimize the bumping process, the current density and time for Sn plating were varied from 0.04 to 0.06 A/cm^2 and from 10 to 40 min, respectively. Bumps with a height of 20 μm were formed successfully with 0.05 A/cm^2 and 30 min without a PR mould. The bump height increased with increasing plating current and time; for example, from 13 μm at 10 min to 33 μm at 40 min in case of 0.06 A/cm^2. The Si dice with electroplated Sn bumps had dimensions of 5 $\times$ 5 mm and thickness of 80 μm. Three Si dice were stacked successfully by micro-soldering at 260 °C. In the interface between the Sn bumps and the Cu filling, a Cu_6Sn_5 intermetallic compound was produced with a thickness of 3.2 μm. Through this study, a process for non-PR solder bumping by electroplating and wafer stacking with TSV was achieved successfully.**

***Index Terms*—Non-PR bumping, packaging, Si chip stacking, through silicon via, tin.**

I. Introduction

RECENTLY, the trend to smaller and lighter electronics has accentuated efforts towards high density, increased performance and miniaturization in packaging technology. For example, in multichip module (MCM) and in system-in-package (SiP), much higher packaging density is required. Stacking of Si dice (3-D packaging) technology has been studied in order to meet these requirements [1]–[3].

The 3-D packaging of Si dice requires several successive processes like via drilling, conductive metal filling in the vias, bumping over the vias and wafer stacking. For via drilling, DRIE [4], [5] and laser drilling [6], [7] are popular processes, and Cu is usually filled in the vias by electroplating to function as an electrode [4], [8]. For metal bumping, Au, Cu, Sn, or Sn alloy are popularly used [2], [3], [9]–[12]. Sn and solder bumps are cost-effective, and they require no pressure for bonding during reflow soldering which avoids damage to the fragile thin wafers.

Generally, Sn or solder bumps can be applied by electroplating [13], [14], ball mounting [15], paste printing [16], or injection molding solder of C4NP (Controlled Collapse Chip Connection New Process) [17] for bumps between stacked chips or bumps of an outer chip. The electroplating process is appropriate to make a tiny bump such as 10 μm or less which is compatible with the fine via diameters of 1–10 μm for 3-D Si dice stacking [18]. The electroplating process also enables approaching mass production and uniform size of bumps. However, its disadvantages can be relatively long bumping time and variations in alloy composition according to the positions of a wafer in the plating bath. Very careful control of current density and plating parameters is required to get suitable bumps.

In general, the electroplated bumps are produced using a photoresist (PR) mould established by lithography technology [13], [19]. Previous published work about non-PR methods of electroplating of bumps is hard to find. The lithography technology consists of several process steps such as PR coating, film masking, UV lightening, patterning, PR stripping, and so forth. This lithography technology takes processing time and adds cost, so a method of bumping without PR mould would be highly desirable. In this study, the feasibility of solder bumping by electroplating without PR mould and Si dice stacking were investigated. These technologies will be helpful to reduce cost and enhance productivity by omitting lithography related processes. Additionally, a process to establish a Cu extrusion on the via [2], [3], [11], [12] was omitted in order to avoid complicated preferential etching of Si to Cu during back grinding of Si.

II. Experimental

For an experimental substrate, a $\langle 100 \rangle$ silicon wafer of p-type was used. The diameter of the wafer was 100 mm, and original thickness before wafer thinning was 500 μm. In order to produce via holes on the wafer surface, the Si wafer was etched by

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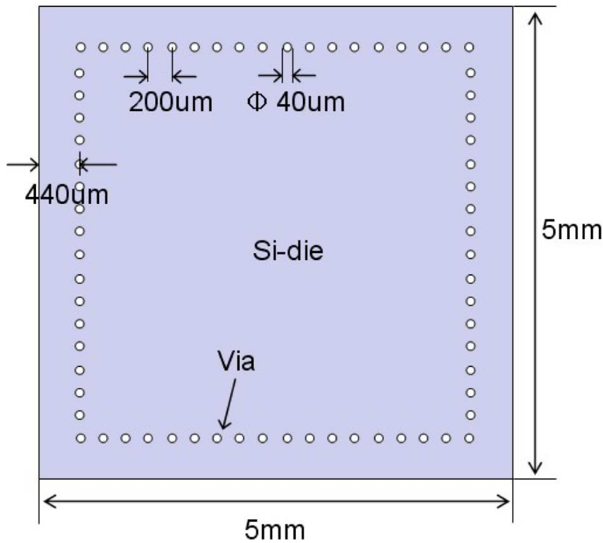

Fig. 1. Dimensions of Si die for experiments.

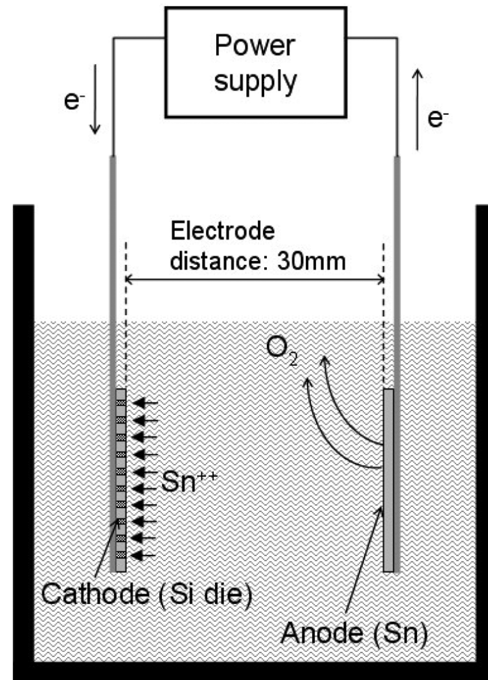

Fig. 2. Arrangement of electroplating equipment.

a deep reactive ion etcher (DRIE) using SF_6 plasma for etching and C_4F_8 plasma for passivation, alternately. The wafer was divided into 284 quadratic dice with 5 mm side length. A total of 68 via holes were produced peripherally in each die. The vias with a diameter of 40 μm and depth of 80 μm were prepared, and the pitch between the vias was 200 μm (see Fig. 1).

On the via walls, dielectric, adhesion, and seed layers of SiO_2, Ti, and Au, respectively, were formed sequentially. The SiO_2 layer was produced by a thermal oxidation method at 1000 $^\circ C$ with 1 μm resulting thickness. Such a high temperature is acceptable if the via is formed before the integrated circuit (via-first process). The Ti and Au layers were deposited by Ar sputtering using 1000 W power of a radio-frequency (RF) sputtering source. Thicknesses of the Ti and Au layers were about 0.1 and 0.7 μm, respectively.

Cu was filled into the vias by electroplating. The electroplating solution for Cu filling was composed of $CuSO_4 \cdot 5H_2O$, H_2SO_4, Cl^- and other additives. For Cu electroplating, direct current (dc) with forward and reverse pulsing method was used. The cathode and anode were Si wafer with vias and a pure Cu ball, respectively.

The back side of the electroplated wafer was polished mechanically and chemically until Cu filling was exposed to the surface without extrusion. The thickness of the back ground wafer became 80 μm, and the wafer was then cut into 5×5 mm dice. Each Si die was attached to the cathode, and Sn was electroplated to make bumps on the exposed Cu fillings without a PR mould. The anode was a Sn plate with dimension of $15 \times 15 \times 0.5$ mm. DC was used for electro-deposition, and the distance between cathode and anode was 30 mm (Fig. 2).

DC was supplied through the seed layer of Au, and the current density was varied among 0.04, 0.05, and 0.06 A/cm^2. The solution for Sn plating was a commercial product (Slotoloy-SN30) and was agitated by a magnetic stirrer with a rotation speed of 240 rpm. Electroplating was performed at 25 $^\circ C$ bath temperature to avoid loss of volatile substances and the oxidation of stannous tin.

The Si dice with Sn bumps were aligned for stacking and reflowed at 260 $^\circ C$ for 20 s in air with rosin mildly activated (RMA) flux. The Cu-filled vias, stacked dice and microstructure of the soldered joint were observed by field emission scanning electron microscopy (FE-SEM). The composition of the intermetallic compound (IMC) along the Sn/Cu interface was analyzed by energy dispersive X-ray analysis (EDS).

III. Results and Discussion

On the exposed Cu filling surfaces, Sn was electroplated as a bump without PR mould. Stable current flow during Sn plating is important to get suitable bumps in a non-PR mould process. Fig. 3 shows the time history of current flows during electroplating with increasing time at different current densities. The current values were kept constant with electroplating time at each current density. Specifically, the current values were 34.2, 42.3, and 50.8 μA for 0.04, 0.05, and 0.06 A/cm^2, respectively. Thus, this stable current was expected to contribute to forming uniform shaped bumps in the Sn plating process.

The principle of Sn bumping over Cu filling without PR mould is suggested in Fig. 4. Current is allowed to flow through a metal layer (Au seed layer) on the Si surface and the Cu filling. This plating current enables formation of Sn bumps on the top of each Cu filling.

Fig. 5(a) shows appearance of the electroplated Sn bumps on Cu filling without PR mould, where the plating condition was dc 0.05 A/cm^2 for 30 min. The size of the Sn bumps was measured as about 22 μm in height and 68 μm in diameter. The bump shape was similar to a mushroom except having no columnar part.

The bumps produced were almost round but did not have as smooth peripheries as the electroplated bumps formed with PR

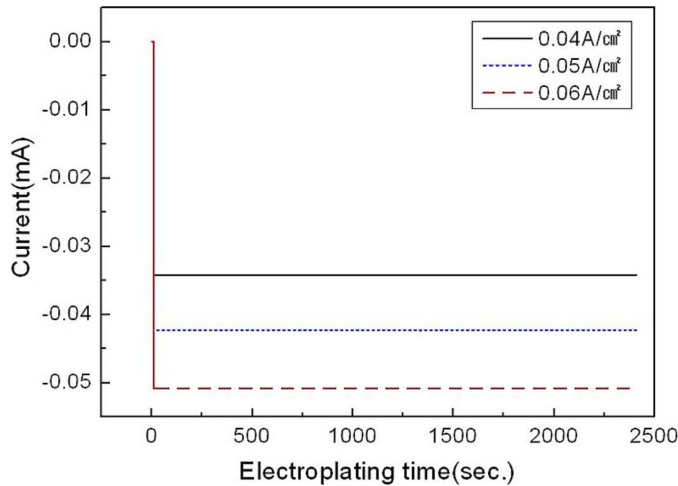

Fig. 3. Relationship between current flows and time during Sn electroplating with different current densities.

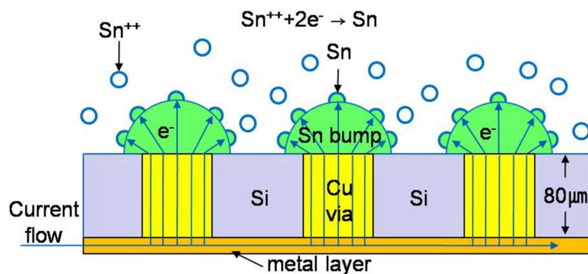

Fig. 4. Principle of electroplating of Sn bumps on Cu filling without a PR mould.

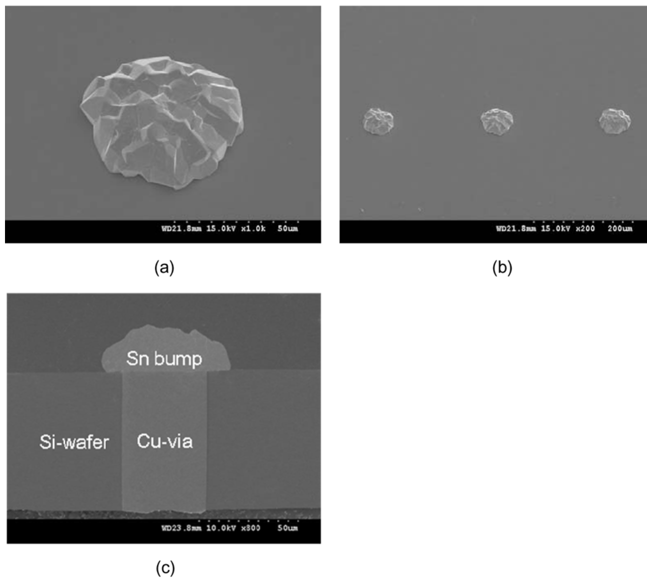

Fig. 5. Sn bumps formed on the Cu filling by dc electroplating without PR mould, (a) bump appearance, (b) bumps having good uniformity, and (c) cross section of a bump (Sn plating condition; 0.05 $\mathrm{A/cm^2}$, 30 min).

mould [13], [14]. From the periphery shape, it seems that the current flow through the Cu filling as well as Sn^{++} ion concentration in the bath around the bump were almost uniform in all directions of the bump. However, in order to further reduce

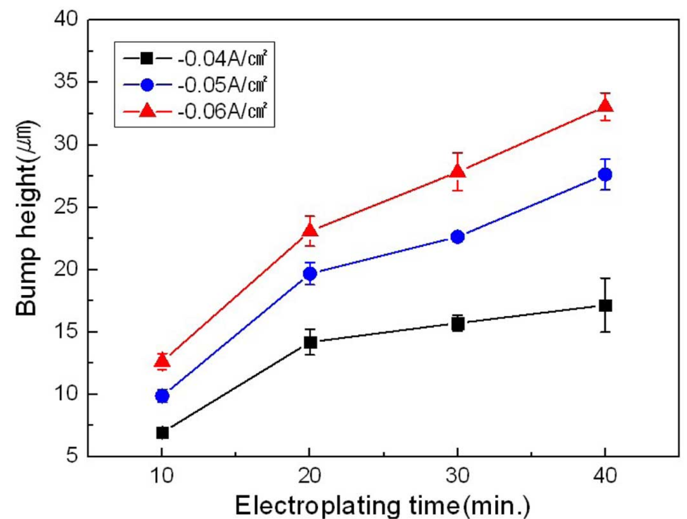

Fig. 6. Relationship between Sn bump heights and electroplating time with different current densities.

the roughness of the electroplated surface, addition of a surface active agent to the electroplating solution should be helpful. Careful control of electroplating parameters such as pulse current and current density are also required [20].

The neighboring bumps showed good uniformity in shapes and sizes as shown in Fig. 5(b). In the cross section of Fig. 5(c), the Sn bump was bonded well on the Cu filling. Serious defects were not observed along the Sn/Cu interface. From these results, the feasibility of Sn bumping without PR mould has been confirmed.

Fig. 6 shows a relationship between Sn bump heights and electroplating time with different current densities. The height increased with increasing electroplating time, but the rate of height growth decreased with time. Specifically, in the case of 0.05 $\mathrm{A/cm^2}$, the bump height increased from 9.9 to 19.7, 22.6, and 27.6 $\mu\mathrm{m}$ with increasing times of 10, 20, 30, and 40 min, respectively. The deposition efficiency during electroplating can be decreased by reduction of Sn concentration in solution with time, hydrogen discharge in acidic media and decomposition of some organic additives [21].

With increasing current density, the bump height also increased as in Fig. 6. Specifically, with a constant time of 30 min, the bump height increased from 15.7 to 23.0 and 27.8 $\mu\mathrm{m}$ by increasing current density from 0.04 to 0.05 and 0.06 $\mathrm{A/cm^2}$, respectively. The uniformity of the Sn bump height without PR mould needs to be high enough for practical applications. For the condition of $40\,\mathrm{min}$ -0.06 $\mathrm{A/cm^2}$, the measured bump heights from Fig. 6 were 35.0, 33.0, 32.6, 32.4, and 32.4 $\mu\mathrm{m}$. More detailed evaluation based on a larger sample size is required in a further study to fully quantify the uniformity of the bumps.

Fig. 7 shows Sn bump widths with electroplating time. The bump width increased with plating time as well as current density, although some data scattering existed. In the case of 0.06 $\mathrm{A/cm^2}$, the width increased from 52.6 to 81.8 $\mu\mathrm{m}$ with increasing time from 10 to 40 min. At 30 min of plating time, the width increased from 54.8 to 75.6 $\mu\mathrm{m}$ by increasing current density from 0.04 to 0.06 $\mathrm{A/cm^2}$. Since PR mould was not present,

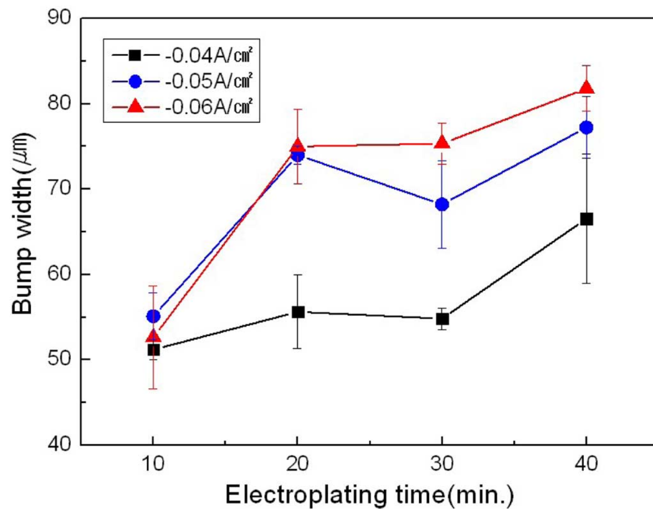

Fig. 7. Relationship between Sn bump widths and electroplating time with different current densities.

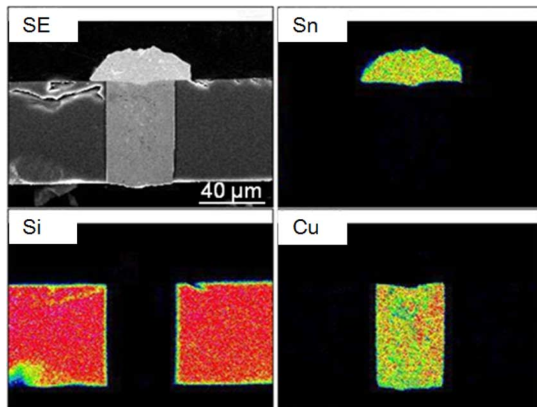

Fig. 8. Analysis of Sn and Cu for the Sn bump and Cu via by EDS.

some of the bumps had wider width and deviated from the tendency of normal width increase. Getting proper bump width is important in this non-PR mould process to avoid unwanted connections between neighboring bumps. Unsuitable connections between neighboring bumps were not observed in this study.

Sn and Cu analysis for the Sn bumps and Cu vias were performed by EDS, as shown in Fig. 8. Sn was plated well over the Cu filling. Sn and Cu inter-diffusion across their mutual interface seemed not serious to create significant Cu-Sn IMC. However, according to more detailed analysis using transmission electron microscopy (TEM), Cu_6Sn_5 formation between Sn film and Cu via has previously been reported even in the as-Sn-plated state [11].

IMC between Sn bumps and Cu filling that can be produced during the reflow process of Si dice was examined. The Sn bump electroplated at 0.05 A/cm^2 for 30 s on Cu filling was heated on the hot plate at 260 °C for 20 s. The reflowed bump showed a hemispherical shape with max width of 53 μm and height of 33 μm (see Fig. 9). Along the Sn/Cu bonding interface, scallop shaped IMC was clearly observed Fig. 9(b). The composition of the IMC was analyzed as 52.7 at.% (37.4 wt.%) Cu and 47.3 at.% (62.6 wt.%) Sn by EDS. This is the typical

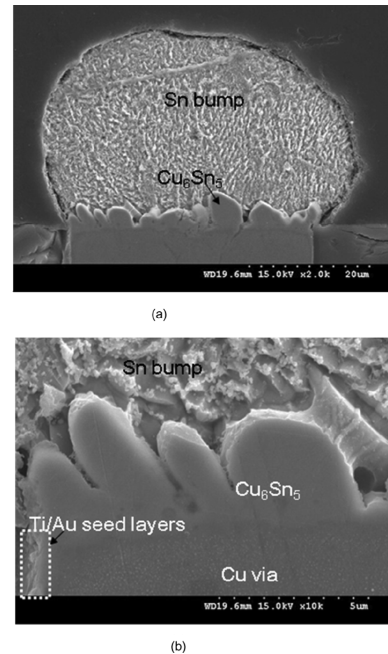

Fig. 9. Cross section of Sn bump after reflow (a), and interfacial IMC (b).

IMC of Cu_6Sn_5 with scallop shape produced between Cu and Sn for most Sn-based solders [22], Sn-film/Cu vias [2], and Sn-2.5%Ag/Cu vias for 3-D packaging [12].

The thickness of the Cu_6Sn_5 was measured as 3.2 μm. This is a little thicker than common in general reflow soldering such as 2 μm produced between Cu and molten Sn at 240 °C for 600 s [23]. In a previous case of reflow soldering of Si dice stacking with 1.5-μm-thick Sn-2.5%Ag layer at 240 °C, all the solder layer changed to Cu_6Sn_5 and Cu_3Sn IMCs [12]. The IMC is a governing factor affecting bondability of the chip stacking joints [12]. Ultrasonic bonding, popular for 3-D packaging but using relatively lower bonding temperature, also produced the Cu_6Sn_5 IMC by the bonding of 0.5-μm-thick Sn to Cu vias at 195 °C [2]. However, since ultrasonic bonding is performed at lower temperature than reflow soldering, the thickness of IMC by ultrasonic becomes thinner [24]. Overgrown IMC can cause a reduction of joint strength [25], [26] and can be a crack path [27]. Thus, from the viewpoint of the IMC thickness, the bonding temperature of 260 °C as used in Fig. 9 is suggested to be excessive.

Three Si dice each of 80 μm thickness were stacked and reflow soldered at 260 °C for 20 s. Fig. 10 shows the cross section of the joined Si dice filled with mounting epoxy between the Si dice. The average gap between the dice was 30 μm, and average bump width at the maximum point was 60 μm. In this study there was no Cu extrusion from the via, while in previous reports, the extrusion has been prepared at 5 μm [12] or 7.5 μm [11] thickness. The preparation of Cu extrusion by preferential etching of Si is relatively complicated. For example, it requires an etchant of mixture of HF and HNO_3, and a precise etching time control [3]. Instead, in this study, a little thicker Sn bump was prepared which resulted in wider gap of 30 μm. This gap is wider than some previously employed such as 10–15 μm [11],

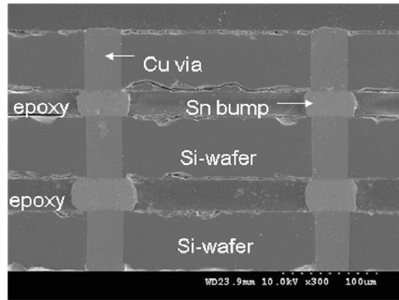

Fig. 10. Cross section of Si-dice stacking by reflow soldering.

[12], but smaller than about 50 μm [3]. Wide gaps can be reduced by fabricating smaller height of Sn bumps by process optimization.

Die-to-die processes have been demonstrated, e.g., Si dice were stacked by ultrasonic bonding or thermo-compression [22], [28]. During those bonding processes, relatively high pressure is required such as 24.5 N at 350 °C for thermo-compression, and 20 N at 150 °C for ultrasonic. This pressure can damage the very thin Si die. In Fig. 10, reflow soldering was applied without bonding pressure and the dice were stacked well. The feasibility of wafer stacking using Sn bumps without PR mould was also confirmed. While the focus of this study is on basic feasibility, further studies on various via diameters, pitches, the uniformity of bump size, and die-to-die or wafer level mass production are required to optimize this non-PR bumping technology.

IV. Conclusion

Si dice with through-silicon-vias were stacked by reflow soldering. In order to reduce the number of steps in the production process for 3-D packaging, the feasibility of Sn bumping on Cu vias without PR mould was investigated. The results are summarized as follows.

1) Sn bumps were successfully produced without a PR mould over the Cu fillings of a Si die by electroplating. Contrary to the mushroom morphology on a smooth column observed at the Sn bump with PR, the non-PR Sn bump exhibited only a head part with mushroom morphology without the columnar part.
2) The heights and widths of Sn bumps increased with electroplating time and current density. Expected Sn bump with height and width of 22.6 μm and 68.2 μm, respectively, was formed by 0.05 A/cm^2 of current density and 30 min of plating time. Serious defects were not observed in the bumps.
3) Three Si dice were stacked by reflow soldering at 260 °C on Cu filling using non-PR Sn bumps. The average gap between the Si die was 30 μm, and average width of bumps was 60 μm. Similarly to dice stacking with PR-mould bumping, the dice stacking without PR mould bump in this study exhibited no connection failure in the soldered joints.
4) Scallop shaped IMC of Cu_6Sn_5 with thickness 3.2 μm was produced along the Sn bump/Cu filling interface after reflow at 260 °C for 20 s.

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