Microelectronic Engineering 93 (2012) 85–90

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Characteristics of electroplated Sn bumps fabricated without a PR mould on a Si chip for 3D packaging

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A R T I C L E I N F O

Article history:
Received 23 March 2010
Received in revised form 30 August 2011
Accepted 31 October 2011
Available online 1 December 2011

Keywords:
Sn bump
Electroplating
Non-photoresist mould
3D packaging
Through-silicon via (TSV)

A B S T R A C T

The characteristics of electroplated Sn bumps, fabricated without a PR (photoresist) mould on copper-plugged TSVs (through-silicon vias), in a Si chip were investigated. A new process of non-PR bumping developed in this research was considered to enhance the productivity and reduce the cost for three-dimensional (3D) chip stacking. To produce Sn bumps, Pt was adopted as an anode, and thinned Si die with Cu-plugged TSVs as a cathode. The polarization curve of the Sn electrolyte was analysed to determine the reduction potential of the Sn ion. The heights, widths, and uniformities of the Sn bumps produced through the proposed non-PR process were evaluated to assess the feasibility of reliable Sn bumping using this process. The experimental results showed that the Sn electrolyte had a reduction potential of −0.463 V. The Sn bumps with rivet-head shapes were produced successfully without a PR mould on Cu-plugged TSV. The Sn bumps grew in both vertical (thickness) and lateral (width) directions due to the absence of a PR mould. The plating time was varied from 2 to 60 min at a constant current density of −30 mA/cm^2, and the bump height and width became 39 and 76 μm at 60 min, respectively. The morphologies of the Sn bumps without a PR mould showed the preferred facet growth by increasing the plating time, which resulted in increase of Sn facet size but decrease of number of facets. The uniformity of the bump widths on a chip was within the range of 86.9–95.4%.

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1. Introduction

In modern electronics, miniaturisation and high levels of integration are important issues. Three-dimensional (3D) packaging based on chip stacking is a promising solution to these issues [1]. In chip stacking, Au wire has been widely used for the electrical connections between the chips [2]. It has some drawbacks, however, such as the need for a larger bonding area and a long connection length to achieve a higher level of integration in chip packaging [3].

TSV (through-silicon via) technology is regarded as a strong candidate to substitute for wire bonding in the vertical connection of stacked chips. A Cu-plugged TSV imbedded in a Si chip can minimize the total length of the electric path, and as a result, faster response and less energy consumption of the electronic device can be achieved. An electrical connection between Cu-plugged TSVs can be made through bonding using Sn or solder bumps fabricated on the top surface of the Cu plugs. Generally, those bumps have been formed by electroplating or an evaporation method [4–12].

The electroplating method of making bumps has various advantages, such as suitability for mass production, easier control of the bump size, and lower production cost. Many studies on the electroplating of bumps have been carried out [5–15], and Sn or Sn-based alloys have been used as bumping materials [7,8]. Sn provides a uniform composition throughout the bumps as well as an easier plating condition compared to Sn-based alloys like Sn–Ag, Sn–Cu, and Sn–Ag–Cu [6,9,13].

The bump bonding process of vertically stacked chips is comprised of the fabrication of solder bumps, and the formation of bonds between bumps and TSVs. In the bump fabrication step, uniform bump heights and widths are desirable to ensure complete joints of whole bumps and TSVs. If bump height is non-uniform, for example, a smaller bump, surrounded by higher bumps, might not have enough contact to the TSV of the upper chip, and result in poor or even no connection. In the bonding formation step, metallic bonding between bumps and TSVs will be made by a soldering process such as reflow soldering or ultrasonic bonding.

Concerning the bump fabrication step, the bump size including the height and width, and its uniformity should be carefully considered for successful bump joints. For the SnAg [16] and PbSn [17] bumps electroplated with PR moulds, the uniformity of the bump size was investigated by Kim and Ritzdorf Bump uniformity for electroplated Sn bumps without a PR mould, however, was not reported.

For electroplating bumps on a Si wafer, photoresist (PR) has been used for patterning [5–12]. The patterned PR mould helps

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doi:10.1016/j.mee.2011.10.020

control the bump size and promotes a uniform morphology of bumps. A lithography process for the PR mould and the related process steps, however, such as the pattern mask, PR coating, UV (ultraviolet) exposure, PR development, and strip, increase the cost and production time even if they are useful in ensuring a better quality of bumps. The complicated process and high cost of lithography are deterring the implementation of the TSV technology to 3D packaging.

To address the shortcomings of the PR mould process in 3D packaging, a new electroplate-Sn-bumping process without PR patterning, which omits the lithography process, was investigated in this study. Sn bumps were directly electroplated on the Cu-plugged vias using a Pt anode, and the electroplating characteristics as well as the bump size and its uniformity were investigated to determine the feasibility of reliable bumping without a PR mould.

2. Experimental work

2.1. Test materials

To produce the Cu-plugged Si wafers, a CMOS (complementary metal-oxide-semiconductor) process was performed in the following sequence: (1) PR coating on a p-type ⟨100⟩ Si wafer (thickness: 520 μm; diameter: 100 mm) and UV (ultraviolet) exposure; (2) PR development; (3) via opening (40 μm in diameter; 70 μm in depth) through DRIE (deep reactive ion etching) and PR removal; (4) deposition of the insulation layer (SiO_2, 1 μm in thickness by chemical vapour deposition), adhesion layer (Ti, 300 nm by sputtering), and seed layer (Au, 500 nm by sputtering) inside the via and on the top surface of the wafer; and (5) Cu plugging into the via by pulsed current electroplating for 15 h.

Then the Cu-plugged wafer was thinned through CMP (chemical and mechanical polishing) to 70 μm and was cut into 264 chips with a diamond saw. Each Si chip had 192 Cu-plugged vias with 200 μm in pitch, and the total exposed area of the Cu plugs was 2.41×10^{-3} cm^2. After CMP and sawing process, a 150 nm-thick Au layer was sputtered on one side of the Si chips to facilitate the electrical contact between Cu-plugged vias and cathode plate. To produce Sn bumps on the Cu plugs, the 5×5 mm^2 Cu-plugged Si chip was selected as a cathode, and 10×10 mm^2 Pt as an anode. As a pretreatment for electroplating, the cathode was immersed in a 5% H_2SO_4 solution for 10 s and rinsed with distilled water. An electrolyte for Sn electroplating (hereafter, "Sn electrolyte") was fabricated, consisting of $SnSO_4$ (42.8 g/L concentration) and H_2SO_4 (106.8 mL/L), with a minor additive.

2.2. Electroplating and analysis

A polarization experiment was conducted on the Sn electrolyte using a commercial electrochemical-pulse plating unit (EPP-4000 by Princeton Applied Research Co.). The reference electrode was SCE (standard calomel electrode). The scanning range of the potentials was changed from 0 to −0.55 V against the SCE, with a scan rate of −2 mV/s. Fig. 1 shows the schematic diagram of the electroplating unit.

For the electroplating of the Sn bumps on the Cu plugs without a PR mould, the −30 mA/cm^2 current density was selected, which provided a proper plating rate of nearly 0.4 μm/min, with a small deviation, based on pre-experiments. The plating time was varied from 2 to 60 min at the constant current density of −30 mA/cm^2. The current was supplied to the Cu-plugged vias through via bottoms which were in contact with the Au layer. The sputtered Au layer connects all separate Cu plugs with ease, and ensures current supply to all Cu plugs without failure. A Cu tape was mechanically

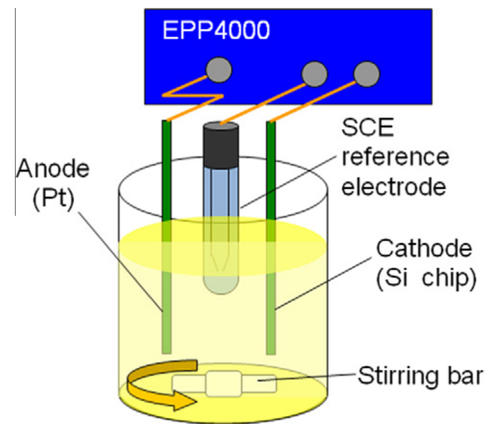

Fig. 1. Schematic diagram of the electroplating unit.

contacted with the Au layer by insulation tape and attached to the cathode (see Fig. 2).

The microstructures and dimensions of the electroplated bumps were assessed through FESEM (field emission scanning electron microscopy). The widths of the electroplated Sn bumps were estimated by assuming the top surface area of the Sn bump as circular in shape. The top surface area, A, was measured using an image analysis tool (the i-solution program by IMT i-Solution Inc.), and was divided by pi (π). The value of A/π was regarded as r^2, and the value of $2r$ as the width of the bump. The height of the Sn bumps was determined by the length from the top surface of the Cu-plugged TSV to the highest point of each Sn bump in a cross-sectional view.

3. Results and discussion

3.1. Polarization curve of the Sn electrolyte

Fig. 3 shows the polarization curve measured from the Sn electrolyte. From the curve, in the plus (+) sign region, the net oxidation current (hereafter, "oxidation current") flows, and electro-etching occurs on the cathode surface. In the minus (−) sign region, however, the net reduction current (hereafter, "reduction current") flows, and electroplating occurs on the cathode.

It was confirmed, as shown in Fig. 3, that −0.463 V (see point P) was the equilibrium potential (E_{eq}), where the net current became zero [18]. In the region between points P and R (region ⓑ), the

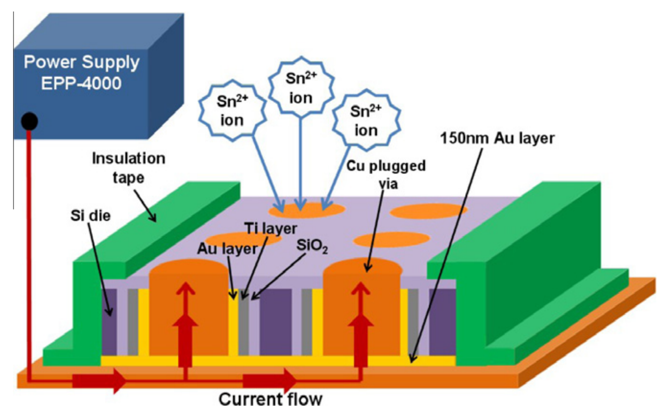

Fig. 2. Schematic diagram of the electroplating of Sn bumps on Cu-plugged vias without a PR mould.

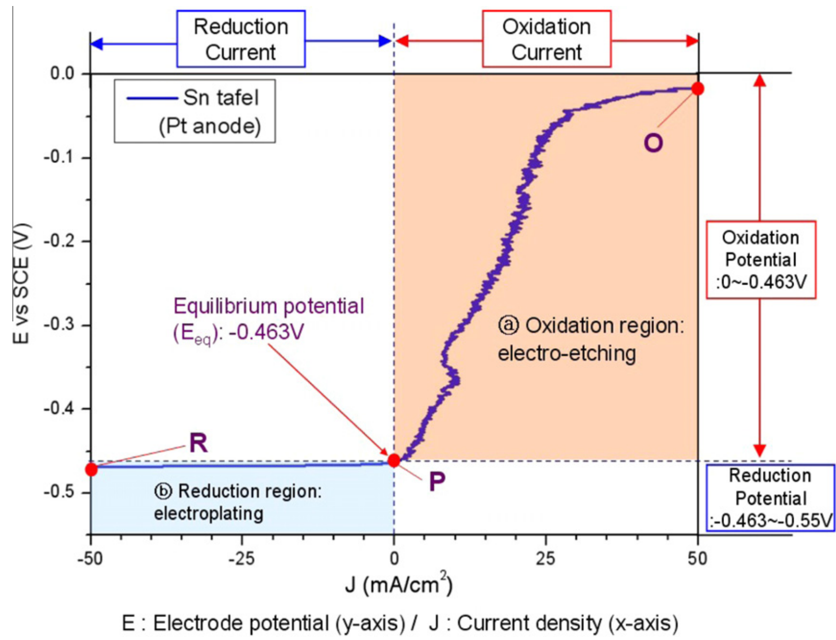

Fig. 3. Polarization curve of the Sn electrolyte.

reduction current flowed, and to ensure Sn reduction on the cathode, it was essential to keep an electropotential under −0.463 V in this study.

Fig. 4(a) presents the cathode surface appearance of a Cu-plugged via in the Sn electrolyte after exposure to the gradual potential change from 0 to −0.4 V and Fig. 4(b), from 0 to −0.55 V. Fig. 4(a) shows the electro-etching from the Cu-plugged via and Fig. 4(b) shows the dendritic Sn along the edge of the Cu-plugged via. The dendritic growth is attributed to the concentration of the current density around the via edge rather than on the surface.

3.2. Growth of the Sn bump

Fig. 5 shows the Sn bumps electroplated on the Cu-plugged TSV without a PR mould, with the plating time, at $-30\ mA/cm^2$. The bumps apparently did not have serious defects (see Fig. 5(a)) or uncontrollable bump growth to one side, which may cause an undesirable connection with the neighbouring bump and may result in an electrical short (see Fig. 5(b)). It was confirmed that the bumps were successfully produced without a PR mould.

The morphology of the Sn bumps in Fig. 5 was changed according to the plating time. At 2 min, small Sn deposits covered the whole surface of the Cu-plugged TSV. At 7 min, facets appeared clearly on the deposit, and the lengths of the facets reached approximately 4–10 μm. With increasing plating time, the preferred facets became larger, and in 60 min, some facets grew to as long as 40 μm.

Fig. 6 explains the growth mode of the Sn bumps by electroplating with and without a PR mould. Fig. 6(a) indicates bumping without a PR mould and Fig. 6(b), conventional bumping with PR. In Fig. 6(a), the deposits can grow to all directions, and the growth mode can be denoted as "anisotropic growth." In terms of morphology, the bump without a PR mould had a rivet-head shape with a relatively irregular periphery, as shown in Fig. 5. In Fig. 6(b), however, the lateral (width-direction) growth of the bump is deterred by the PR mould, but vertical-direction growth is promoted. These bumps had a smoother periphery, but in the case of the mushroom bump, the bump head was similar to the head of the non-PR bump [6,12].

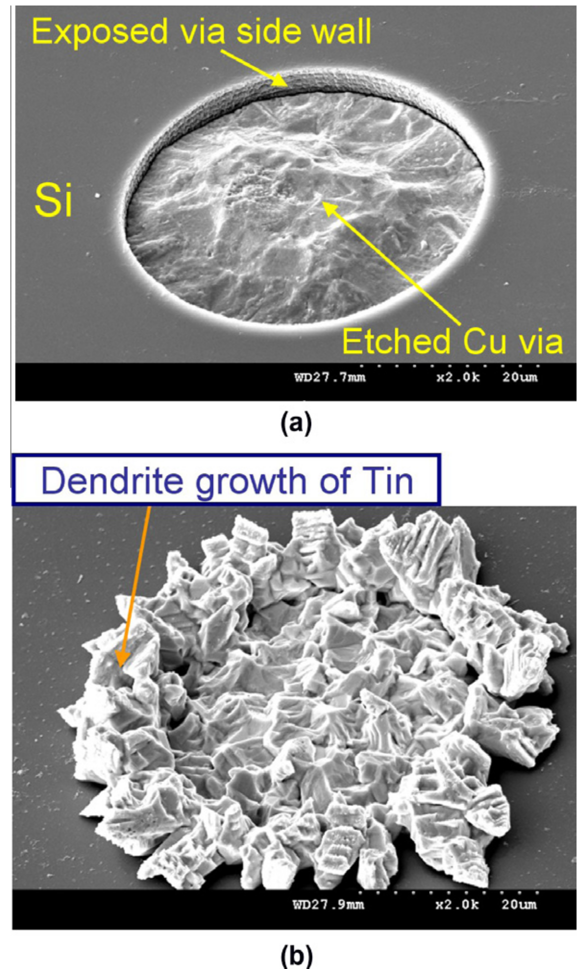

Fig. 4. Cathodes in the Sn electrolyte with the applied potentials (a) 0 to −0.4 V and (b) 0 to −0.55 V (scanning rate: −2 mV/s).

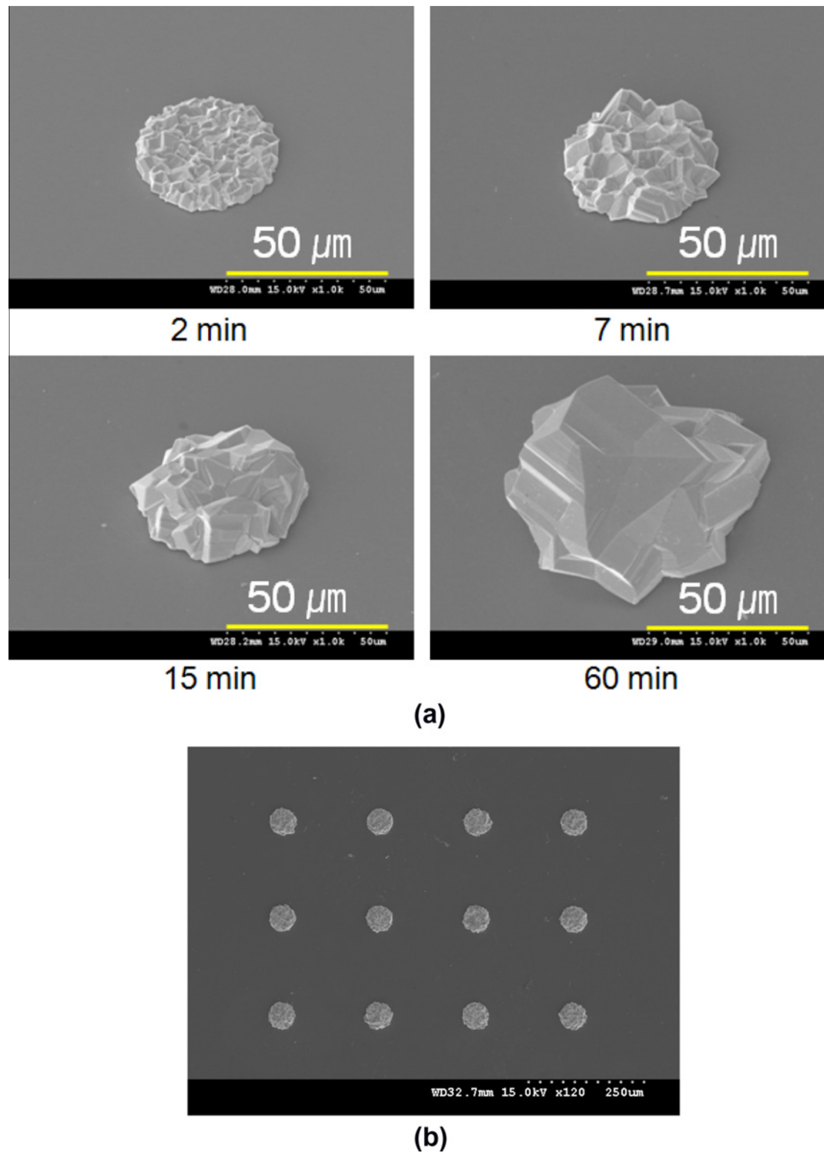

Fig. 5. Morphologies of Sn bumps electroplated without a PR mould according to the plating time at −30 mA/cm^2 (a) and arrayed bumps on a chip plated for 20 min (b).

Fig. 7 shows the cross-section of the electroplated Sn bumps on the Cu plugs. Each Sn bump bonded well to the Cu plug without any serious defect at the Cu/Sn interface. It was known that even in the just-electroplated state of Sn without heating, Cu_6Sn_5 was produced at the interface between Sn and the Cu plug through the diffusion of the Cu and Sn atoms, as determined through the TEM (transmission electron microscopy) analysis, and Sn and the Cu plug bonded well [7].

Fig. 8 shows the Sn bump height with a plating time of up to 60 min. The bump height increased from 2.8 to 39.1 μm when the plating time was raised from 2 to 60 min. The standard deviation of the bump height under 10 min was less than 1 μm, but at over 15 min, the standard deviation became approximately over 3 μm. The reason for the large deviation after 15 min may be the growth of the preferred facet, as shown in Fig. 5.

The overall growth rate of the bump height (the slope of the graph in Fig. 8) with time tended to reduce with increased plating time. It was mostly constant, however, in the electroplate-bumping process with a PR mould [12] as well as in the electroplating of Sn on a plate [19] or Cu on a wafer [20]. In non-PR bumping, a longer plating time provides a larger bump diameter due to the absence of a PR mould, such as 62.8 μm at 30 min in Fig. 9, which increases the plated area to approximately 2.5 times larger than the initial Cu plug diameter of 40 μm. Under the constant via area of the current path, the enlarged bump surface decreased the current density so that the plating and growth rates of the bump height would be reduced.

Fig. 9 shows the growth of the Sn bump width according to the plating time. The width increased from 41.6 to 75.8 μm as the plating time was raised from 2 to 60 min. Generally, in electroplate bumping with a PR mould, the growth of the bump width is confined by the PR mould. In this non-PR-mould process, however, the growth of the bump width cannot be confined, and the width increased.

Since the width growth cannot be confined by the PR mould in non-PR bumping, the uniformity of the bump widths is important to avoid unwanted contact with neighbouring bumps and to obtain a reliable bump size. Fig. 10 shows the bump arrays on the Si chip plated without a PR mould; the bump uniformity looked quite good. The uniformity of the bump height was calculated in this

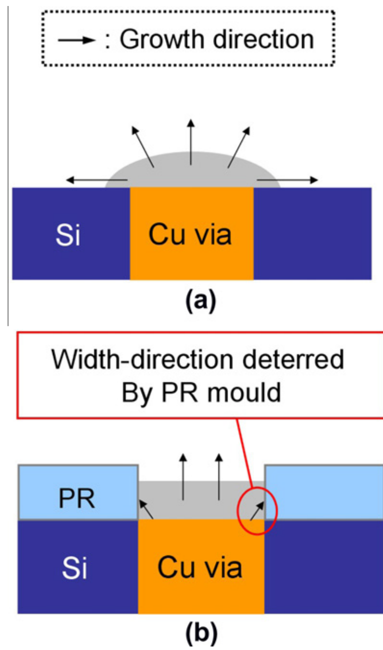

Fig. 6. Growth mode of the Sn bumps in electroplating with and without a PR mould: (a) bumping without a PR mould and (b) conventional PR bumping.

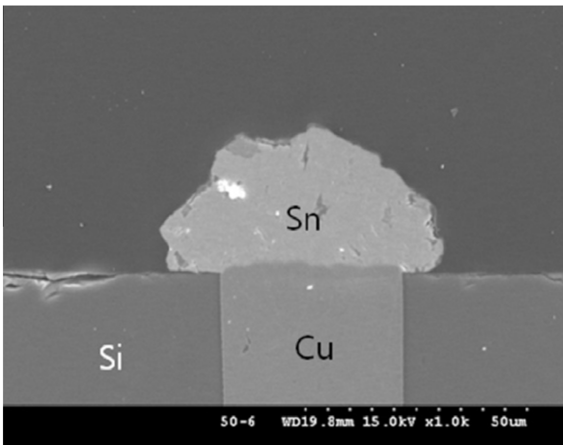

Fig. 7. Cross-section of an electroplated Sn bump on a Cu plug without a PR mould (30 mA/cm^2, 30 min).

study using the formula [1 – (maximum height – minimum height)/(2 × average height)] × 100 (%), which is similar to the formula used by Kim and Ritzdorf [(maximum height – minimum height)/(2 × average height)] × 100 (%) [19]. The uniformity of the bump width can also be calculated similarly by substituting width for the height. In this study, the higher the value of uniformity, the better the uniformity of the bump size; conversely, in the formula used by Kim and Ritzdorf the lower the value of uniformity, the better the uniformity of the bump size.

Fig. 11 shows the uniformities of the height and width of the Sn bumps produced without a PR mould. The uniformity of the bump width was between 93.2% (at 30 min) and 97.5% (at 2 min), and the height uniformity was between 78.8% (at 15 min) and 96.4% (at 2 min). The uniformities looked good in spite of the fact that non-PR electroplating was employed. Especially, the electroplating time of less than 10 min gave high uniformity (over 90%) to both the width and the height, which is comparable to the uniformity

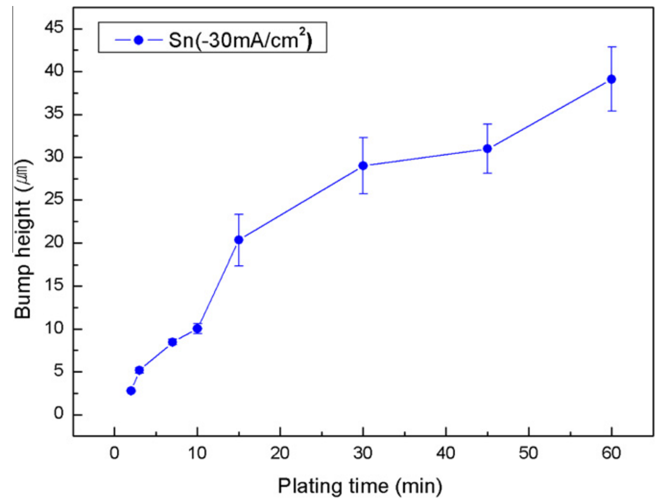

Fig. 8. Sn bump height versus electroplating time.

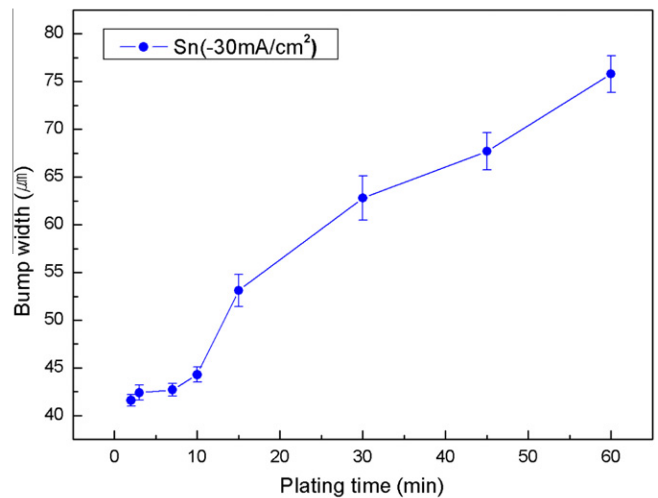

Fig. 9. Sn bump width versus plating time at −30 mA/cm^2.

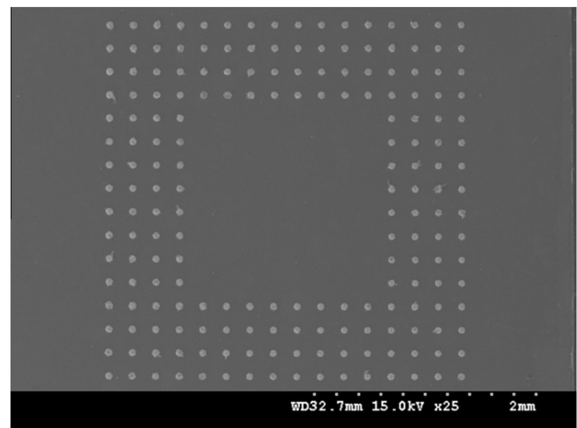

Fig. 10. Electroplated bump arrays on a Si chip without a PR mould (plating at −30 mA/cm^2 for 20 min).

values obtained in the PR bumping of Sn–Ag [16] and eutectic SnPb and Cu [17]. In this study, however, uniformity was estimated for the limited bumps produced on a chip, and further work for the wafer level is required.

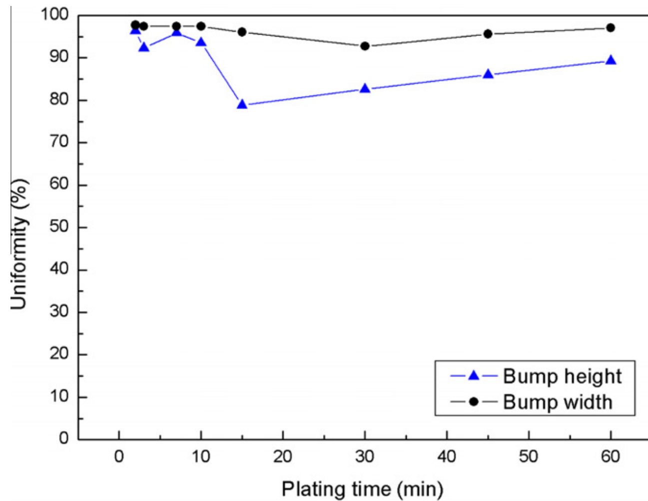

Fig. 11. Uniformities of the Sn bump heights and widths fabricated without a PR mould.

4. Conclusions

The feasibility of electroplate Sn bumping on Cu-plugged vias without a PR mould was investigated for 3D chip stacking. Specifically, the electroplating characteristics and the bump size were examined. The results can be summarized as follows:

(1) Electroplate Sn bumps were produced successfully without a PR mould using a Pt anode on a Cu-plugged TSV in a Si chip. The bumps had rivet-head shapes, and their appearance did not show serious defects.
(2) In the Sn electrolyte, the reduction potential of the Sn ion was revealed to be −0.463 V by the polarization curve, and the Sn ion began to be deposited under this potential.
(3) The Sn bumps grew in both the vertical (thickness) and lateral (width) directions with the plating time because there was no PR mould. The bump height increased from 2.8 to 39.1 μm, and the width from 41.6 to 75.8 μm, when the plating time was raised from 2 to 60 min at −30 mA/cm^2.
(4) The uniformities of the bump width and height on a chip became over 90% within 10 min of plating time, without a PR mould.

Acknowledgement

This study was conducted with support from the Seoul R&BD program (JP100096 and No. 10890).

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