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A New Non-PRM Bumping Process by Electroplating on Si Die for Three Dimensional Packaging

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A new bumping process on a Si die by electroplating without a photo-resist-mold (PRM) was assessed for the three dimensional (3D) stacking of Si dice. In this process, solder bumps were deposited selectively onto the surface of a Cu plugged-through silicon-via (TSV) in a Si die. Since lithography related processes to make a PRM for solder bumping were omitted, it can reduce the production time and cost for bumping. The substrate was a Si wafer, and TSVs were produced by deep-ion-reactive-etching (DRIE). As an insulation layer, SiO_2 was formed by high-density-plasma-chemical-vapor-deposition (HDPCVD) or wet oxidation method. A Ti adhesion and an Au seed layers were deposited by sputtering. Cu was plugged into the vias by pulsed direct-current (DC) electroplating. The backside of the Si wafer was ground by chemical-mechanical-polishing (CMP). Sn bumps were electroplated on the Cu plugged vias by a current supplied through a Cu-overplated layer (COL) on the vias surface. As experimental results, wet oxidation provided a uniform SiO_2 thickness through the via depth, whereas the SiO_2 thickness by HDPCVD decreased with the via depth. The Ti and Au thicknesses also decreased along the via depth. In electroplating for Cu plugging, defect-free Cu plug was achieved by pulsed DC for 18 h, where one cycle composed of a 5 s cathodic term with $-12.2\,mA{\cdot}cm^{-2}$ and a 25 s anodic term with $2.3\,mA{\cdot}cm^{-2}$. Sn bumping using COL without PRM was accomplished successfully at a current density of $-30\,mA{\cdot}cm^{-2}$ for 15 min. The diameter and height of the Sn bumps ranged from 48.5 to 52 μm and 22 to 25 μm, respectively. The bumps had a rivet head shape without a columnar part and showed facets on the bump surface. The COL was removed by CMP without damage to the bumps.
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1. Introduction

Advanced microelectronic device architectures such as multichip modules (MCMs) and system in packages (SiPs) require a high interconnection density. In electronics packaging, demands for high performance and smaller size of an electronic device have been addressed by decreasing pitch and connection length. However, conventional two dimensional packaging technologies have some limitations in fully satisfying these demands.

In order to meet this trend, many studies have examined three dimensional (3D) packaging as a noble concept.[1–3] Significant decreases in power consumption, size and weight can be expected by the application of 3D packaging.[2] In particular, 3D packaging with through-silicon-via (TSV) can minimize the total length of the current path as well as signal delay.

For the achievement of 3D stacking structures with TSV, key processes including via fabrication, conductive material plugging and bumping for connecting plugged vias need to be developed. For the via fabrication, DRIE (Deep Ion Reactive Etching) process is popular because it provides vias with relatively precise dimensions. An insulating layer of SiO_2 on the via wall can be fabricated by CVD (Chemical Vapor Deposition) or by oxidation methods.[4–8] Ti, which enhances the adhesion between the insulation and seed layer, has been widely adopted as an adhesion layer.[4,5,9] Cu is frequently used as a seed layer due to its low cost and lower electrical resistivity.[1,10–12] However, Au can be used instead of Cu due to its chemical stability in electrolytes and good oxidation resistance, which removes the need for oxide pre-cleaning on the seed layer.

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Cu is a popular material for plugging vias. For Cu deposition, an electro-plating method[1,13] is preferred to an electroless process[14] because the latter has a low plating speed[15] and an inability to form a deposit layer more than 1 μm thick.[16] However, when an electroplating method is applied, defects such as voids or fillets can be produced during Cu plugging.[1,14,17] To overcome these issues, chemical additives may be added[18] and/or the current waveform[19] can be modified. In this study, modification of the current waveform was used to avoid defects in the Cu plugs.

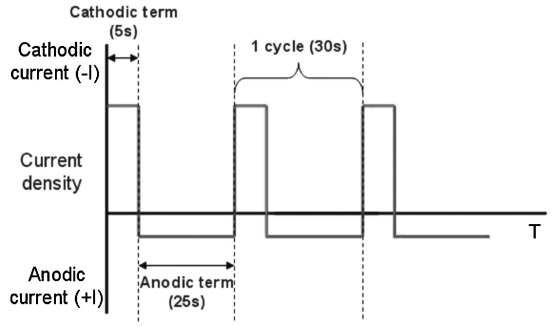
The fabrication of solder bumps is one of the design strategies to connect Cu plugged vias embedded in a Si die. As a bumping method, electroplating is considered to be a suitable process due to its efficiency in fabricating smaller sized and narrower pitched bumps.[20] Electroplating processes for solder bumps generally employ a photo-resist-mold (PRM) on a Si wafer[20–26] to confine the cathode surface area and control the shape of the deposits. However, applying a PRM requires a series of processes; PR coating, ultra-violet (UV) exposure, development and PR removal, which involve extra time and cost.

In this study, a new process for Sn bumping on a Si die by electroplating without PRM was proposed to save processing cost and time of a bumped Si die for 3D stacking. The new process adopts a Cu-overplated layer (COL) as a current path for the electroplating of Sn bumps and does not require PRM fabrication and removal processes.

2. Experimental

2.1 Via fabrication and Cu plugging

A ⟨100⟩ p-type silicon wafer, 100 mm in diameter and 500 μm in thickness, was used as a starting substrate. For via



	Cathodic term (5s)	Anodic term (25s)	Total plating time
Current pulse A	-40.0mA·cm^{-2}	7.6mA·cm^{-2}	1h
Current pulse B	-12.1mA·cm^{-2}	2.3mA·cm^{-2}	18h

Fig. 1 Two types of pulsed current waves for Cu plugging.

fabrication, DRIE was conducted on the Si wafer to produce 50,688 cylindrically shaped vias, 40 µm in diameter and 70 µm in depth. As an insulation layer, a 1 µm thick SiO_2 layer was formed either by wet oxidation or high-density-plasma-chemical-vapor-deposition (HDPCVD) for comparison. For the wet oxidation treatment, the Si wafer with the vias was placed in a furnace, and heated to 1000°C in a N_2 gas atmosphere. H_2O vapor was then supplied with N_2 gas for 3 h to form a SiO_2 layer on the via walls. In HDPCVD, SiH_4, O_2 and Ar mixed gas was supplied to the chamber where the Si-wafer had been placed. A potential bias was applied to generate a plasma of the mixed gas in the chamber, and SiH_4 and O_2 gas reacted to form a SiO_2 layer on the via walls. The total reaction time was 17 min, and the reaction temperature on the Si surface was maintained at 250°C. The thicknesses of the SiO_2 layers by HDPCVD and wet oxidation were measured at various via depths by analyzing the secondary-electron (SE) images of the cross-sectioned vias. In the SE images, Si and SiO_2 have different contrast, and the thickness of SiO_2 was measurable.

Ti and Au as an adhesion and seed layer, respectively, were deposited on the SiO_2 layer by successive sputtering. The target thicknesses of the Ti and Au layers were 300 and 500 nm, respectively. Before depositing the Ti and Au layers, Ar plasma etching with 500 W RF (Radio Frequency) was performed. The thicknesses of the Ti/Au layers on the SiO_2 formed by HDPCVD and wet oxidation were measured from the contrast and morphological differences between Ti/Au and SiO_2 using same method as the previous SiO_2 layer measurement.

To fabricate the Cu plugs into the vias, two different types of pulsed direct-current (DC) waveform, pulse A and B, were applied (see Fig. 1). The plating times were 1 h and 18 h for pulse A and B, respectively. Cu balls, 30 mm in diameter, contained in a Ti-mesh basket were used as an anode. The Si wafer with the seed layers was connected as a cathode. The electrolyte for Cu plating consisted of 67 g·l^{-1} of $CuSO_4 \cdot 5H_2O$, 92.4 ml·l^{-1} of H_2SO_4, 0.04 ml·l^{-1} of HCl and other additives, such as an inhibitor and leveler. The electrolyte in the plating bath was stirred constantly by a

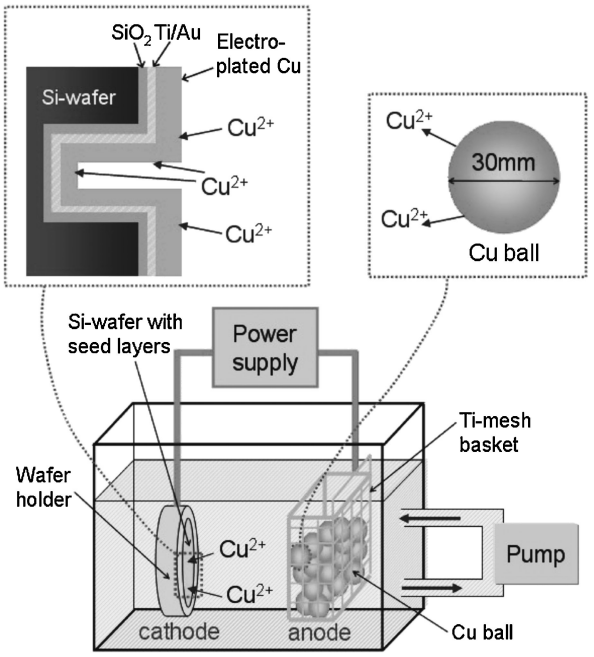


Fig. 2 Schematic diagram of the electroplating cell for Cu plugging.

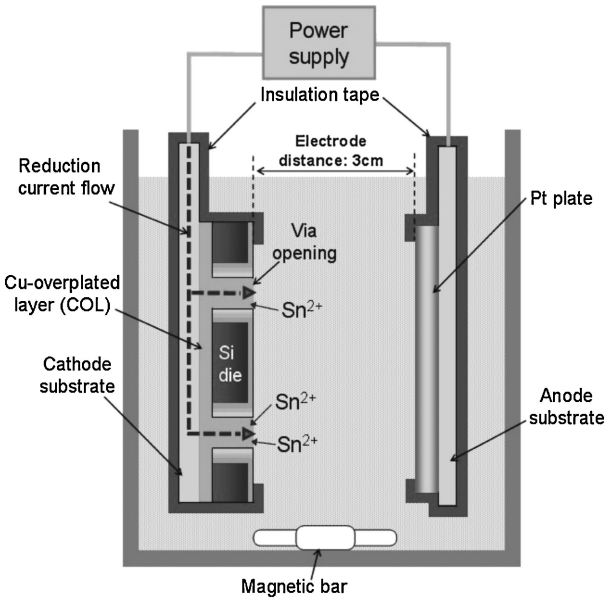


Fig. 3 Schematic diagram of the reduction current flow from the cathode substrate to via opening.

circulating pump and kept at room temperature during electroplating. Figure 2 shows a schematic diagram of plating cell for Cu plugging.

2.2 Non-PRM Sn bumping

For electroplating Sn bumps without a PRM on the Cu plugged vias, the backside of each Si wafer was ground by chemical-mechanical-polishing (CMP) until the bottoms of the Cu plugged vias were exposed. The background Si wafer was cut into 264 square dice, $5 \times 5\,mm^2$ in each, using a diamond saw. Each Si die was placed on a cathode set for Sn bumping (see Fig. 3), and a reduction current was supplied from the cathode to Cu plugged via through a Cu-overplated

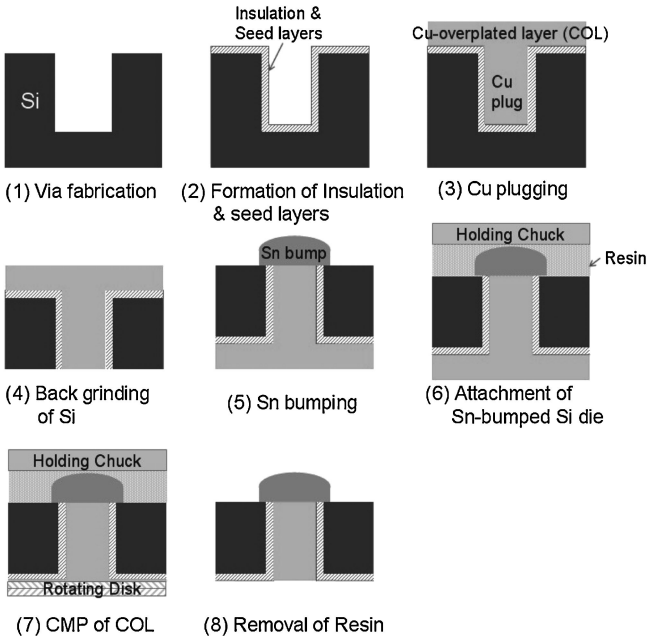


Fig. 4 Process flow for producing a bumped Si die by non-PRM.

layer (COL) on the backside of a die. The anode was a $10 \times 10\,\mathrm{mm}^2$ Pt plate, and the distance between cathode was 3 cm.

To fabricate the Sn bumps, a DC with the density of $-30\,\mathrm{mA \cdot cm^{-2}}$ was applied for 15 min. The Sn electrolyte consisted of $42.8\,\mathrm{g \cdot l^{-1}}$ of $SnSO_4$, $106.8\,\mathrm{ml \cdot l^{-1}}$ of H_2SO_4, and other minor additives of an inhibitor and leveler. The Sn electrolyte was stirred by 200 rpm (revolutions per minute) using a rotating magnetic bar, and kept at room temperature during electroplating. After Sn bumping, the COL was removed by CMP. Figure 4 shows a schematic diagram of non-PRM process flow from the fabrication of vias to the Sn bumps.

3. Results and Discussion

3.1 Functional layers on via walls

Prior to fabricating the non-PRM bumps by electroplating, the insulation, adhesion and seed layers were deposited on the via walls, and Cu plugging was performed. Figure 5 shows the thicknesses of SiO_2 insulation layers formed on the via side walls using HDPCVD and wet oxidation methods. In the case of HDPCVD, the thickness of the SiO_2 layer decreased with increasing via depth. For example, the SiO_2 layer was 1.02 µm in thickness at the via depth of 5 µm, whereas the thickness reduced to 0.30 µm at the via depth of 65 µm, which is around 70% decrease. On the other hand, SiO_2 layer formed by wet oxidation showed almost constant thickness, from 1 to 1.1 µm, through the via depth.

The difference in thickness from the two methods was attributed to the different production mechanism of SiO_2. In the HDPCVD method, SiO_2 is deposited by a reaction of two external gases, SiH_4 and O_2, at the via surface. In a confined space such as the bottom of a via, it is difficult for gas reactants to maintain the appropriate concentration and reaction rate. This results in thinner SiO_2 layer at deeper part in the vias, which concurs with a prior report describing

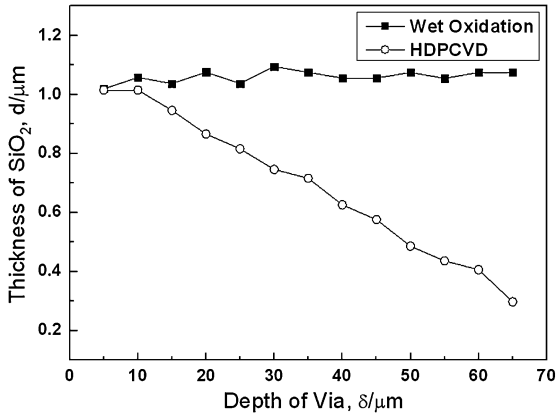


Fig. 5 Thickness variation of SiO_2 layers fabricated by wet oxidation and HDPCVD at various depths within the vias.

the lack of deposition became severe when the aspect ratio (depth to width) of the via was large.[27]

However, in the wet oxidation method, the SiO_2 layer is produced by direct chemical reaction between the Si via surface and supplied H_2O vapor. Once the SiO_2 layer is formed on the via wall, it operates as a barrier against the diffusion of H_2O vapor into the inner Si layer for further oxidation. Due to this interruption effect by the existing SiO_2 layer, the growth rate of SiO_2 decreases with time. Accordingly, the thickness of SiO_2, d, is proportional to square root of the oxidation time; $d \propto \sqrt{t}$.[28] The interruption effect reduces the SiO_2 growth rate at the part of the thicker SiO_2 film, whereas it has less effect on growth in thinner SiO_2 area. Consequently, in the wet oxidation method, the thickness of SiO_2 could become almost constant through the via depth.

Although the wet oxidation method provided an even SiO_2 layer, it requires a high reaction temperature of 1000°C, which exceeds what a conventional CMOS structure can tolerate. Therefore, the wet oxidation method is only applicable when vias are formed before the formation of a CMOS structure in a Si wafer. On the other hand, the HDPCVD method can fabricate SiO_2 layer at relatively low temperatures (250°C), which makes this process applicable to the Si die that already contains CMOS structures. Despite the thinner SiO_2 layer at the deeper parts of the via walls, HDPCVD is a more suitable if the thinnest part of SiO_2 has sufficient electrical insulation.

Figure 6 shows the thicknesses of the Ti and Au layers on the SiO_2 layer in the vias. The thickness profiles were similar and not affected seriously by the SiO_2 depositing method of HDPCVD or wet oxidation. At the via top, the thicknesses of the Ti/Au formed by HDPCVD and wet oxidation were 510 and 530 nm, respectively. At a depth of 65 µm from the via top, the Ti/Au thicknesses by HDPCVD and wet oxidation became 80 and 71 nm, respectively. The thickness at a depth of 65 µm was approximately 15% compared to that of the top. This is because the probability of deposition at the via depends on the incidence angle of Ti and Au atoms to the via. While the top part of the via can be hit by atoms from both low and high incidence angles, the bottom part of the via can only be hit by atoms from a high incidence angle. Therefore, the bottom part of the via has a lower probability to be hit by Ti and Au atoms than the top for deposition. The hit

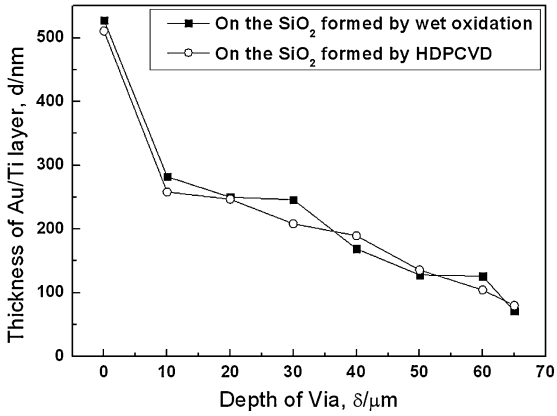


Fig. 6 Thickness variations in the Ti/Au layer deposited on the SiO_2 layers fabricated by wet oxidation and HDPCVD.

probability decreases further with increasing aspect ratio of the via, which results in a thinner deposition layer near the bottom of the via.[29)]

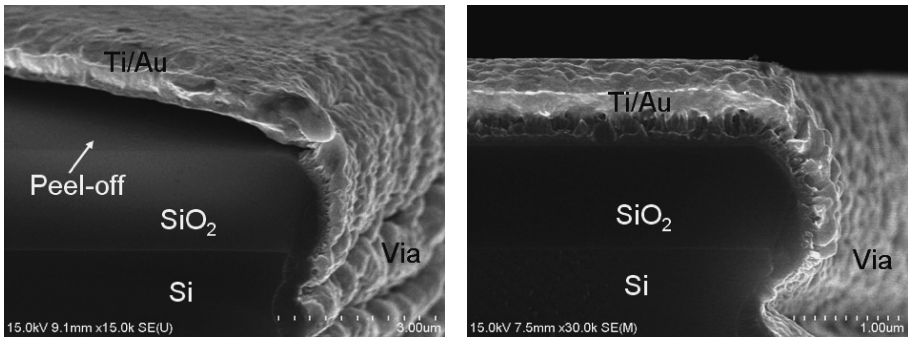
Figure 7(a) and (b) show the sputtered layers of Ti and Au on the wafer surface and side wall of the via without and with Ar plasma pre-etching, respectively. In Fig. 7(a), the Ti/Au layers had detached from the wafer surface. However, in Fig. 7(b) Ti/Au layers showed good adhesion to the via wall due to Ar plasma etching for 60 s with 500 W. Plasma etching has been reported to enhance the adhesive strength of polyethylene through an anchor effect,[30)] namely, the adhesive strength increases with increasing surface roughness. In this study, Ar plasma pre-etching was assumed to have a similar effect to improve adhesion. From the result of Fig. 7, Ar plasma etching can be recommended to achieve better adhesion of seed layers for the following Cu-plugging process.

3.2 Cu plugging and non-PRM Sn bumping

Figure 8(a) and (b) show cross sections of the Cu plugged vias plated by pulsed currents A and B, respectively, as defined in Fig. 1. In Fig. 8(a), a kernel-shaped void was observed at the center of the Cu plug. On the other hand, no void was found in Fig. 8(b). According to previous studies, this kind of void defect was produced by early closing of Cu deposits due to the intensified current concentration on the edge of the via opening.[31,32)]

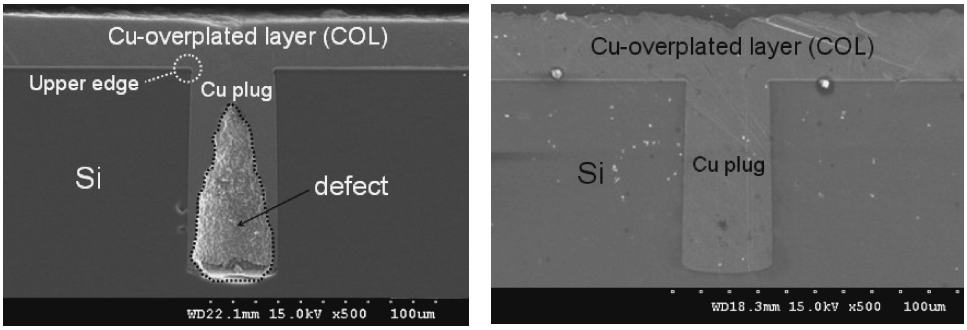
In pulse electro-plating, an effective reduction charge can be obtained by subtracting the electrical charge of the oxidation term from that of the reduction term.[21)] According to this, pulse A and B were calculated to apply different amount of reduction charges in a cycle; -2.5×10^{-3} C·cycle^{-1} for A and -7.5×10^{-4} C·cycle^{-1} for B. Pulse A has 3.3 times more reduction charge than pulse B. This produced higher current concentration at the via edge for the pulse A, and early closing of the via opening.

Figure 9(a) and (b) present the face surface and cross-section of the background Si die with Cu plug. Sn ions deposited selectively on the 'P' area in Fig. 9(a) and (b) by



(a) (b)

Fig. 7 Ti/Au coating state on the wafer surface and side wall of the via; (a) without Ar plasma pre-etching, (b) with Ar plasma pre-etching.



(a) (b)

Fig. 8 Cross sectioned images of a Cu plugged Si die; (a) Cu plug by current pulse A (-40.0 mA·cm^{-2} for 5 s and 7.6 mA·cm^{-2} for 25 s), (b) Cu plug by current pulse B (-12.1 mA·cm^2 for 5 s and 2.3 mA·cm^2 for 25 s).

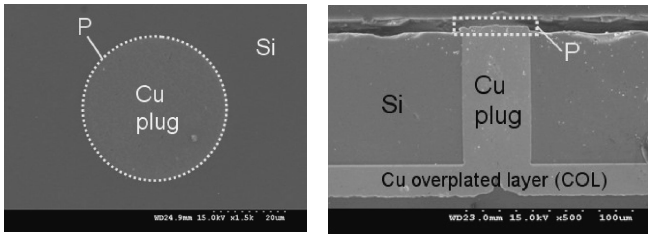


Fig. 9 Back ground Si die with Cu over plated layer; (a) top surface, (b) cross section.

the current applied through the Cu-overplated layer (COL) and Cu plug. The basic bumping scheme was explained previously in Fig. 3.

Figure 10 shows Sn bumps on Cu plugs produced without a photo-resist-mould (PRM). The Sn bumps were electroplated at a current density of $-30\,\mathrm{mA\cdot cm^{-2}}$ for 15 min. The diameter and height of the bumps ranged from 48.5 to 52 µm and 22 to 25 µm, respectively. Serious defect was not found in the Sn bumps. The bump had a rivet head shape that is similar to the bump head produced using a PRM. The bump electroplated using a PRM commonly has a mushroom shape with a columnar part which is as high as the PRM thickness.[33] Characteristics of non-PRM Sn bumps were discussed and compared with those of conventional solder bumps fabricated by a PRM in authors' another report.[34]

Although Sn bump by non-PRM showed a different morphology from the conventional bump by a PRM, the non-PRM bumps on a chip had a little deviation in diameter and height, 3.5 and 3 µm, respectively. Thus, the feasibility of small deviation of Sn bumps by the non-PRM process may be favorable as a connection for 3D chip stacking.

Figure 10(b) shows a cross-section of bumped Si die with a COL. The COL should be removed before stacking the Si die for 3D packaging. A CMP process was applied to the Si die to remove the COL. The rotating speed and pressing force of the disc were 50 rpm and $20\,\mathrm{N\cdot cm^{-2}}$, respectively. In Fig. 10(d), it is clear that the COL was removed from the bottom of Si die. Despite the pressing and shear stresses on the Si die during CMP, there was no evidence of damage or cracks on the Sn bumps and the Si die. Figure 10(c) shows the face surface of the Sn bump after CMP. Compared to Fig. 10(a), before CMP, the face surface of Sn bump also showed no signs of noticeable damage or change.

4. Conclusions

A new process of Sn bumping on Cu plugged vias in a Si die by electroplating without a photo-resist-mould (PRM) was proposed. The new process for solder bumping on the Si die does not require a series of lithography processes related to the PRM. The results can be summarized as follows:

(1) Sn bumps were fabricated successfully by electroplating without a PRM on the Cu plugged vias in a Si die. The electroplating current for Sn deposition was supplied through a Cu-overplated layer (COL) on the backside of the Si die and Cu plugs.

(2) The bumps without a PRM had rivet head shapes lacking of a columnar part, and the diameter and height of the bumps ranged from 48.5 to 52 µm and 22 to 25 µm, respectively, at a current density of -30 $\mathrm{mA\cdot cm^{-2}}$ for 15 min.

(3) The SiO_2 insulation layer on the via walls fabricated by wet oxidation had an almost uniform thickness of approximately 1.1 µm. On the other hand, in case of

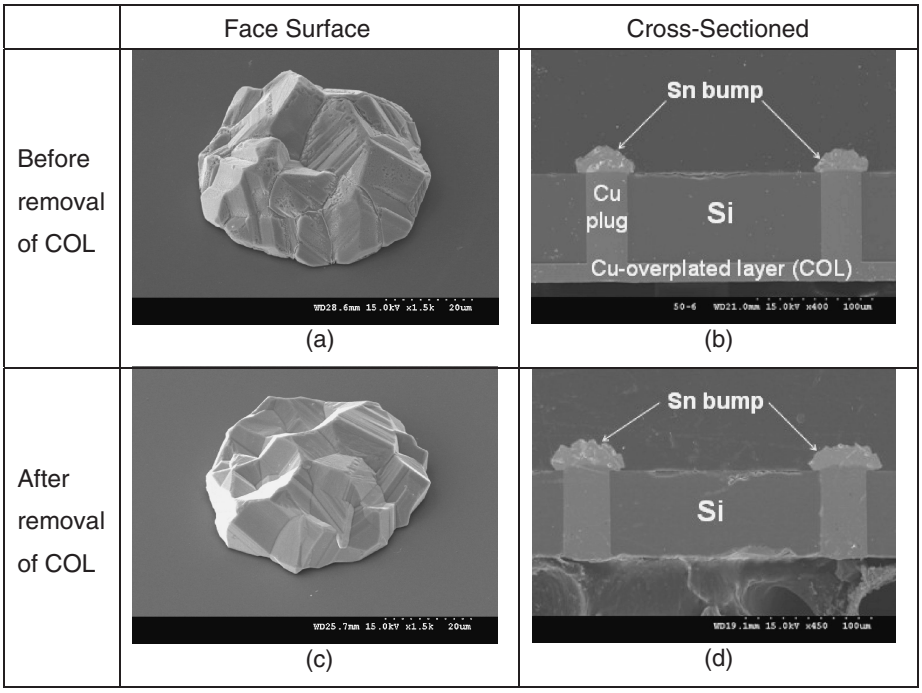


Fig. 10 Face surface and cross sectioned images of a Sn bumped Si dice before and after removing the Cu over-plated layer; (a) face surface before removal, (b) cross sectioned view before removal, (c) face surface after removal, (d) cross sectioned view after removal.

the HDPCVD method, the thickness of the SiO_2 layer decreased with increasing via depth.

(4) Cu was plugged into the vias by electroplating for 18 h using pulsed wave current composed of -12.1 $mA{\cdot}cm^{-2}$ for 5 s and 2.3 $mA{\cdot}cm^{-2}$ for 25 s, and void defect was not observed. However, a larger reduction charge in a cycle caused a central void in the Cu plugs by early closing of the via openings.

(5) After electroplating Sn bumps on a Si die, COL was removed by CMP without imposing a damage on the Sn bumps and Si die when the rotating speed and pressing force of the disc were 50 rpm and 20 $N{\cdot}cm^{-2}$, respectively.

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REFERENCES

1) K. Takahashi, H. Terao, Y. Tomita, Y. Yamaji, M. Hoshino, T. Sato, T. Morifuji, M. Sunohara and M. Bonkohara: Jpn. J. Appl. Phys. **40** (2001) 3032–3037.
2) S. F. Al-sarawi, D. Abbott and P. D. Franzon: IEEE Trans. CPMT-part B **21** (1998) 2–14.
3) K. Hara, Y. Kurashima, N. Hashimoto, K. Matsui, Y. Matsuo, I. Miyazawa, T. Kobayashi, Y. Yokoyama and M. Fukazawa: IEEE Trans. Adv. Pack. **28** (2005) 367–376.
4) H. Ronald, L. S. W. Ricky, Z. X. Shawn and C. K. Wong: Proc. 7th Electron. Packag. Tech. Conf., (IEEE **2** 2005) pp. 384–389.
5) L. S. W. Ricky, H. Ronald, Z. X. Shawn and C. K. Wong: Proc. 7th Electron. Pack. Tech. Conf., (IEEE **1** 2005) pp. 795–801.
6) T. Kenji, T. Hiroshi, T. Yoshihiro, Y. Yasuhiro, H. Masataka, S. Tomotoshi, M. Tadahiro, S. Masahiro and B. Manabu: Jpn. J. Appl. Phys. **40** (2001) 3032–3037.
7) H. Kazumi, K. Yohei, H. Nobuaki, M. Kuniyasu, M. Yoshihide, M. Ikuya, K. Tomonaga, Y. Yoshihiko and F. Motohiko: IEEE Trans. Adv. Pack. **28** (2005) 367–376.
8) D. Henry, N. Sillon, D. Belhachemi, C. Bruunetmanquat, C. Puget and G. Ponthenier: Proc. Electron. Syst. Tech. Conf., (IEEE 2006) pp. 274–281.
9) S. W. Ho, S. W. Yoon, Q. Zhou, K. Pasad, V. Kripesh and J. H. Lau: Proc. 58th Electron. Comp. Tech. Conf., (IEEE 2008) pp. 1946–1952.
10) K. Ishihara, C. F. Yung, Arturo and M. Martin: J. Microelectromech. Sys. **8** (1999) 403–408.
11) A. Yu, N. Khan, G. Archit, D. Pinjala, K. C. Toh, V. Kripesh, S. W. Yoon and J. H. Lau: Proc. 58th Electron. Comp. Tech. Conf., (IEEE 2008) p. 24.
12) G. Ritter, P. McHugh, G. Wilson and T. Ritzdorf: Sol. Sta. Electron. **44** (2000) 797–807.
13) R. Nagarajan, K. Prasad, L. Ebin and B. Narayanan: Sens. Act. A **139** (2007) 323–329.
14) P. P. Lau, C. C. Wong and L. Chan: Appl. Surf. Sci. **253** (2006) 2357–2361.
15) G. Yingpeng, G. Zhancheng and L. Weichang: Mat. Lett. **59** (2005) 667–670.
16) B. James: *Design for Manufacturability Handbook, 2nd ed.*, (McGraw-Hill Professional, New York, 1998) pp. 8–33.
17) K. Takahashi, M. Umemoto, N. Tanaka, K. Tanida, Y. Nemoto, Y. Tomita, M. Tago and M. Bonkohara: Microelectron. Relia. **43** (2003) 1267–1279.
18) D. Weiping, L. Chihchan, S. Yongchih, S. Shaoping, H. Chenchia, L. Cliff, H. Bob and H. Shar: Electroch. Acta **54** (2009) 5894–5901.
19) D. Pradeep and M. Jianmin: J. Electroch. Soc. **153** (2006) G552–G559.
20) B. Kim and T. Ritzdorf: J. Electroch. Soc. **150** (2003) C577–C584.
21) B. Neveu, F. Lallemand, G. Poupon and Z. Mekhalif: Appl. Surf. Sci. **252** (2006) 3561–3573.
22) M. Bigas and E. Cabruja: Microelectron. J. **37** (2006) 308–316.
23) S. W. Jung, J. P. Jung and Y. N. Zhou: IEEE Trans. Adv. Pack. **29** (2006) 10–16.
24) J. Helneder, C. Hoyler, M. Schneegans and H. Torwesten: Microelectron. Eng. **82** (2005) 581–586.
25) H. Hwang, S. M. Hong, J. P. Jung and C. S. Kang: Sold. Surf. Mount Tech. **15** (2003) 10–16.
26) S. Arai, H. Akatsuka and N. Kaneko: J. Electroch. Soc. **150** (2003) C730–C734.
27) F. Sami: *Introduction to Microfabrication, 1st ed.*, (Wiley, England, 2004) p. 86.
28) G. S. May and C. J. Spanos: *Fundamentals of Semiconductor Manufacturing and Process Control*, (Wiley, England, 2006) pp. 28–29.
29) T. Karabacaka and T. M. Lu: J. Appl. Phys. **97** (2005) 124504.
30) M. Tahara, N. K. Cuong and Y. Nakashima: Surf. Coat. Tech. **173–174** (2003) 826–830.
31) J. M. Quemper, E. D. Gergam, N. F. Rodriguez, J. P. Grandchamp and A. Boseboeuf: J. Micromech. Microeng. **10** (2000) 116–119.
32) A. C. West, C. C. Cheng and B. C. Baker: J. Electrochem. Soc. **145** (1998) 3070–3074.
33) H. R. Jung, H. H. Kim and W. J. Lee: J. Electron. Mater. **35** (2006) 1067–1073.
34) S. J. Hong, J. H. Jun, J. P. Jung, M. Mayer and Y. Zhou: IEEE Trans. Adv. Pack. (2010) in press.