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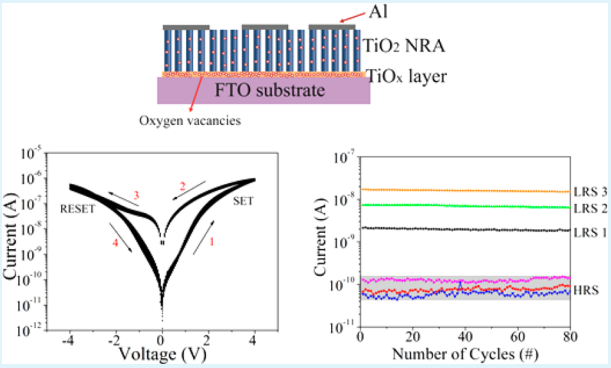
Reliable and Low-Power Multilevel Resistive Switching in TiO_2 Nanorod Arrays Structured with a TiO_x Seed Layer

Ming Xiao,[†,‡,§] Kevin P. Musselman,[†,‡,§] Walter W. Duley,[†,∥] and Y. Norman Zhou*[,†,‡,§]

[†]Centre for Advanced Materials Joining, [‡]Waterloo Institute of Nanotechnology, [§]Department of Mechanics and Mechatronics Engineering, and [∥]Department of Physics and Astronomy, University of Waterloo, Waterloo, Ontario N2L 3G1, Canada

Supporting Information

ABSTRACT: The electrical performance of TiO_2 nanorod array (NRA)-based resistive switching memory devices is examined in this paper. The formation of a seed layer on the fluorine-doped tin oxide (FTO) glass substrate after treatment in $TiCl_4$ solution, before the growth of TiO_2 NRAs on the FTO substrate via a hydrothermal process, is shown to significantly improve the resistive switching performance of the resulting TiO_2 NRA-based device. As fabricated, the Al/TiO_2 NRA/TiO_x layer/FTO device displayed electroforming-free bipolar resistive switching behavior while maintaining a stable ON/OFF ratio for more than 500 direct sweeping cycles over a retention period of 3×10^4 s. Meanwhile, the programming current as low as $\sim 10^{-8}$ A and 10^{-10} A for low resistance state and high resistance state respectively makes the fabricated devices suitable for low-power memristor applications. The TiO_x precursor seed layer not only promotes the uniform and preferred growth of TiO_2 nanorods on the FTO substrate but also functions as an additional source layer of trap centers due to its oxygen-deficient composition. Our data suggest that the primary conduction mechanism in these devices arises from trap-mediated space-charge-limited current (SCLC). Multilevel memory performance in this new device is achieved by varying the SET voltage. The origin of this effect is also discussed.



KEYWORDS: *resistive switching, low power, multilevel memory, TiO_2 nanorod array, space-charge-limited current, seed layer*

1. INTRODUCTION

One-dimensional (1D) nanomaterials, especially those involving semiconducting and metal oxide nanowires (nanorods), have recently gained much interest for different nanoelectronic and optoelectronic applications due to their unique physical and chemical behaviors inherently different from the parent bulk as well as thin film materials. Through careful design and controlled synthesis, nanowires will provide the building blocks for new systems of unique photonic and electronic devices.[1,2] Furthermore, the incorporation of nanowires into complex functional units via layer-by-layer assembly[3] and nanojoining[4] will enable the creation of smaller devices exhibiting novel functionality.

A new type of nanodevice, resistive switching random access memory (ReRAM) is now becoming of interest for next-generation nonvolatile memory devices due to its simple structure and promising switching speed as well as excellent scalability.[5] Such devices represent a practical application of the fourth circuit element: the memristor.[6] In comparison with thin films, the introduction of nanowires (nanorods) in ReRAM devices offers structural advantages that are expected to improve the performance of memristive devices. For example, during resistive switching operation, nanowires will facilitate the formation of straight conduction paths that enhance carrier transport.[7] This is in contrast to the branched conducting filaments that normally occur in structures based on thin films.[8] As a result, high-quality memristor performance together with good stability and reproducibility can be realized.[7] In addition, the confined structure of nanowires enable the precise engineering of the conductive paths (channels) as well as the metal/semiconductor barriers via the application of biases, leading to multilevel memory performance,[9−12] which offers much promise for high-density data storage in nonvolatile memory devices.

Many different kinds of 1D semiconductor nanomaterials were proposed for ReRAM devices, including TiO_2,[11−13] Si/a-Si core−shell nanowires,[14] ZnO,[15−18] CuO_x,[19,20] Co_3O_4,[9] WO_3,[21] NiO,[22] Ag_2S,[17] and NiO/Pt nanowire arrays.[10] Much interest has been devoted to TiO_2 which has been widely studied as a typical metal oxide material exhibiting resistive switching due to its intrinsic variety of possible crystal phases and the associated richness of switching dynamics.[23] However, compared with the widely studied TiO_2 thin film for ReRAM devices, there has been little research on 1D TiO_2 nanoma-

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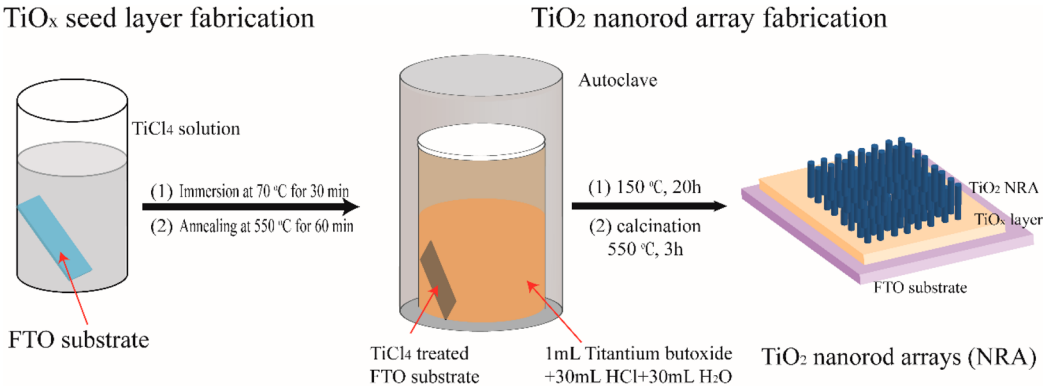

Figure 1. Schematic diagram of the fabrication process of TiO_2 NRA with seed layer.

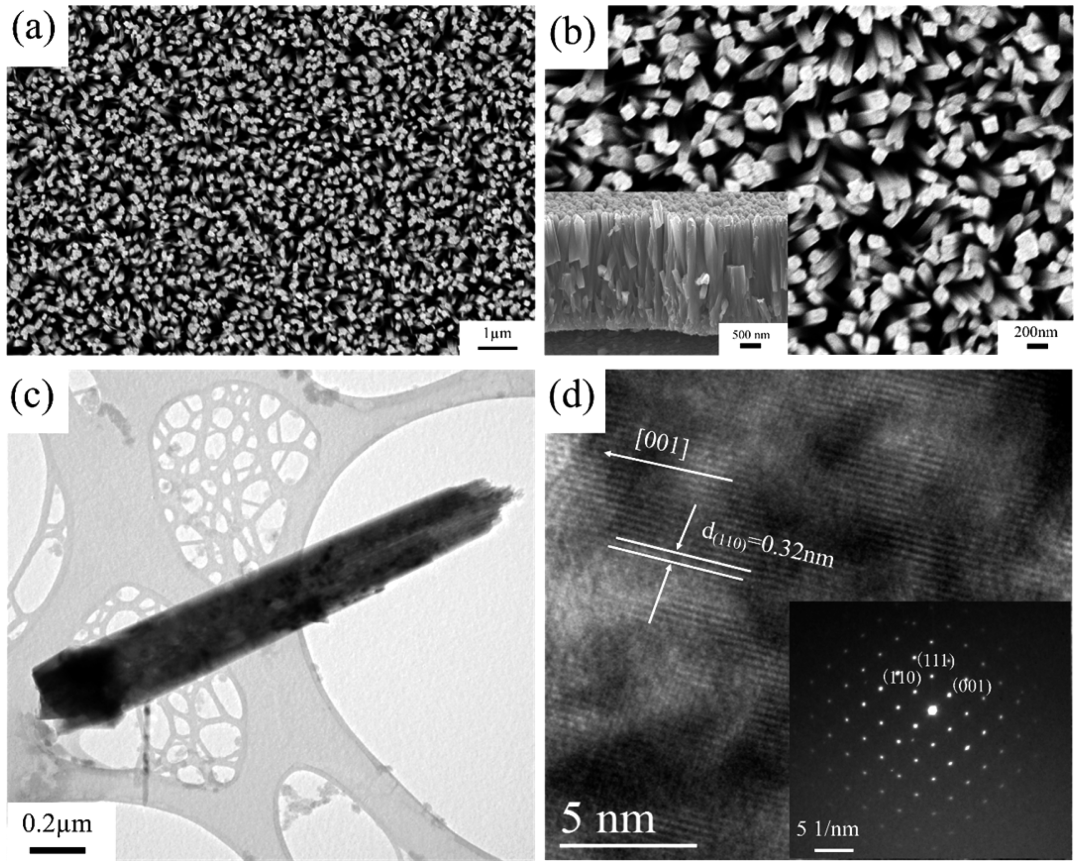

Figure 2. Morphology of TiO_2 NRAs prepared with a seed layer: (a) low magnification top-view SEM image, (b) high magnification top-view SEM image (inset: 70° tilted cross-sectional view), (c) TEM image of a single TiO_2 nanorod, (d) HRTEM image of a TiO_2 nanorod (inset: SAED pattern of the same nanorod).

terials.[11−13] It was reported that a single TiO_2 nanowire-based heterojunction can exhibit multilevel memory performance, but the realization of resistive switching required a prolonged (20 min) high voltage forming process, which is not desirable for device operation.[12] In another study, a similar Au−TiO_2 nanowire−Au heterostructure was processed with femtosecond laser irradiation to engineer the distribution of oxygen vacancies, and this resulted in improved controllable multilevel memory performance.[11] However, nanowire-based ReRAM devices from single nanowires are not economical due to the cost and complexity of the e-beam lithographic process required to fabricate the electrodes bridging the individual nanowires. Therefore, it is important to find simple cost-effective ways to obtain nanowire-based ReRAM devices which combine excellent low-current response, good uniformity and reliability, distinguishable resistance states, and potential to display multilevel memory performance as required for the next-generation nonvolatile memory devices.

The hydrothermal method to obtain well-aligned nanorod arrays (NRAs) is easier compared with costly ways to get a TiO_2 thin film (by sputtering or atomic layer deposition) as well as the individual nanowires. This commonly used method to obtain nanowires provided the possibility to control the electrical performance of the corresponding ReRAM devices via the morphology and the properties of the nanowires, such as the electrolyte of the solution, the growth period of the

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hydrothermal process, etc. Moreover, the wide suitability of hydrothermal-growth of metal oxide nanowire arrays on different substrates provided great potential for engineering the performance of obtained ReRAM devices from the interface perspective.[7,24,25] Recently, TiO_2 NRAs, grown on bare fluorine-doped tin oxide (FTO) substrates by a hydrothermal process, have been reported showing resistive switching behavior.[13] The FTO substrate provides nucleation sites for the growth of the NRAs and functions as the bottom electrode for the device. However, once again, the result showed that the realization of resistive switching behavior required a forming process and displayed high-amplitude current response.[13] The possibility that TiO_2 NRA-based ReRAM devices can be used for multilevel memory devices, and mechanisms related to this property in such devices have yet to be reported.

In this paper, we report a forming-free low-power multilevel bipolar resistive switching behavior in TiO_2 NRAs on FTO glass substrates. The key to obtaining these properties is $TiCl_4$ treatment of the FTO substrate to create an oxygen-deficient TiO_x seed layer on the substrate before the hydrothermal process. This seed layer ensures the preferential growth of a uniform, vertically oriented TiO_2 NRA structure on the substrate. The improved NRA morphology results in a significant improvement in stability, controllability of the resistive switching performance, and enabling bias-engineering of multilevel memory. We also compare the resistive switching characteristics of this new device to that of a unit formulated without the TiO_x seed layer and use this comparison to elucidate switching mechanisms in such structures.

2. EXPERIMENTAL SECTION

2.1. TiO_2 NRA Synthesis and Device Fabrication. The synthesis process of TiO_2 NRAs on a FTO glass substrate incorporating a seed layer is illustrated in Figure 1.[26−28] In the first step, the FTO substrate (40 mm × 20 mm × 2 mm, 12−15 Ω/□) after thoroughly cleaning in acetone, 2-propanol, and Milli-Q water for 15 min was immersed for 30 min in a 0.15 M $TiCl_4$ solution at 70 °C and then underwent heat treatment at 550 °C for an additional 30 min. This generated a seed layer on the surface of the FTO substrate. The seeded-FTO substrate was then placed against the wall of the Teflon-sealed autoclave containing a solution of 30 mL of H_2O, 30 mL of concentrated hydrogen chloride aqueous solution, and 1.0 mL of titanium butoxide. This was held at a temperature of 150 °C for 20 h. The resulting TiO_2 NRAs were rinsed with water, dried with nitrogen gas, and further annealed in air at 550 °C for 3 h, after which they were ready for materials characterization and device fabrication. For comparison, the same procedure was used to produce the TiO_2 NRAs on a bare FTO substrate without the initial treatment in $TiCl_4$ solution. For device fabrication, an upper Al layer with a thickness of 50−100 nm was deposited on the top surface of the TiO_2 NRAs by e-beam evaporation process with a shadow mask. The diameter of the top electrode was 1 mm.

2.2. Characterization. The morphology of the TiO_2 NRAs was examined by scanning electron microscopy (SEM, LEO-1550). Transmission electron microscopy (TEM) and high resolution transmission electron microscopy (HRTEM, JEOL 2000) operation was carried out at an acceleration voltage of 200 kV. X-ray diffraction analysis (XRD, PANalytical X'pert PRO MRD) in grazing incidence (GIXRD) mode was used for the phase and crystal structure analysis of the TiO_2 materials. Surface chemical states in the seed layer and TiO_2 NRAs were examined by X-ray photoelectron spectroscopy (XPS, Thermo- VG Scientific ESCALab 250).

Electrical characterization of the prepared devices was performed with a Keithley 2602A source-meter. The bias voltage was applied to the top Al electrode, and the FTO layer was grounded under ambient conditions.

3. RESULTS AND DISCUSSION

3.1. Materials Characterization. *3.1.1. SEM and TEM.* Figure 2a,b shows SEM images of the top of TiO_2 NRAs on a seeded FTO substrate. A well-defined and compact NRA with tetragonal crystallographic planes is observed. This is in contrast to the TiO_2 NRAs grown on bare FTO substrates, which have poor vertical orientation and intersecting nanorods (Figure S1 in Supporting Information). In photovoltaic applications, such as dye-sensitized solar cells, a seed layer would normally be introduced to prevent occasional electrical shorting due to direct contact between the redox electrolyte and FTO layer.[26,27] In this present study, we adopt this method to improve the performance of TiO_2 NRA-based ReRAM devices. By immersing the FTO substrate into a $TiCl_4$ solution, a seed layer with a thickness of ∼20 nm is typically deposited on the surface.[26] The seed layer is expected to promote the nucleation of nanorods on the FTO substrate, leading to well-defined dense NRAs with a preferred growth direction normal to the substrate.[27,29] Preferential growth normal to the surface, and the formation of well separated nanorods, should restrict electron transport to individual nanorods, minimizing cross-talk between adjacent nanorods. This, together with the formation of a continuous Al top electrode, will result in more uniform electrical performance in the fabricated ReRAM devices.

The average height of the nanorods in the TiO_2 NRA is ∼3 μm as calculated from a tilted cross-sectional view of the NRAs (inset in Figure 2b). Figure 2c shows a TEM image of an individual nanorod. The length of this nanorod has been truncated because of the preparation technique. The HRTEM and inset selected-area electron diffraction (SAED) pattern of the TiO_2 NRAs displayed in Figure 2d confirmed that the individual nanorod was single crystalline. The HRTEM image shows a (110) interplanar distance of 0.32 nm, suggesting that the preferred growth of the rutile TiO_2 nanorods occurs along the [001] crystal orientation, which is in agreement with NRAs synthesized elsewhere.[30]

3.1.2. GIXRD. Figure 3 shows typical GIXRD characterization of the seed layer and the TiO_2 NRAs with and without the seed

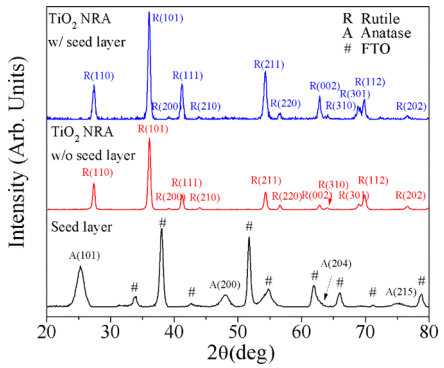

Figure 3. GIXRD characterization of the seed layer. TiO_2 NRAs prepared with and without a seed layer.

layer, respectively. It is evident that the seed layer after the annealing process is in the anatase phase (JCPDS file no. 21-1245), while the TiO_2 NRA appears as a pure tetragonal rutile phase (JCPDS file no. 21-1276) which is consistent with the HRTEM and SAED results in Figure 2d. This is in agreement with the observation of rutile TiO_2 NRA on FTO substrates typically used for solar cells.[26,27] Unlike the bare FTO substrate, the TiO_2 seed layer facilitates the epitaxial nucleation and

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growth of TiO_2 nanorods considering the decreased surface roughness of the seeded-FTO films after the treatment in $TiCl_4$ solution.[27] This leads to the enhancement of density and vertical growth of the nanorod array normal to the substrate. Furthermore, the crystallographic phase of obtained TiO_2 nanorods is not dependent on the phase of the seed layer, as researchers have demonstrated that both rutile[31] and anatase seed layers[32−34] lead to the growth of rutile nanorod arrays. The enhanced ratio of the intensities of the (002) to (101) XRD peaks in the TiO_2 NRA with a seed layer compared to the ratio of the NRA without a seed layer is suggestive of enhanced growth along the [001] direction perpendicular to the substrate.[35,36] This preferred growth direction is also in agreement with the TEM results.

3.1.3. XPS. Additional information regarding the surface states of the TiO_2 NRAs grown on the seed layer was obtained by XPS. The survey spectrum (Figure 4a) confirms the

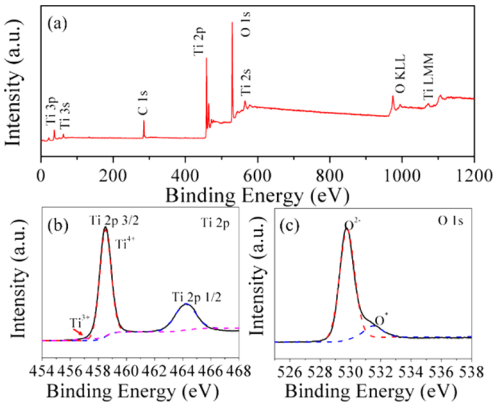

Figure 4. XPS spectra of TiO_2 NRA prepared with a seed layer: (a) survey, (b) Ti 2p, and (c) O 1s.

existence of C, Ti and O elements where the C atoms can be ascribed to a small concentration of carbon-based contaminants. High-resolution XPS spectra and their Gaussian deconvolution peak fittings of Ti 2p and O 1s are given in Figure 4b and Figure 4c, respectively. The Ti 2p peaks at 464.18 and 458.50 eV can be attributed to Ti $2p_{2/1}$ and $2p_{3/2}$, respectively. The peak separation is calculated to be ∼5.7 eV, which suggests the existence of Ti^{4+} oxidation states in the TiO_2 NRA.[37] A very weak peak centered at 457.28 eV can be attributed to Ti^{3+} states, which might originate from the reduction of Ti^{4+} by free electrons donated by oxygen vacancies.[38] The O 1s spectrum is fitted by two Gaussian peaks (Figure 4c). The peak at the lower binding energy is attributed to the Ti−O bonds while the peak at the higher binding energy is related to oxygen vacancies in the TiO_2 materials. This suggests that TiO_2 nanorods as-synthesized contain a low concentration of oxygen vacancies. These defects are expected to play an important role in the ReRAM devices fabricated from synthetic TiO_2 nanorod structures.

An analysis of surface states in the seed layer and in the TiO_2 NRA without the seed layer (Figures S2 and S3 in Supporting Information) can be used to find the proportion of individual oxygen chemical states in each component. The resulting percentages are summarized in Table 1. We find that the oxygen vacancy concentration in the TiO_2 NRA incorporating a seed layer is much smaller than that observed in the seed layer itself and the TiO_2 NRA formed without the seed layer. This

Table 1. Fractional Percentage of Oxygen (O 1s) States in Samples (%)

samples	O^{2-} (TiO_2)	O*(TiO_{2-x}, oxygen vacancies)	others (OH, etc.)
seed layer	66.45	33.55	–
TiO_2 NRA without a seed layer	77.80	21.03	1.17
TiO_2 NRA with a seed layer	89.02	10.98	–

indicates that TiO_2 NRAs grown on the seed layer are less electrically conductive. The reason for the difference in oxygen vacancies for NRAs grown with and without seed layer is under further investigation. One possible explanation is the postannealing process for reducing the concentration of oxygen vacancies in both NRAs. The NRAs prepared with the seed layer have a more compact morphology and smaller diameter (correspondingly higher surface areas), leading to a further reduction in oxygen vacancy concentration under the same annealing condition. This difference of concentration influences the initial resistance state of as-fabricated ReRAM devices (see section 3.2). As the fraction of oxygen vacancies in the seed layer exceeds 30%, this layer is highly oxygen deficient. In our discussion, the seed layer will be denoted as TiO_x where $x < 2$. It should be noted that an additional small shoulder on the O 1s state was occasionally observed in some TiO_2 NRA samples. This peak can be attributed to the presence of surface hydroxyl groups (OH) (Figures S3 in Supporting Information). The effect of residual surface OH on the resistive switching behavior is expected to be negligible because the dominating mechanism for TiO_2-based ReRAM devices is known to arise from oxygen vacancies.[39]

3.2. Electrical Characterization. *3.2.1. Resistive Switching Behavior.* Figure 5 is a record of the resistive switching behavior over 100 successive cycles in TiO_2 NRA-based ReRAM devices as prepared with and without a seed layer. Both devices display prototypical bipolar resistive switching characteristic. As shown in Figure 5a, when the voltage sweeps from 0 to +4 V in the Al/TiO_2 NRA/TiO_x layer/FTO device, the device switches from the high resistance state (HRS) to the low resistance state (LRS) and a nonvolatile "ON" state was obtained (SET process). The LRS remained after negative voltage was applied until the negative voltage is high enough to switch the device from LRS to HRS and an "OFF" state was achieved (RESET process). The resistive switching performance of the Al/TiO_2 NRA/FTO device is similar, but the polarity of the ON/OFF transition is reversed. It is important to note that the resistive switching behavior in both devices was obtained without the usual electroforming process.[13] These results are also consistent with the behavior of single ∼6 μm-long TiO_2 nanowire-based multilevel memory devices previously studied in our group, which demonstrated intrinsic forming-free resistive switching characteristics attributed to the existing oxygen vacancies in the individual nanowire.[11] This forming-free property, related to the introduction of oxygen vacancies in the switching layer, is desirable for ReRAM in the electronic industry as it simplifies operation and enables high density memory devices.[40]

To be noted, although Al was used as the top electrode, the $I-V$ performance of the present Al/TiO_2 NRA/TiO_x layer/FTO device was not the same as that of other TiO_2 thin film devices using Al as the top electrode.[16,41,42] In thin film devices, the interaction between Al and TiO_2 to form an insulating Al−

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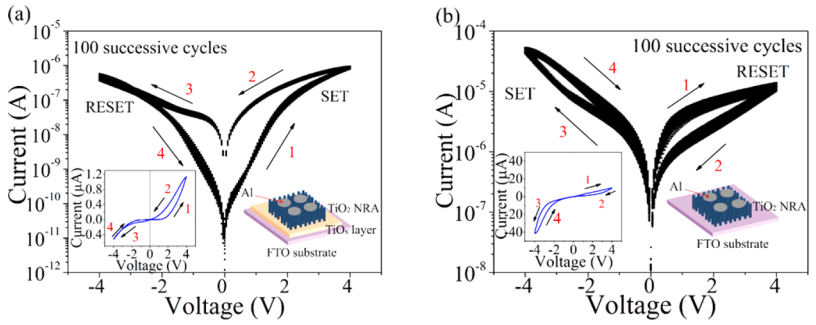

Figure 5. *I*−*V* curves of (a) Al/TiO_2 NRA/TiO_x layer/FTO device and (b) Al/TiO_2 NRA/FTO device for 100 successive cycles (for each figure, left inset: *I*−*V* curve for a typical cycle, and right inset: schematic design of the device).

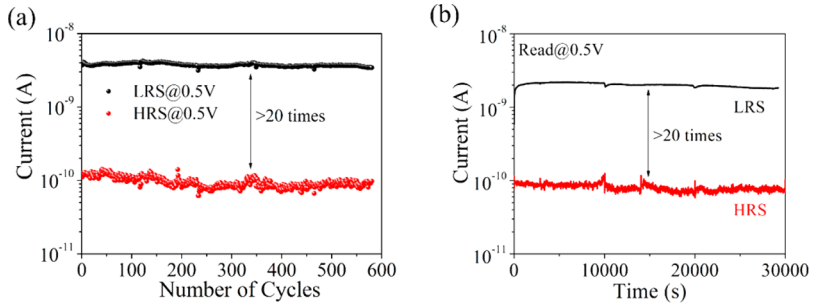

Figure 6. (a) Endurance and (b) retention performance of Al/TiO_2 NRA/TiO_x layer/FTO device.

Ti−O layer which functions as a source of oxygen ions improves the resistive switching behavior. In our fabricated Al/TiO_2 NRA/TiO_x layer/FTO device, the Al layer is expected to enhance performance compared to devices using the Pt[13] electrodes because of its oxygen affinity and ability to form an interfacial Al−Ti−O layer. However, the switching mechanism in the current devices is dominated by the TiO_2 NRAs because the thickness of the Al−Ti−O layer is likely 3−5 nm,[16] which is much less than the height of the TiO_2 NRAs (~3 μm). As a result, the resistance of an Al−Ti−O layer will be much smaller than the total resistance of the TiO_2 NRA layer. This hypothesis is confirmed by the polarity at which the device transitions from the HRS to LRS. This polarity is opposite to the negative polarity required for thin film TiO_2 devices with an Al top electrode in which the interfacial Al−Ti−O layer is expected to be crucial in determining the resistive switching behavior.[43−45] In addition, the smooth change of the *I*−*V* curves of both devices indicates that the switching mechanism in our devices is likely dominated by uniformly distributed valence states or space charge at the interface rather than the formation and rupture of filament in response to electric field.[44,46]

Other differences are also apparent in the properties of devices prepared with and without the TiO_x seed layer. For example, the current amplitude in the Al/TiO_2 NRA/TiO_x layer/FTO device is approximately 1 order of magnitude less than that of the device prepared without a seed layer, indicating that the Al/TiO_2 NRA/TiO_x layer/FTO device is more insulating. This suggests that the higher concentration of oxygen vacancies observed in the TiO_2 NRAs in the absence of a seed layer makes the device more electrically conductive. Due to the large difference between the thickness of the seed layer (~20 nm) and the height of the nanorods, the resistance of the seed layer is small compared to that of the NRAs and the electrical performance can then be dominantly ascribed to the TiO_2 NRAs. Variations in the concentration of oxygen vacancies in the nanorods in the two types of device may also be responsible for differences between the initial states in resistive switching operations, in which the fabricated Al/TiO_2 NRA/TiO_x layer/FTO device starts from the HRS under sweeping operations, while the initial condition for Al/TiO_2 NRA/FTO devices is the LRS. This behavior is indicated by the arrows in Figure 5.

I−*V* curves under cyclic voltage sweeping show that the bipolar resistive switching response in Al/TiO_2 NRA/TiO_x layer/FTO devices is more stable and repeatable while maintaining a relatively high ON/OFF ratio (>20). Stable electrical performance can be associated with the compact, fine surface morphology of the TiO_2 NRAs grown on the seed layer. TiO_2 nanorods constrain current flow along their longitudinal axis due to their small cross section. This leads to the formation of direct conduction paths for electrons and the minimization of interactions between channels in adjacent nanorods. Such structures also facilitate the deposition of compact Al electrodes. To illustrate this point, the resistive switching behavior of Al/TiO_2 NRA/FTO devices is characterized by high fluctuation and a small ON/OFF ratio (Figure S4 in Supporting Information). Both of these properties are not desirable for industrial applications of ReRAM devices in the electronic industry.[40] It is important to note that the higher cell uniformity in these Al/TiO_2 NRA/TiO_x layer/FTO devices with distinguishable resistance states ensure that they are promising as a candidate for nonvolatile ReRAM devices (Figure S5 in Supporting Information). From the above analysis, it can be concluded that the introduction of a TiO_x seed layer can significantly improve the resistive switching performance of the TiO_2 NRA-based ReRAM devices.

3.2.2. Endurance and Retention Study. The endurance performance of the fabricated Al/TiO_2 NRA/TiO_x layer/FTO device is given in Figure 6a by direct-current cyclic sweeping

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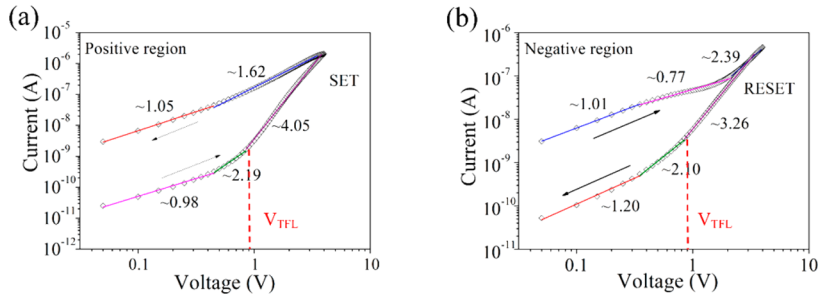

Figure 7. Log–log I–V response for the Al/TiO_2 NRA/TiO_x layer/FTO device: (a) Positive region and (b) negative region.

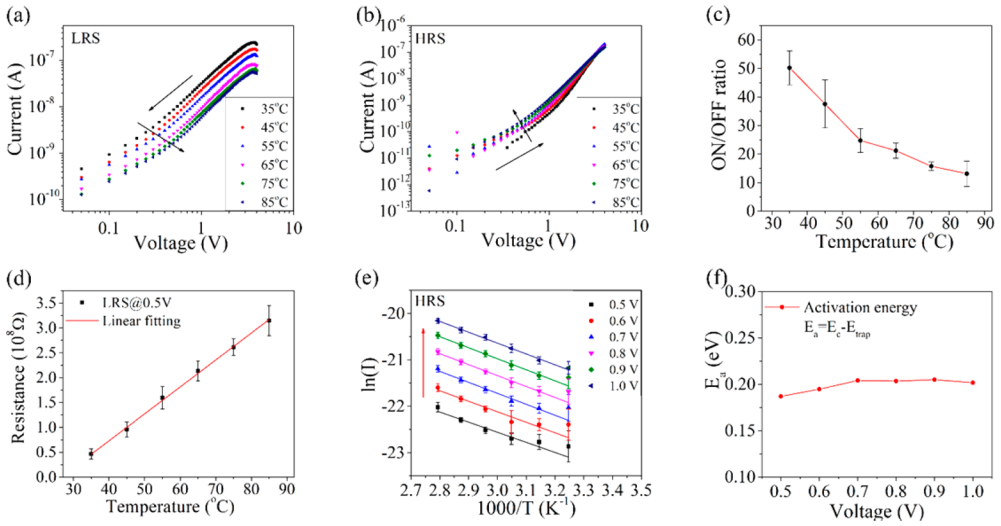

Figure 8. Log–log I–V curves of (a) LRS and (b) HRS at different temperatures, (c) ON/OFF ratio vs temperature, (d) linear fit for LRS resistance, (e) ln(I) vs 1000/T and corresponding fits at specific read voltages, and (f) activation energy $\Delta E = E_c - E_{trap}$ calculated from the slopes in part e plotted as a function of V. The standard deviations for parts c, d, and e are from the statistical average of 15 repeatable cycles. All measurements were carried out under ambient atmospheric conditions.

operations. We find that this new device maintains a high stable ON/OFF ratio (>20) over at least 500 cycles. This ratio is sufficient to distinguish different states in potential ReRAM devices. The cumulative probability curve of both LRS and HRS resistances illustrated that the distribution of LRS and HRS resistances is in the range of 1.3×10^8 Ω and ~5.3×10^9 Ω, respectively, with very good cycle-to-cycle uniformity as demonstrated by the cumulative probability curve (Figure S6 in Supporting Information). The coefficient of variations for LRS and HRS resistances (defined as the standard deviation of the measured resistance divided by the mean values) for more than 500 cycles are 0.04 and 0.15, respectively, suggesting promising stable resistive switching performance. It is also apparent that the low current amplitude (<10^{-8} and 10^{-10} A for LRS and HRS read at 0.5 V, respectively) during resistive switching is very promising with respect to low operating power and heat generation requirements for emerging applications of memristor devices such as logic and neuromorphic devices.[47,48] Furthermore, data retention of the Al/TiO_2 NRA/TiO_x layer/FTO device was studied by probing the current changes in the OFF and ON state for a long period of time. As seen in Figure 6b, a well-defined ON/OFF ratio, showing only limited fluctuations, was obtained in the device for more than 3×10^4 s. Robust endurance and low operating power together with long retention time is indicative of the high reliability and nonvolatile nature of these fabricated Al/TiO_2 NRA/TiO_x layer/FTO devices.

3.2.3. Switching Mechanism Study. The conduction mechanism in the Al/TiO_2 NRA/TiO_x layer/FTO device can be obtained from an analysis of the I–V characteristic curves shown on a log–log scale in Figure 7. Under positive bias, the Schottky barrier at the FTO/TiO_x interface limits the electron transport and the device is initially in the HRS, given the difference between the work function of the FTO substrate (4.7 eV) and the ideal Fermi level of TiO_2 (4.2 eV).[49] The I–V characteristic for the HRS consists of three different regions, the Ohmic region ($I \propto V$) which is dominated by thermally generated free carriers, the Child's law region ($I \propto V^2$), where traps are being filled by electrons, and the trap-filled-limit region including a threshold voltage (V_{TFL}) and steep current rise. The V_{TFL} in our device is ~1 V, which corresponds to the voltage at which all traps are filled by electrons, after which the electrons flow through the conduction band, switching the device from HRS to LRS. This behavior can be easily understood from the trap-controlled space-charge-limited current (SCLC) mechanism, in which the oxygen vacancies serve as electron traps that would form/rupture electron transport channels.[50] Oxygen vacancies are present in the individual nanorods as well as in the TiO_x seed layer due to its high oxygen deficiency. As the voltage sweeps from +4 to 0 V, the I–V curve first has a slope of ~1.62 as the traps remain filled. A slope of 1.62 instead of 2, as expected for a space-charge-limited current, can be attributed to trapping in the interfacial layer formed in the vicinity of the Al electrode during

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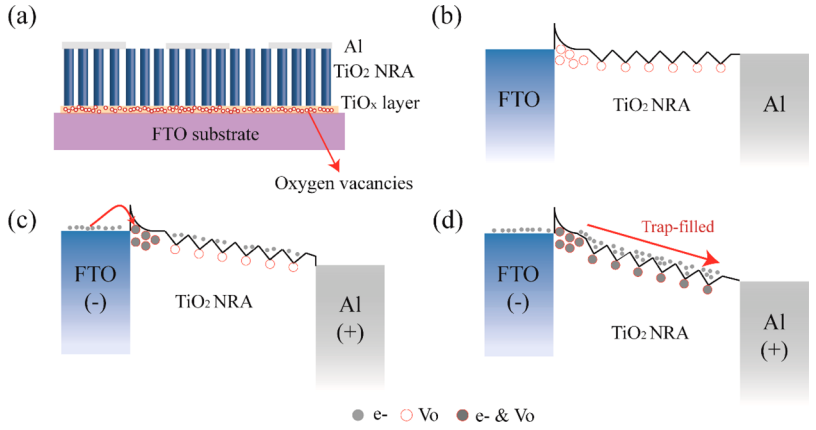

Figure 9. Schematic representation of the switching mechanism in the fabricated Al/TiO_2 NRA/TiO_x layer/FTO device, (a) cross-sectional design, (b) pristine state, (c) positive bias, 0 → V_{TFL}, traps are partially filled, (d) positive bias, V_{TFL} → 4 V → 0 V, traps are fully filled, the device has transitioned from HRS to LRS.

the metal deposition process.[51] Migration of oxygen vacancies in the nanorods as well as in the TiO_x seed layer would also play a role in the deviation of slopes.[42,52] When the voltage approaches zero, the slope decreases to ∼1, as the injection of carriers is reduced and ohmic conduction dominates.

During the RESET process (Figure 7b), the Al electrode is negatively biased, and electrons start to be injected from this layer toward the bottom FTO electrode. The slope of the $I-V$ curve is ∼1.0 when the bias voltage is less than −0.4 V. As the voltage becomes more negative, the slope initially decreases before increasing to >2.0. This suggests that the traps associated with oxygen vacancies remain filled. As the voltage sweeps from −4 V to 0 V, the slope of the curve first decreases from ∼3 to ∼2 as the voltage approaches −0.4 V. The slope then becomes ∼1 at lower negative voltage down to 0 V, indicating that the current arises from free carriers. This behavior suggests that electrons are released from all of the traps at ∼−0.4 V and the device retransitions from the LRS to HRS.

Further understanding of the conduction mechanism in fabricated Al/TiO_2 NRA/TiO_x layer/FTO devices can be obtained by the $I-V$ response at different temperatures (Figure 8a and 8b). The resulting temperature-dependent ON/OFF ratio is shown in Figure 8c. It can be seen that the LRS resistance decreases as the temperature decreases. In addition, the LRS resistance at a 0.5 V read voltage increases linearly with temperature, as shown in Figure 8d. This indicates an ohmic behavior under LRS as evidenced by a slope of ∼1 under low read voltages in Figure 7a. In contrast, the current response in the HRS at different temperatures is more complicated (Figure 8b). The HRS current is controlled with the SCLC mechanism over a range of temperature,[53] as illustrated in Figure 8b. To identify the physical mechanism, the Child's Law current response at different temperatures is plotted as $\ln(I)$ vs $1000/T$ in Figure 8e. On the basis of the SCLC theory, the current in the Child's Law region can be expressed as

$$I = \frac{9}{8} A\varepsilon\mu\theta \frac{V_a^2}{d^3} \quad (1)$$

$$\theta = \frac{N_c}{N_t} \exp\left[\frac{-(E_c - E_{trap})}{KT}\right] \quad (2)$$

This solution is based on the assumption that the electrons traps (oxygen vacancies in our case) are restricted to a single discrete energy level (E_{trap}). In the equations, A is the effective area for the conduction channels, μ is the mobility, and ε and d are the permittivity and thickness of the oxide layer, respectively. Furthermore, V_a is the applied voltage, E_c is the energy at the conduction band minima, N_c is the effective density of states in the conduction band at temperature T, N_t is the total trap density, and K is Boltzmann's constant.

From eq 1 and eq 2, the current response $\ln(I)$ in this region is a linear function of $1/T$, with a slope $-(E_c - E_{trap})/1000T$. Arrhenius plots of measured data at different read voltages are given in Figure 8e. The activation energy calculated from these data at different read voltages is $\Delta E = E_c - E_{trap} = 0.18-0.20$ eV (Figure 8f). Thus, energy levels associated with these traps are more shallow than trap levels arising from oxygen vacancies in bulk TiO_2, which are theoretically calculated to lie 0.8−1.0 eV below the conduction band.[53−55] This difference in trap levels might be attributed to the proximity of the surface in the high surface-to-volume ratio of nanorods and the role of the surface in reducing the energy for vacancy formation. Furthermore, the diffusion of defects from inside the nanorod to the surface will also increase the surface defect density.[56] Similar reports about the ZnO nanowire arrays showed much higher photocurrent response compared with the thin film under the same thickness condition, mainly due to the increasing of self-induced surface defects.[57] The overall effect is that the trap states of the oxygen vacancies are expected to be more shallow below the conduction band, compared to those in TiO_2 thin films. Research about the relationship between the surface defects of nanorods and the corresponding resistive switching performance is ongoing.

A tentative model of the switching mechanism for an Al/TiO_2 NRA/TiO_x layer/FTO device is schematically illustrated in Figure 9. In its pristine state, the device possesses a limited concentration of oxygen vacancies at the FTO/TiO_x interface as well as in the NRAs (Figure 9b). These oxygen vacancies yield a series of electron traps as shown below the TiO_2 conduction band. The traps are gradually filled with electrons when a forward bias is applied to the Al electrode. Figure 9c corresponds to the forward region below the V_{TFL}. After all of these traps are filled, the current abruptly increases as the device transitions from HRS to LRS (Figure 9d).[58] Significant detrapping of these oxygen vacancies occurs when a high

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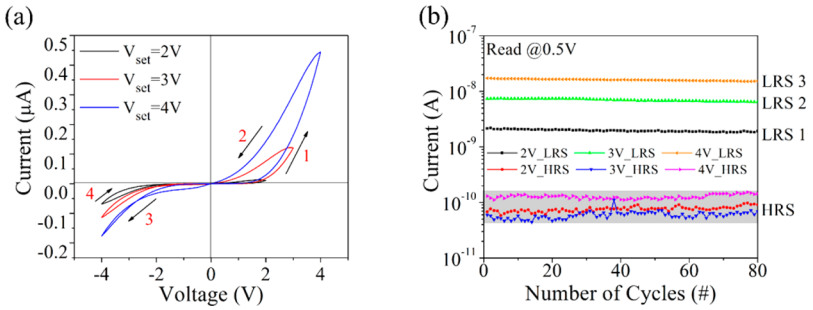

Figure 10. (a) $I-V$ curve for Al/TiO_2 NRA/TiO_x layer/FTO device under different SET voltages and (b) demonstration of four-level memory performance under cyclic voltage sweeping.

negative voltage is applied on the top Al electrode, which would switch the device back from LRS to HRS.

3.2.4. Multilevel Memory Behavior. The potential for obtaining multilevel memory in the TiO_2 NRA-based device was studied by applying different SET voltages while keeping the RESET voltage at −4 V. Figure 10 shows well-defined differences in LRS current under cyclic sweeping operations, such that a four-level memory may be feasible while maintaining a nearly constant HRS current (read @0.5 V). The four-level memory performance was measured to be stable for 80 cycles, and the measurements indicate that this behavior can be extended to more cycles given the very small variation in current in each level (Figure 10b). We also find that a six-level memory can be achievable using SET voltages of 5 and 6 V, even though the current response for higher voltage is not as distinguishable as for lower SET voltages (Figure S7 in Supporting Information). Furthermore, the current response of LRS for each level is still below 10^{-7} A under different SET voltages, suggesting significant potentials for low-power ReRAM devices. Overall, this indicates that the TiO_2 NRAs grown on a seed layer are very promising in multilevel memory devices. The multilevel memory performance for the Al/TiO2 NRA/FTO device is not achievable due to its poor reliability.

Though some metal oxide nanomaterials exhibit multilevel memory performance, the origin of multilevel memory is still controversial. It has been suggested that multilevel memory can be obtained by engineering of the size of conductive filaments (more generally, conduction paths) as determined by the accumulation of ions or defects controlled by the compliance current,[59,60] maximum voltages,[61] and a series of applied voltages.[11] Different ionic charge traps or intermediate energy states below the valence band within the oxide layer have also been suggested.[62] Modification of the effective barrier height and narrowing of the depletion layer have also been proposed to engineer a range of ON/OFF ratios[39] or different levels of current amplification.[12] In the current work, the origin of the multilevel memory performance in the fabricated devices has been studied by examining the $I-V$ characteristics at different SET voltages on a log−log scale (Figure S8 in Supporting Information). This shows that the switching mechanism in the devices under all five SET voltages arises from SCLC.[63] Changes in the slope of the current for $V > V_{TFL}$ with SET voltage are also described via SCLC theory (Figure S9 in Supporting Information).[38] It can then be concluded that the accumulation of oxygen vacancies and size engineering of conductive paths or filaments can be excluded as the origin of a multilevel memory in the present device. For $V > V_{TFL}$, all available traps would have been filled and the injection carriers are mainly contributed by the increase in free electrons. Because higher applied voltages (V_a) would result in a larger amount of free electrons, higher LRS current at the same low read voltages could be expected considering that the slopes for the LRS current response are approximately the same under different SET voltages. This could be the reason for the multilevel memory performance in our devices. Further studies on the dependence of $I-V$ characteristic on pad size, and the effects of the height of the TiO_2 nanorod array on the multilevel memory response are being examined to clarify the switching mechanism in these Al/TiO_2 NRA/TiO_x layer/FTO devices.

4. CONCLUSIONS

We have demonstrated the improved resistive switching performance in the devices based on TiO_2 NRAs on a FTO substrate by the introduction of a seed layer. The TiO_x seed layer on the surface of the FTO substrate enhances the vertical growth of TiO_2 NRAs normal to the substrate, leading to compact and fine nanorod morphology. Meanwhile, the concentration of oxygen vacancies of obtained NRAs is lower compared with NRAs prepared without the seed layer. The obtained Al/TiO_2 NRA/TiO_x layer/FTO devices exhibit a stable forming-free bipolar resistive switching behavior and maintain a higher ON/OFF ratio with lower switching currents under voltage sweeping over 500 cycles. The retention period is found to exceed 3×10^4 s. Switching in as-fabricated devices is controlled by a trap-mediated SCLC mechanism in which the existing oxygen vacancies in nanorods as well as in the seed layer function as trap centers. We also find that a multilevel memory feature of the device, each dominated by SCLC current flow, is obtained in response to variations in the SET voltage. Such intrinsic nonvolatile multilevel resistive switching properties and low power operation, combined with robust endurance and retention, make Al/TiO_2 NRA/TiO_x layer/FTO devices promising candidates for future nonvolatile ReRAM devices.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.6b14206.

SEM images of TiO_2 NRAs prepared without a seed layer, XPS spectra of TiO_x seed layer and TiO_2 NRAs prepared without a seed layer, endurance study of Al/TiO_2 NRA/FTO device under voltage sweeping, cell-uniformity result of both Al/TiO_2 NRA/TiO_x layer/FTO and Al/TiO_2 NRA/FTO device, cumulative probability curve for LRS and HRS resistances of Al/TiO_2 NRA/

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TiO_x layer/FTO device, $I-V$ curves of Al/TiO_2 NRA/TiO_x layer/FTO device at different SET voltages and demonstration of six-level memory response in cyclic voltage sweeping, log−log $I-V$ curves for Al/TiO_2 NRA/TiO_x layer/FTO device at different SET voltages, slope of $I-V$ curve of Al/TiO_2 NRA/TiO_x layer/FTO devices in the region with $V > V_{TFL}$ for different SET voltages (PDF)

AUTHOR INFORMATION

Corresponding Author

*E-mail: nzhou@uwaterloo.ca.

ORCID

Ming Xiao: 0000-0003-2018-4807

Notes

The authors declare no competing financial interest.

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