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The mechanism of pore segregation in the sintered nano Ag for high temperature power electronics applications

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ABSTRACT

It is widely accepted that nano pores of sintered nanoparticles can coalesce into micro pores during high temperature service. When applying sintered nanoparticles in power electronics, the pore segregation and delamination seriously degrade the bond strength and thermal conductivity, but the reason is still not well understood. In this paper, both finite element analysis and experimental results confirmed that thermal stress is the main driving force for this phenomenon, which was not considered in the previous study. The effect of pore segregation on performance and reliability of power devices is also discussed.
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1. Introduction

Nowadays, power electronics are widely used in many field such as electric vehicle, aircraft, and energy industry [1]. The wide band gap semiconductors, such as SiC, have been developed for high temperature (>300 °C) applications [2]. However, traditional lead free die attach materials are not suitable due to the low melting point (Sn based solder) or the high price (Au based solder) [3]. In recent decades, nano Ag sintering technology emerged as a promising candidate for the power electronics packaging due to its low process temperature and high operating temperature [1,4]. However, the unstable nature of nanoporous structure of sintered Ag brings some uncertain factors for its high temperature reliability [5,6]. Many researchers observed this pore segregation and delamination phenomenon but the reason is not understood [7,8].

In this paper, the reliability of sintered Ag at harsh environment of 350 °C was evaluated. The pore segregation and delamination in the bondline, where nano/micro pores coalesce and aggregate close to SiC chips, creating a continuous growing layer near substrates, is observed and the mechanism was analyzed by both experiments and finite element analysis (FEA). Its effect on performance and reliability of power devices is also discussed.

2. Experiment

The nano Ag paste was manufactured with hybrid nano Ag particles of two average diameters (80 nm and 800 nm). The SiC diode chips (1.85 × 1.85 mm^2, Ti/Ni/Ag metallization) were sintered with the nano Ag paste on direct bond copper (DBC) substrates (Ni/Au metallization). Sintered samples were divided into 5 groups, 1 group for comparison and the others for high temperature storage (HTS) at 350 °C for 200 h, 400 h, 800 h, and 1200 h, respectively.

The samples were cut and polished with the ion beam by Leica EM TIC 3X to keep the details of porous structure. The porosity was observed with SEM.

3. Results and discussion

The pore evolution of this study is shown in Fig. 1 and can be divided into 3 stages. During the initial stage, the sintering process form interconnected pores with arbitrary shapes in average diameter of 1–2 μm (Fig. 1a). In the second stage (<400 h HTS), the interconnected pores are shrinking and closing off, resulting the decreasing total porosity in Fig. 1f. Further storage in the final stage (≥400 h HTS) finds some large pores (diameter ≥ 10 μm) grow up at the expense of small pores (<1 μm), resulting the increasing total porosity in Fig. 1f. A similar result was reported in [6].

A pore segregation and delamination phenomenon simultaneously occurred with pore coalescence, especially when the storage time was beyond 800 h. The porosity near SiC chips increased while it decreased near DBC substrates. Fig. 1f clearly shows the

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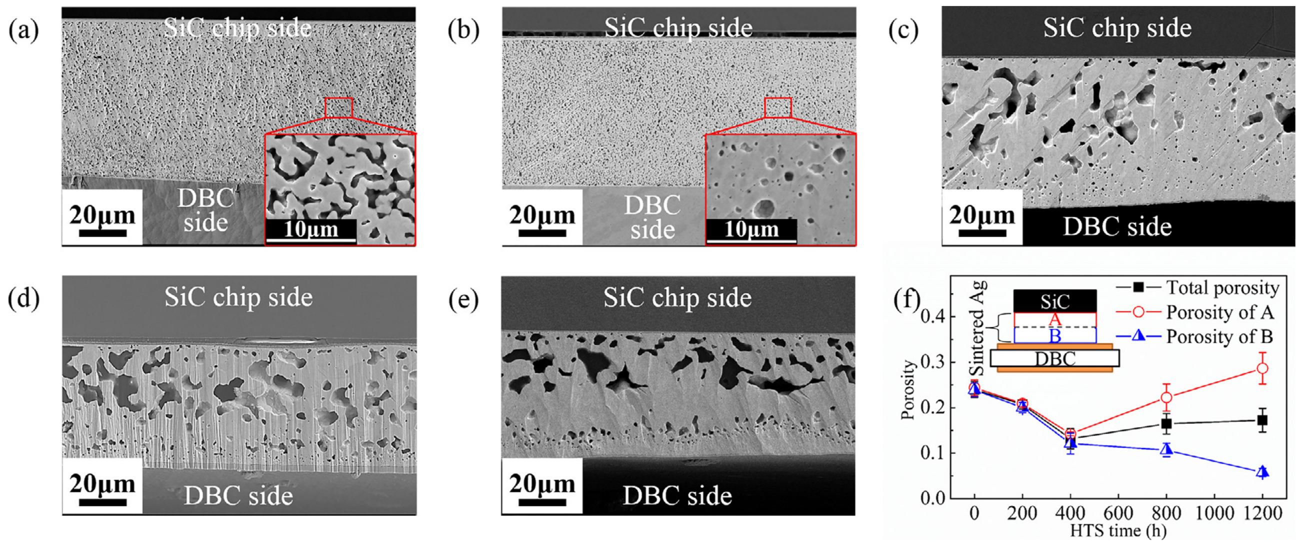

Fig. 1. Evolution of porous microstructure: (a) as-sintered; after HTS at 350 °C for (b) 200 h, (c) 400 h, (d) 800 h, (e) 1200 h, (f) porosity vs storage time. The porosity comparison of upper (A) and lower (B) parts reveals the pore segregation.

largely different porosities between the upper (SiC) and lower (DBC) parts in sintered Ag. Similar pore segregation phenomenon was also observed on DBC substrates with Au surface and Pd surface after a long-term HTS in [9], indicating that this phenomenon is not the effect of surface metallization.

The evolution of porous structure is driven by the principle of minimum energy, which drives the material transporting during sintering and HTS [7]. The difference in vacancy concentration causes a flux of vacancies, which equals to flux of atoms in the opposite direction. The equilibrium vacancy concentration is [7,8]

$$c_v = c_0 exp\left(\frac{\sigma\Omega}{kT}\right) \approx c_0\left(1 + \frac{\sigma\Omega}{kT}\right) \quad (1)$$

where c_v is the equilibrium vacancy concentration, k is Boltzmann constant, T is thermodynamic temperature, σ is the stress (define tensile stress is positive while compressive stress is negative), Ω is the vacancy volume, and c_0 is the unstressed vacancy concentration. The equation indicates the vacancy flux is proportional to the stress gradient. Thus, the positive surface tension stress gradient from the convex necks to the neighbor parts results the growth of necks and shrinkage of pores, while the positive stress gradient from small pores to the large pores results the pore coalescence effect [7,8].

The mismatch of thermal expansions among different materials in the sandwich package structure can also introduce a thermal stress gradient, which is believed to be the main driven force of the pore segregation phenomenon. FEA is employed to analyze the thermal stress distribution in sintered Ag, a characteristic assembly with SiC chip on DBC substrate is modeled as presented in Fig. 2a. The sintered Ag is elastic-plastic and the other materials are elastic as presented in Table 1 [10–12]. Metallization layers are ignored due to their thin thickness (<2μm).

Fig. 2b shows the symmetric Von Mises stress distribution in the sintered Ag layer, thus it is sufficient to analyze stress distribution in one cross section as shown in Fig. 2c. The negative principal stress in Fig. 2d (P3) indicates the compressive state of sintered Ag, therefore the vacancy concentration gradient is inversely proportional to the Von Mises stress gradient. As the pores mainly segregate in the thickness direction (z-axis), the stress distributions along z-axis of P1 ~ P4 are compared in Fig. 2e (min principal stress) and f (Von Mises stress). Therefore the vacancy concentration of the Ag bondline decreases along the direction from DBC to SiC chip and according to equation (1), there is a vacancy flux away from DBC side towards SiC chip side, driving the pores to segregate close to the interface with SiC chip.

In order to verify and confirm the relation between pore segregation and thermal stress gradient, bulk Ag chip instead of SiC chip were bonded and stored at 350 °C for 400 h and 1200 h, respectively. The microstructure evolution in Fig. 3a–d indicates no pore segregation in those samples. Comparing the stress distribution in Fig. 3e with Fig. 2b, the max principle stress of bondline with bulk Ag chip (61 MPa) is only 1/3 of that with SiC chip (188 MPa). The Von Mises stress gradient in the sintered Ag bondline is obviously smaller (<1/2) when the SiC chip (Fig. 2f) is replaced by bulk Ag chip (Fig. 3f), thus no pore segregation can be observed. The data in the literature also support this theory. For a thick bondline (126 μm), the pore segregation did not happen after 1000 h storage at 250 °C [13]. But for a thin bondline (26 μm), it happened just after 500 h storage at 300 °C [14].

According to this theory, it can be deduced that the densification of the Ag bondline layer can facilitate the aggregation process. The elastic modulus of sintered Ag bondline increases with the decreasing of porosity during HTS, leading to a higher stress gradient. Meanwhile, the annealing can reduce stress due to recrystallization. The two effects are competing during the HTS, but the thermal stress gradient direction remains the same. Therefore, the direction of pore segregation does not change due to the CTE mismatch between SiC chip and DBC substrate, leading to the pore segregation phenomenon after a long-term HTS.

Miranda [15] measured the thermal conductivity of sintered Ag and found that the reduced porosity were effective in increasing the thermal conductivity. However, the pore segregation will dramatically decrease the thermal conductivity even the total porosity remains the same. Moreover, the region with high porosity has smaller loading area, reducing the effective mechanical property of the total sintered Ag layer. Therefore, for power electronic package, the pore segregation lowers its reliability and should be prevented in high temperature application. A possible solution may be compositing the sintered Ag with SiC nanoparticles which is effective in lower the total CTE [11] and stabilizing the evolution of pores [16].

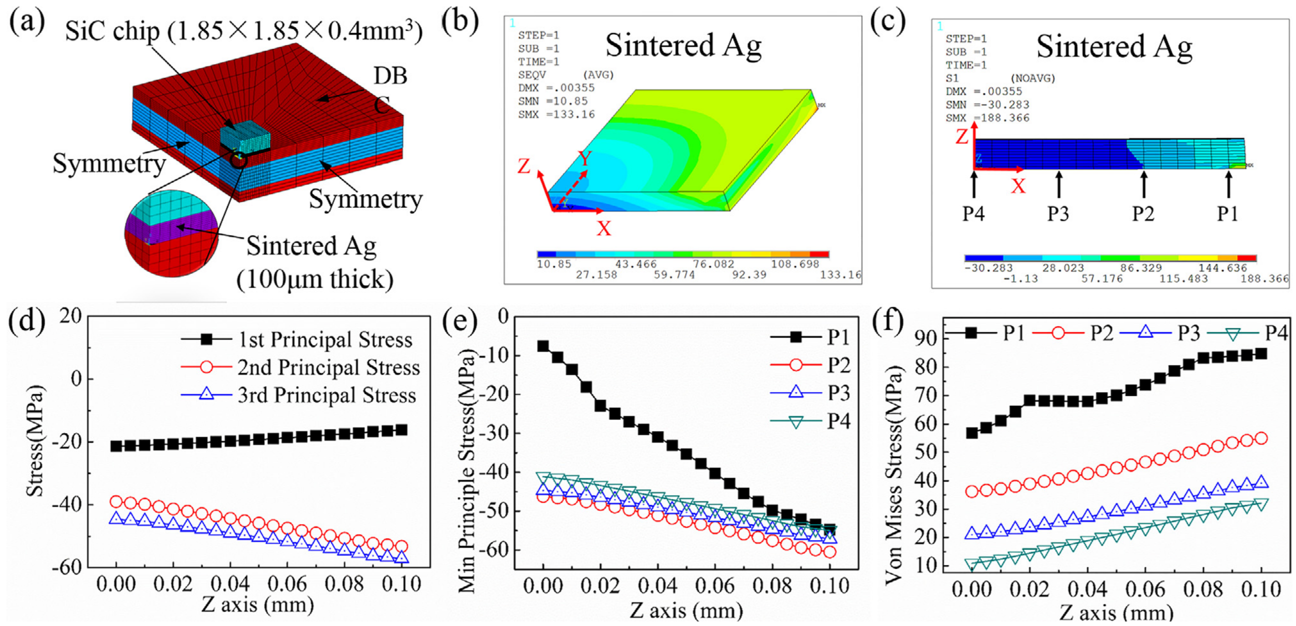

Fig. 2. (a) Double symmetric FE model of SiC chip sintered on DBC. (b) symmetric distribution of Von Mises stress in sintered Ag (SiC chip and DBC are hidden), (c) max principal stress in cross section of sintred Ag. (d) stress distribution along z-axis of P3 (P1 ~ P4 have similar distribution). (e) min principal stress distribution and (f) Von Mises stress distribution along z-axis of P1 ~ P4, indicating the vacancy flux from z = 0 (DBC) towards z = 0.1 (SiC chip).

Table 1
Material property for FEA [11–14]

Material	CTE, 10^{-6}/K	Elastic modulus, GPa	Poisson's ratio	Yield strength, MPa	Density, g/cm^3
Sintered Ag	19	40*	0.38	80*	8.92
SiC	4.1	446	0.17	–	3.16
Cu	16.5	120	0.34	–	8.96
Al_2O_3	7.7	390	0.24	–	3.6

* Mechanical property of the sintered Ag (15% porosity) after 400 h HTS is based on[10].

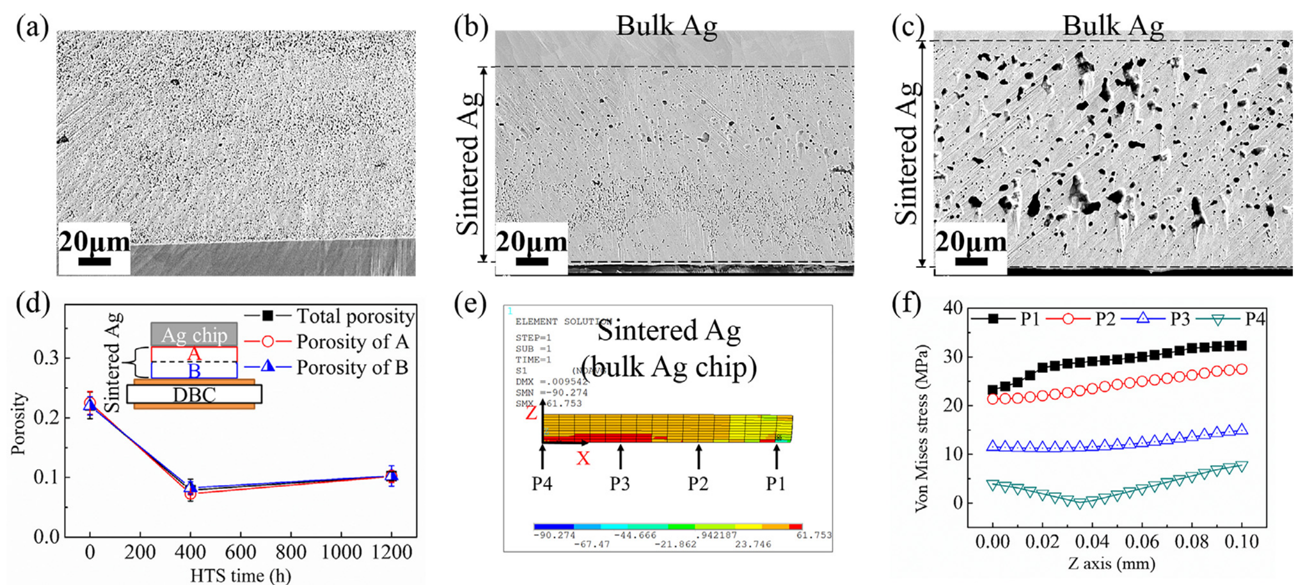

Fig. 3. Microstructure of sintered Ag with bulk Ag chips: (a) as-sintered; after 350 °C HTS for (b) 400 h, (c) 1200 h, (d) porosity vs storage time. (e) max principal stress in the cross section of sintred Ag with bulk Ag chip, (f) Von Mises stress distribution along z-axis of P1 ~ P4.

4. Conclusion

A pore segregation phenomenon was observed after the long-term (≥800 h) HTS. The vacancy concentration gradient induced by the thermal stress gradient is the main reason for the pore segregation, which is verified and confirmed by both FEA and experimental results. The pore segregation can dramatically degrade the property and reliability of the power device, and further works are required to prevent this phenomenon.

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