Course Outline

Integrated Digital Electronics (3C,1T,1.5L)

ECE 445 - Spring 2011

Instructor
Dr. Vincent Gaudet

Course Description:

Digital CMOS integrated circuits are enabling today's high-performance electronic systems, e.g. personal electronic devices, computer servers, as well as high-speed and portable wireless communications. Currently, several billion transistors can be integrated into a single CMOS chip, and this number is expected to continue to increase over coming years as CMOS technologies shrink and transistor performance improves.

This course will cover transistor and circuit-level aspects of digital integrated circuit design. Major topics will include: (a) logic gate design at the transistor level, including how to translate a Boolean logic function into a transistor-level circuit, transistor sizing, and characterization of gate delays, (b) design and optimization of sequential systems, (c) arithmetic circuits and delay optimization, and (d) physical design of integrated circuits, i.e. how to translate your transistor-level designs into "blueprints" that can be used by fabrication engineers to build your design. The laboratory component of the course will use an industrial-grade CAD tool (Cadence) for schematic entry and simulation of your circuits, and for physical design, and will culminate in a group design project.

By the end of the course you will have a thorough understanding of how to design digital circuits at the transistor level, where delays in digital circuits come from and how to minimize them, where power is consumed in digital circuits and how to characterize it, and how circuit designs are mapped onto integrated circuit layouts ready for fabrication. Although analog and mixed-signal circuits are not part of this course, many of the design techniques you will learn in this course are also relevant to those areas.

Prerequisites: ECE 231/331; Level at least 4A Computer Engineering or Electrical Engineering.

Tutorial Description: Question and answer on material covered in lectures, quizzes (2), specific help with problems from the textbook, background material for labs, and problem-solving skills.

Project Description: A group integrated circuit design project is an essential component of this course. The project involves transistor-level (<20 transistors) digital circuit design, simulation, and layout.

Computer Experience: Integrated circuit design software tools (Cadence: schematic entry, simulation, layout, DRC, LVS)
The course will cover the following topics:
- Review of the MOS transistor and logic design (3 hours)
- CMOS inverter characterization (5 hours)
  - Inverter circuit
  - DC transfer characteristic
  - Propagation delay, rise and fall time
  - Transistor sizing
- CMOS combinational circuits (6 hours)
  - Circuits
  - Transistor sizing
  - Characterizing delay in combinational circuits
- CMOS sequential circuits (6 hours)
  - Sequencing methods
  - Circuits for latches and flip-flops
- CMOS arithmetic circuits (8 hours)
  - Optimizing delay in combinational circuits
  - Adder and subtractor circuits
  - Specialized arithmetic circuits
  - Power consumption in digital circuits
  - Physical design of digital circuits
- Interconnect parasitics (4 hours)
- Timing issues in digital circuits (4 hours)

**Use of Calculators in Examinations**
Programmable and/or scientific calculators without formula storage nor text display features may be used during examinations. Personal computers may not be used in examinations.

**Grading**

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Labs</td>
<td>25%</td>
</tr>
<tr>
<td>Quizzes (2)</td>
<td>10%</td>
</tr>
<tr>
<td>Midterm</td>
<td>15%</td>
</tr>
<tr>
<td>Final Examination</td>
<td>50%</td>
</tr>
</tbody>
</table>

**Textbook**

**Required materials:**
- Instructor’s Course Notes (to be distributed during the term)

**Recommended books:**