ECE 445 Integrated Digital Electronics- Spring 2021

Instructor

Prof. Lan Wei

COURSE DESCRIPTION:

Digital CMOS integrated circuits are enabling today's high-performance electronic systems, e.g. personal electronic devices, compute servers, as well as high-speed and portable wireless communications. Currently, several billion transistors can be integrated into a single CMOS chip, and this number is expected to continue to increase over coming years as CMOS technologies shrink and transistor performance improves.

This course will cover transistor and circuit-level aspects of digital integrated circuit design. Major topics will include: (a) logic gate design at the transistor level, including how to translate a Boolean logic function into a transistor-level circuit, transistor sizing, and characterization of gate delays, (b) design and optimization of sequential systems, (c) arithmetic circuits and delay optimization, and (d) physical design of integrated circuits, i.e. how to translate your transistor- level designs into "blueprints" that can be used by fabrication engineers to build your design. The laboratory component of the course will use an industrial-grade CAD tool (Cadence) for schematic entry and simulation of your circuits, and for physical design, and will culminate in a group design project.

By the end of the course you will have a thorough understanding of how to design digital circuits at the transistor level, where delays in digital circuits come from and how to minimize them, where power is consumed in digital circuits and how to characterize it, and how circuit designs are mapped onto integrated circuit layouts ready for fabrication. Although analog and mixed- signal circuits are not part of this course, many of the design techniques you will learn in this course are also relevant to those areas.

Prerequisites: Level at least 4A Computer Engineering or Electrical Engineering. From a conceptual point of view, this course naturally follows the ECE140/240/340 electronics sequence. There are also linkages to ECE 331 (for EE students) and to ECE 327 (for CompE students).

Tutorial Description: Question and answer on material covered in lectures, specific help with problems from the textbook, background material for labs/projects, and problem-solving skills.

Project Description: A group integrated circuit design project is an essential component of this course. The project involves transistor-level digital circuit design, simulation, and layout.

Computer Experience: Integrated circuit design software tools (Cadence: schematic entry, simulation, layout, DRC, LVS)

Course instructor:	Lan Wei, Ph.D. lan.wei@uwaterloo.ca
Office hours:	TBD
Teaching assistants:	Hazem Elgabra helgabra@uwaterloo.ca
Office hours:	TBD and By appointment

MATERIALS

Required materials:

- Instructor's Course Notes (to be distributed during the term)
- N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th Ed., Pearson, 2010.
- A. Sedra & K.C. Smith, Microelectronic Circuits, 8th Ed., Oxford Press, 2020.

Recommended books:

- J. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, 2nd Ed., Pearson, 2003.
- S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits, McGraw-Hill.

Websites:

- Course website is available on LEARN (all announcements, notes, pre-recorded lectures/tutorial, problem set questions and solutions)
- Live lecture session and office hours on WebEx, access links on LEARN
- Q&A is available on Piazza: piazza.com/uwaterloo.ca/spring2021/ece445
- Tests are tentatively to be distributed via Crowdmark
- Problem sets submission TBD

Tentative topics to be covered during the course:

- Review of the MOS transistor and logic design
  - MOSFET models
  - Logic gate design and sizing
- CMOS inverter characterization
  - Inverter circuit
  - DC transfer characteristic
  - Propagation delay, rise and fall time
- CMOS combinational circuits
  - Characterizing delay in combinational circuits
  - Optimizing delay in combinational circuits
  - Power consumption in combinational circuits
- CMOS sequential circuits
  - Sequencing methods
  - Timing issues in digital circuits
  - Circuits for latches and flip-flops
- CMOS arithmetic circuits
  - Adder circuits
  - Memory circuits
  - Power consumption in digital circuits
  - Physical design of digital circuits
- IC testing
- Interconnect parasticis

SCHEDULE

Lectures
Lectures are pre-recorded, to be uploaded on LEARN.
Live lecture sessions (tentative): 1hr every other week (Thursday 11:30-12:30): On Webex. Access through LEARN.

Tutorials
Pre-recorded, to be uploaded on LEARN.

Office hours
On Webex, access through LEARN.

Any change of schedule will be posted on LEARN.

PROBLEM SETS

Problem sets will be assigned and made available through the course website on LEARN. **You are expected to attempt all assigned problems.** You will be required to submit your solutions of selected questions, which will be graded. Solutions will be provided on LEARN after the submission deadline.

GRADING

Marking Scheme 1		
Homework	5%	
Projects (3)	35%	Project 1: 5%; Project 2: 25%; Project 3: 10%. Due dates TBD.
Test 1	30%	
Test 2	30%	

Marking Scheme 2		
Homework	5%	
Projects (3)	35%	Project 1: 5%; Project 2: 25%; Project 3: 10%. Due dates TBD.
Test 1	20%	
Test 2	40%	

Your final grade will be the higher of the two.

TESTS

- The tests are *open book and open notes.* However, you are NOT allowed to access any content online other than the materials on LEARN and/or e-text book from the publishers' website (text-books only, no other learning resources.) You are absolutely forbidden to consult any other person or website for any course related content during the tests.
- Programmable and/or scientific calculators without formula storage or text display features may be used during the tests. Other electronic devices are not permitted during tests. A list of approved calculators can be found at https://uwaterloo.ca/math/current-undergraduates/regulations-and-procedures/calculator-regulation

Test Policies

- No make-up test.
- If you miss Test 1 for any *valid* reason (e.g. illness supported by a Verification of Illness form that indicates a **severe** illness), your Test 2 will be worth 60%.
- The *instructor is the final judge of validity* for the reason behind your absence. As per the university's policies, under no circumstances will travel be accepted as a valid reason.
- For those taking supplementary exam, you are expected to attend both tests, and your supplementary exam score will be the average of the two.

Academic Integrity: In order to maintain a culture of academic integrity, members of the University of Waterloo community are expected to promote honesty, trust, fairness, respect and responsibility. [Check www.uwaterloo.ca/academicintegrity/ for more information.] **Grievance:** A student who believes that a decision affecting some aspect of his/her university life has been unfair or unreasonable may have grounds for initiating a grievance. Read Policy 70, Student Petitions and Grievances, Section 4, www.adm.uwaterloo.ca/infosec/Policies/policy70.htm. When in doubt please be certain to contact the department's administrative assistant who will provide further assistance. **Discipline:** A student is expected to know what constitutes academic integrity [check www.uwaterloo.ca/academicintegrity/] to avoid committing an academic offence, and to take responsibility for his/her actions. A student who is unsure whether an action constitutes an offence, or who needs help in learning how to avoid offences (e.g., plagiarism, cheating) or about "rules" for group work/collaboration should seek guidance from the course instructor, academic advisor, or the undergraduate Associate Dean. For information on categories of offences and types of penalties, students should refer to Policy 71, Student

Discipline, www.adm.uwaterloo.ca/infosec/Policies/policy71.htm. For typical penalties check Guidelines for the Assessment of Penalties, www.adm.uwaterloo.ca/infosec/guidelines/penaltyguidelines.htm. **Appeals:** A decision made or penalty imposed under Policy 70 (Student Petitions and Grievances) (other than a petition) or Policy 71 (Student Discipline) may be appealed if there is a ground. A student who believes he/she has a ground for an appeal should refer to Policy 72 (Student Appeals) www.adm.uwaterloo.ca/infosec/Policies/policy72.htm. **Note for Students with Disabilities:** AccessAbility Services, located in Needles Hall, Room 1132, collaborates with all academic departments to arrange appropriate accommodations for students with disabilities without compromising the academic integrity of the curriculum. If you require academic accommodations to lessen the impact of your disability, please register with them at the beginning of each academic term.