ECE 636: Advanced Analog Integrated Circuits (Fall 2024)
Course Outline (Tentative)

Course Content: This course covers the design of complementary metal-oxide-semiconductor (CMOS) analog integrated circuits at the transistor level, with an emphasis on the analysis and design of single-stage and multi-stage amplifiers. Related topics including device modeling, biasing, stability, and noise will be presented. In addition, an introduction to higher-level analog and mixed analog/digital systems, such as switched-capacitor circuits, will be covered. Computer-aided design (CAD) software for circuit simulation will also be used.

Instructor:
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Lecture Schedule:
- Wednesdays at 11:30 AM–12:50 PM and Fridays at 1:00–2:20 PM.

Course Topics:
- MOSFET physical characteristics, operating regions, and performance limits
- Systematic design of single-stage and two-stage amplifiers
- Biasing and reference circuits
- Feedback, stability, and settling
- Distortion
- Fully-differential amplifiers and common-mode feedback (CMFB) circuits
- Noise modeling and analysis
- Mismatch analysis
- Introduction to switched-capacitor (SC) circuits

Additional Course Topics (as time permits):
- Layout (physical design) of analog circuits
- Design of three-stage amplifiers
- Amplifier output stages (power amplifiers)
- Introduction to analog-to-digital converters (ADCs)

Background and Pre-requisites:
- Required: One of ECE 242, ECE 340, NE 344, BME 489, or equivalent. These undergraduate courses cover cascode amplifiers, current mirrors, MOS/BJT differential and multi-stage amplifiers, frequency response, feedback, etc. See chapters 8–11 of Sedra and Smith, 8th ed. for a complete list of topics.
- Required: An undergraduate-level course in (1) signals and systems and (2) linear control systems.

Evaluation (tentative):

Review Problem Set:	5%
Mini-Projects:	15% (all equally weighted)
Final Project:	15%
Midterm exam:	15%
Final exam:	50%

Mini-Projects and Graded Review Problem Set: There will be three graded mini-projects. These normally involve circuit design and the use of CAD software. There will also be one graded problem set meant as a review of your pre-requisite knowledge. Students will complete all mini-projects and the graded problem set individually. Partial solutions to some problems may be released.

Non-Graded Problem Sets: Pencil-and-paper-style problem sets will be made available periodically. These problem sets are not to be submitted and are not graded. Partial solutions to some problems in each set may be released.

Final Project: The final project will be assigned by the instructor and will involve transistor-level schematic design and simulation of an analog system (e.g., first stage of a pipelined ADC, sample and hold amplifier, etc.) with various performance specifications. Students will complete the project individually.

Midterm Exam: A 90-minute in-class midterm exam will be given in weeks 6−8 of the term (to be determined). The exam will be closed book and closed notes. A formula sheet will be provided.

Final Exam: There will be a 2.5-hour final exam given during the regular Fall term exam period. The exam will be closed book and closed notes. You will be responsible for all material covered in the course. A formula sheet will be provided.

CAD Software: You will use industry-standard circuit simulation software from Cadence (Virtuoso and Spectre) to complete the mini-projects and final project. No prior experience with these CAD tools is required. Prior experience using Linux is helpful (since the CAD tools we use run on Linux only), but is not required. However, it is expected that you are familiar with mathematical software such as MATLAB or Excel. Note that you can obtain MATLAB, Excel, and other software from the Information Systems and Technology website (https://uwaterloo.ca/information-systems-technology/).

Course Website:

- All relevant course materials will be posted on the ECE 636 course website on Learn (https://learn.uwaterloo.ca).
- Course announcements will also be posted on Learn; please check Learn regularly for these.

Linux Support:

- For any issues related to Linux accounts, licensing, VPN access, etc., contact Eric Praetzel, ECE Lab Instructor/Hardware Specialist (email: praetzel@uwaterloo.ca).

Audit Requirements: You can officially audit the course if you wish, but you are expected to meet the same requirements as students taking the course for credit. You must also obtain the minimum grade for your degree program to pass the course and receive the AUD designation on your transcript.

Reference Texts:

- P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed., Hoboken, NJ: Wiley, 2009.

- B. Razavi, *Design of Analog CMOS Integrated Circuits*, New York: McGraw-Hill, 2001 (1st ed.) or 2016 (2nd ed.).

- T. Chan Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd ed., Hoboken, NJ: Wiley, 2012.

- R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, 3rd ed., Hoboken, NJ: Wiley, 2010. (Second edition available online through University of Waterloo Libraries website.)

- W. M. C. Sansen, *Analog Design Essentials*, Dordrecht, The Netherlands: Springer, 2006 (Available online through University of Waterloo Libraries website.)

- A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 6th ed. or later, New York: Oxford University Press.

Academic Integrity: In order to maintain a culture of academic integrity, members of the University of Waterloo community are expected to promote honesty, trust, fairness, respect and responsibility. [Check www.uwaterloo.ca/academicintegrity/ for more information.]

Plagiarism: For all mini-projects, final project, and the graded problem set, students are welcome to consult with others. However, the material submitted by each student for evaluation must be the student's own work. This means that text, equations, analysis, diagrams, figures, graphs, tables, CAD files, simulation results, etc. must be the student's own and not copied from other sources. Students will be severely penalized if they are found to have plagiarized submitted work.

Grievance: A student who believes that a decision affecting some aspect of his/her university life has been unfair or unreasonable may have grounds for initiating a grievance. Read Policy 70, Student Petitions and Grievances, Section 4, www.adm.uwaterloo.ca/infosec/Policies/policy70.htm. When in doubt please be certain to contact the department's administrative assistant who will provide further assistance.

Discipline: A student is expected to know what constitutes academic integrity [check www.uwaterloo.ca/academicintegrity/] to avoid committing an academic offense, and to take responsibility for his/her actions. A student who is unsure whether an action constitutes an offence, or who needs help in learning how to avoid offences (e.g., plagiarism, cheating) or about "rules" for group work/collaboration should seek guidance from the course instructor, academic advisor, or the undergraduate Associate Dean. For information on categories of offences and types of penalties, students should refer to Policy 71, Student Discipline, www.adm.uwaterloo.ca/infosec/Policies/policy71.htm. For typical penalties check Guidelines for the Assessment of Penalties, www.adm.uwaterloo.ca/infosec/guidelines/penaltyguidelines.htm.

Appeals: A decision made or penalty imposed under Policy 70 (Student Petitions and Grievances) (other than a petition) or Policy 71 (Student Discipline) may be appealed if there is a ground. A student who believes he/she has a ground for an appeal should refer to Policy 72 (Student Appeals) www.adm.uwaterloo.ca/infosec/Policies/policy72.htm.

Note for Students with Disabilities: AccessAbility Services, located in Needles Hall, Room 1401, collaborates with all academic departments to arrange appropriate accommodations for students with disabilities without compromising the academic integrity of the curriculum. If you require academic accommodations to lessen the impact of your disability, please register with the AccessAbility Services at the beginning of each academic term.

Note on the use of Generative AI (GenAI): This course includes the independent development and practice of specific skills, such as analog circuit design. Therefore, the use of Generative artificial intelligence (GenAI) trained using large language models (LLM) or other methods to produce text, images, circuit schematics, simulation results, or code, like ChatGPT, DALL-E, or GitHub CoPilot, is not permitted in this class. Unauthorized use in this course, such as running course materials through GenAI or using GenAI to complete a course assessment is considered a violation of Policy 71 (plagiarism or unauthorized aids or assistance). Work produced with the assistance of AI tools does not represent the author's original work and is therefore in violation of the fundamental values of academic integrity including honesty, trust, respect, fairness, responsibility and courage (ICAI, n.d.).

You should also be prepared to show your work. To demonstrate your learning, you should keep your rough notes, including research notes, brainstorming, and drafting notes. You may be asked to submit these notes along with earlier drafts of their work, either through saved drafts or saved versions of a document. If the use of GenAI is suspected where not permitted, you may be asked to meet with your instructor to provide explanations to support the submitted material as being your original work. Through this process, if you have not sufficiently supported your work, academic misconduct allegations may be brought to the Dean of Engineering.