ECE 730T30 Advanced VLSI Devices

COURSE DESCRIPTION:

The nano era has seen modern VLSI technologies become increasingly sensitive to structural details and fabrication techniques. While "technology scaling" continues as the strongest driver for technology advancement, it has evolved from traditional Dennard Scaling into a multi-dimensional concept that combines new materials, novel structures and different physical principles. Accordingly, this course will cover topics such as: advanced VLSI devices design; future challenges of VLSI devices; the implications for device electrical performance caused by fabrication technique, physical models for nanometer scale structures, control of electrical characteristics (threshold voltage, short channel effects, ballistic transport) in small structures; and alternative device structures for VLSI in the nano era.

Expected background knowledge: solid state physics and devices (ECE630, or equivalent). Students should be familiar with the physical principles and operation of p-n junctions, MOS capacitors and long-channel MOSFETs.

For those who would like to **request override** due to lack of prerequisite course, there will be a time slot before the first lecture (likely on Sept 6, exact time/location/details to be announced on LEARN) for you to come and take a short test with the instructor to determine whether the override can be granted.

Class Days/Hour/Locations: TBD
Instructor: Prof. Lan Wei. lan.wei@uwaterloo.ca, E5-4023.

COURSE OBJECTIVE:

- At the end of the course, you will be able to:
  - Make projections about CMOS device scaling and how it affects circuit/system performance
  - Recognize the relevant device physics that underlies CMOS device design
  - Go to a conference or read a journal article about CMOS devices and use the knowledge obtained in this course to understand the material
  - Design a state-of-the-art MOSFET and project its performance
  - Use electronic design automation (EDA) tools for device simulation and interpret results from device simulation
- Develop an intuitive feel in addition to solving equations
- Obtain necessary skills to explore the research space of state-of-the-art VLSI technology

GRADING POLICY:

The Course grade will be based on the total numerical score on the following:

- Homework: 20%
- Project: 40%
- Final: 40%

HOMEWORK:

- Usually around one week to finish each homework. Submission details and deadline see each homework assignment.
- No credit for late submission.

COURSE MATERIAL:

- **Textbook:**
  - **Y. Taur & T. H. Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press 2nd Edition**
    - ISBN-13: 9780521832946 (Hardcopy, 2nd edition)
    - Roughly, I will cover Chapters 1 – 5 and 10
- **Course notes:**
  - Available on-line (course website LEARN)

COURSE OUTLINE (TENTATIVE):

- Overview of the semiconductor industry (~1 week)
- MOSFET – MOS capacitor, MOSFET long channel behavior (a short review) (~1week)
- Si MOSFET device scaling, non-scaling factors (~1 week)
- Device modeling (~1 week)
  - EDA tools, fundamentals of numerical device simulation, interpretation of device simulation results and tricks of the trade
- MOSFET electrostatics (~2.5 weeks)
  - Short-channel MOSFET
  - Channel length, scale length theory, minimum channel length
  - PDSOI, FDSOI, ultra-thin body SOI, double-gate, FinFET, multi-gate FET, gate-all-around (nanowire) FET
  - Threshold voltage, quantum effects
  - Non-uniform channel doping, halo, super-halo
- MOSFET electrodynamics (~2.5 weeks)
  - Carrier mobility, velocity saturation
  - Scattering theory, ballistic transport
  - Virtual source model
  - Strain effects, alternative channel materials (Ge, III-V)
- High field effects (~1 week)
  - Impact ionization and breakdown, band-to-band tunneling, tunneling into gate dielectrics, hot carriers, dielectric degradation mechanisms
- Parasitic elements (~0.5 week)
  - Series resistance, parasitic capacitance
  - Interconnect R and C, interconnect scaling
- CMOS performance factors (~1 week)
  - CMOS circuit elements, propagation delay, delay metrics, power dissipation
  - Device pitch scaling
  - Device design tradeoff, energy-delay optimization