# ECE 621: Computer Organization
# Winter 2025

November 16, 2024

## Course description

Organization and performance of conventional uniprocessors, pipelined processors, parallel processors and multiprocessors; memory and cache structures; multiprocessor algorithms and synchronization techniques; special-purpose architectures.

## Class days, times, building, and room number

**Class duration** Jan 6, 2025 – Apr 4, 2025.
**Lecture 1**: Friday 13:00 – 15:50, E5-4106/28
**Quiz 1 and Quiz 2 dates**: TBD
Please consult the tentative schedule for important dates. This has been posted on LEARN.

## Instructor information

**Instructor:** Prof. Hiren Patel, `Email`
**Office:** E5-4018.
**Office hours:** Send an email.

## Teaching assistant information

**TA**: None
**Note:** When sending email to the TA or the course instructor:

1. Ensure that the email's subject contains 621W24.
2. The email is sent from a University of Waterloo mail server with your official UWid. Email from unofficial addresses (even if sent through) such as `gmail` and the like will not be responded to.

## Course websites

- Piazza: We will use this for questions and answers.
- **LEARN**: This website will contain lecture materials, problem sets, and solutions. LEARN **will** be used as the primary medium for communication with the class.
- **https://git.uwaterloo.ca**: Benchmarks, examples and scripts will be posted in git repositories.

## Course delivery

- Lectures: Synchronous in-person. I will make an attempt to post slides before the lecture.

**COVID Contingency**

In the event that this course must be delivered fully online, we will move lectures, tutorials, and labs to synchronous online.

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# Course textbook

- D. A. Patterson and J. L. Hennessy, Computer Architecture: A Quantitative Approach, $6^{th}$ Edition, Morgan Kaufmann, 2017.

# Course objectives

- Become fluent in the architectures of pipelined high performance processors
- Be competent in the instruction scheduling strategies in integer/floating point pipelines and reducing pipeline stalls due to various hazards
- Multiprocessor performance limitations, distributed cache coherence protocols and multiprocessor synchronization problems.
- Solve design problems related to topics in computer architecture in a timed setting.

# Course requisites

Antireq: ECE 429

# Evaluation

The course grade will be based on quizzes and the project.

## Project

The project *can* contribute to a maximum of $40\%$ of the final grade $G$. The amount the project contributes to the final grade depends on the combined grade received in the quizzes. The project is split into 6 lab deliverables (PD)s. The distribution of marks for the project deliverables is as follows.

$$(PD_0, PD_1, PD_2, PD_3, PD_4, PD_5) = (0\%, 2\%, 3\%, 5\%, 15\%, 15\%)$$

Let us assume that $LG_i$ is the grade received out of 100 for the $i^{th}$ lab deliverable, $PD_i$. For example, $LG_1$ refers to the grade out of 100 received for $PD_1$. We compute the lab marks $L$ as

$$L = (LG_1/100) * 2 + (LG_2/100) * 3 + (LG_3/100) * 5 + ((LG_4/100) + (LG_5/100)) * 30.$$

## Quizzes

The quizzes contribute to a maximum of $60\%$ of the final grade. Let $Q1$ and $Q2$ be the grades received out of 100 for quiz 1 and 2, respectively. We compute the marks received from examinations as

$$E = MAX((25 * Q1/100 + 35 * Q2/100), (15 * Q1/100 + 45 * Q2/100)).$$

## Final grade

We compute your final course grade $G$ as follows.

- If $E \leq 24$, then your course grade $G = E$. This means that your project counts for 0 if you are unable to achieve a combined 24 out of 60 of the quiz marks. Note that 24 is $40\%$ of the quiz component $E$.
- If $E \geq 30$, then your course grade is $G = E + L$. This means that your project counts for $L$ if you achieve a combined 30 out of 60 of the quiz marks. Note that 30 is $50\%$ of the examination component $E$.
- If $24 < E < 30$, then $G = E + ((E - 24)/6) * L$.

The instructor reserves the right to adjust the weights of any of the quizzes and project components, as well as curving the final marks. The instructor also reserves the right to update and adjust the deadlines and schedule.

## Late project submissions

Every $PD$ is due on or before the deadline. If for any reason you are unable to submit it by the deadline, you would receive a 0 for that $PD$. In order to recover a maximum of 50% of the marks for the respective $PD$, you will be able to submit it until the last day of class. We will only re-evaluate it after the last day of class. For example, if you miss the deadline for $PD_3$, then you can receive a maximum of $2.5\%$ if it is submitted before the last day of class. Of course, we would evaluate it and assess the grade for the late submission.

### Missed quiz 1

A student missing the quiz 1 will receive a score of 0 for that quiz. If the student provides appropriate documentation (e.g. verification of illness form) within 48 hours of the exam and it is accepted by the instructor, then quiz 2 will weigh $60\%$. This means the weight of quiz 1 gets shifted to quiz 2. Therefore, $E = 60 * F$.

### Missed quiz 2

A student missing only quiz 2 will receive a score of 0 for quiz 2. If the student provides appropriate documentation within 48 hours of the final exam and it is accepted by the instructor, then the student will receive a grade of INC, and the student will have to complete the requirement of quiz 2 for future a offering of ECE621 one year later.

### Review of quiz 1

Review of quiz 1 must occur within 2 weeks of the return of the grades for the quiz. The request must be made in writing. You will need to state the questions that should be reconsidered, and reasons for it. Note that later requests for re-assessments will not be honoured.

### Academic violations

Any violations of academic honesty and integrity policies will result in receiving a 0 for the corresponding assessment, and an additional $-5\%$ will be assessed on the final grade. Multiple infractions will incur multiple reductions on the final grade.

## Project Overview

The project will be completed in pairs.
**Cycle-accurate Implementation of a processor:** You will design and implement a cycle-accurate RISCV processor architecture. Further details on the specifics of the architecture and compiler suite used will be provided in class.

## Topics

Performance metrics, instruction-set architectures, caches, virtual memory, pipelining and branch prediction, superscalar, static and dynamic scheduling, multiprocessors, cache coherency, memory consistency models, hardware multithreading, and on-chip interconnects.

| Topic | HP5 Sections |
|---|---|
| Performance metrics | 1.1 – 1.12 |
| Instruction-set architecture | A.1 – A.7, A.9 – A.11 |
| Caches | B.1 –B.3, 2.1 – 2.3 |
| Virtual memory | B.4 – B.7, 2.5 – 2.8 |
| Pipelining and branch prediction | C.1 – C.7, 3.1 – 3.3, 3.9 |
| Superscalar | |
| Static and dynamic scheduling | 3.2, 3.4 – 3.5, 3.11 |
| VLIW/EPIC | 3.7 |
| Hardware multithreading | 3.12, 3.15 |
| Multiprocessors: Synchronization | 5.5 |
| Multiprocessors: Cache coherency | 5.1 – 5.4 |
| Multiprocessors: Memory consistency models | 5.5.6 – 5.10 |
| Data-level parallelism | 4 |

# University Policies

The following statements are a required part of every course outline. You may also want to consult related information at https://uwaterloo.ca/engineering/current-undergraduate-students/academic-support/course-responsibilities, and Petitions and Challenges. The actual policies can be found at: Policies.

Academic integrity: In order to maintain a culture of academic integrity, members of the University of Waterloo community are expected to promote honesty, trust, fairness, respect and responsibility. (Check www.uwaterloo.ca/academicintegrity/ for more information.)

Grievance: A student who believes that a decision affecting some aspect of his/her university life has been unfair or unreasonable may have grounds for initiating a grievance. Read Policy 70, Student Petitions and Grievances, Section 4, Policy 70. When in doubt please be certain to contact the department's administrative assistant who will provide further assistance.

Discipline: A student is expected to know what constitutes academic integrity (check www.uwaterloo.ca/academicintegrity/) to avoid committing an academic offence, and to take responsibility for his/her actions. A student who is unsure whether an action constitutes an offence, or who needs help in learning how to avoid offences (e.g., plagiarism, cheating) or about "rules" for group work/collaboration should seek guidance from the course instructor, academic advisor, or the undergraduate Associate Dean. For information on categories of offences and types of penalties, students should refer to Policy 71, Student Discipline, www.adm.uwaterloo.ca/infosec/Policies/policy71.htm. For typical penalties check Guidelines for the Assessment of Penalties, www.adm.uwaterloo.ca/infosec/guidelines/penaltyguidelines.htm.

Appeals: A decision made or penalty imposed under Policy 70 (Student Petitions and Grievances) (other than a petition) or Policy 71 (Student Discipline) may be appealed if there is a ground. A student who believes he/she has a ground for an appeal should refer to Policy 72 (Student Appeals) www.adm.uwaterloo.ca/infosec/Policies/policy72.htm.

Note for students with disabilities: The Office for Accessability, located in Needles Hall, Room 1401, collaborates with all academic departments to arrange appropriate accommodations for students with disabilities without compromising the academic integrity of the curriculum. If you require academic accommodations to lessen the impact of your disability, please register with the Accessability at the beginning of each academic term.