ECE 637 Digital Integrated Circuits
DRAFT Course Outline

Fall 2024 - Prof. Vincent Gaudet

Course description: Digital CMOS integrated circuits are enabling today's electronic systems, ranging from power-efficient and portable personal electronics to cloud computing and the high-performance compute servers at the core of today's Internet. Several billion transistors can be integrated into a single CMOS chip, and this number is expected to continue to increase over coming years as CMOS technologies shrink and transistor performance improves. However, the continued scaling of CMOS technologies deep into the nanometer regime also leads to emerging design challenges, in terms of evolving transistor models, high-speed design, energy-efficient design, integration with other modalities (e.g. analog and sensors), and testing.

This course covers transistor, circuit, and physical-design aspects of CMOS digital integrated circuits. Major topics include: (a) optimization of critical path delays using logical effort, (b) power optimization, (c) design of high-speed sequential systems, (d) design of efficient arithmetic circuits, and (d) physical design of integrated circuits, i.e. how to translate your transistor-level designs into "blueprints" that can be used by fabrication engineers to build your design. The project uses Cadence tools for schematic entry, simulation, and layout. The course has been designed to be complementary to ECE 636, which focuses on analog CMOS design.

Prerequisites: (a) Undergraduate courses in microelectronic circuit design, e.g. using the Sedra/Smith *Microelectronic Circuits* textbook (e.g. ECE 240 and ECE 340); (b) undergraduate courses in digital logic design (e.g. ECE 124). More senior-level courses in digital CMOS circuits (e.g. ECE 445), hardware architecture (e.g. ECE 327), or analog design (e.g., ECE 444) are valuable but not necessary.

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Grading

- Project 1 20%
- Project 2 30%
- Final Examination 50%

Materials

- Instructor's Course Notes and other materials available on LEARN
- Sedra/Smith/Chan Carusone/Gaudet, *Microelectronic Circuits*, 8th Ed., Oxford Press, 2020.
- Rabaey/Chandrakasan/Nikolic, *Digital Integrated Circuits*, 2nd Ed., Prentice-Hall, 2003.
- Weste/Harris, *CMOS VLSI Design*, 4th Ed., Pearson Education, 2011.

Lectures: Friday 2:30 - 5:20pm EIT 3151

Project Description: Two projects, to be completed individually, involve transistor-level design of arithmetic and sequential circuits with up to a few hundred transistors, and include simulation, optimization, layout, and post-layout verification components. Details of the projects will be provided later on.

Final Exam Policy

- The final examination is *closed book.*
- The final examination is **comprehensive**, i.e., covers material from the start of term, as well as any reasonable pre/co-requisite materials.
- You are allowed to bring a single letter-sized double-sided crib sheet *that you have made yourself* to the final examination. You are allowed to write anything on the sheet. The instructor reserves the right to collect crib sheets.
- Programmable and/or scientific calculators without formula storage or text display features may be used during the midterm and final examinations. Other electronic devices are not permitted during the final examinations.

Late Projects

- You will get a total of five (5) grace days, totaled over the two projects, for late submission. The penalty after running out of grace days is -10%/day, applied first to the last project, then the second

Collaboration vs. Plagiarism

- The projects are to be completed individually, albeit with the following instructions:
  - I encourage you to interact with other students to get to know the Cadence software and its particularities. The learning curve for Cadence is steep and it helps to have others around you.
  - I expect that most of you will have "high-level" discussions with others about how to approach the projects, but once pen hits paper and fingers hit keyboard, you must do your own work.

Recording of Lectures

- In the event of COVID or other illness, I reserve the right to deliver some of the lectures over zoom or Teams. If this happens, I will communicate instructions in advance over LEARN. Lectures would take place live/synchronously at the same time as the scheduled lectures.
- I do not intend to record my lectures. However, **your own audio or video recordings are allowed for personal use only** and may not be shared beyond registered course attendees. Such recordings must be destroyed at the end of the term.

Academic Integrity: In order to maintain a culture of academic integrity, members of the University of Waterloo community are expected to promote honesty, trust, fairness, respect and responsibility. [Check www.uwaterloo.ca/academicintegrity/ for more information.] **Grievance:** A student who believes that a decision affecting some aspect of his/her university life has been unfair or unreasonable may have grounds for initiating a grievance. Read Policy 70, Student Petitions and Grievances, Section 4, www.adm.uwaterloo.ca/infosec/Policies/policy70.htm. When in doubt please be certain to contact the department's administrative assistant who will provide further assistance. **Discipline:** A student is expected to know what constitutes academic integrity [check www.uwaterloo.ca/academicintegrity/] to avoid committing an academic offence, and to take responsibility for his/her actions. A student who is unsure whether an action constitutes an offence, or who needs help in learning how to avoid offences (e.g., plagiarism, cheating) or about "rules" for group work/collaboration should seek guidance from the course instructor, academic advisor, or the undergraduate Associate Dean. For information on categories of offences and types of penalties, students should refer to Policy 71, Student Discipline, www.adm.uwaterloo.ca/infosec/Policies/policy71.htm. For typical penalties check Guidelines for the Assessment of Penalties, www.adm.uwaterloo.ca/infosec/guidelines/penaltyguidelines.htm. **Appeals:** A decision made or penalty imposed under Policy 70 (Student Petitions and Grievances) (other than a petition) or Policy 71 (Student Discipline) may be appealed if there is a ground. A student who believes he/she has a ground for an appeal should refer to Policy 72 (Student Appeals) www.adm.uwaterloo.ca/infosec/Policies/policy72.htm. **Note for Students with Disabilities:** The Office for Persons with Disabilities (OPD), located in Needles Hall, Room 1132, collaborates with all academic departments to arrange appropriate accommodations for students with disabilities without compromising the academic integrity of the curriculum. If you require academic accommodations to lessen the impact of your disability, please register with the OPD at the beginning of each academic term.