University of Waterloo

ECE 740: Mixed-Signal Integrated Circuits (Spring 2025)

ECE 740 is an advanced-level Integrated Circuit (IC) design course that explores the principles and practical techniques of mixed-signal IC design. The course covers a wide range of mixed-signal components that are essential to modern electronic systems, including data converters such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), time-to-digital converters (TDCs), digital-to-time converters (DTCs), associated anti-aliasing/reconstruction filters, digital phase-locked loops (PLLs), and/or digital low drop-out regulators (LDOs). These circuits are fundamental building blocks in numerous applications, from consumer electronics (e.g., smartphones, modems, gaming consoles, and audio/video devices) to advanced computing and IoT systems (e.g., quantum computers, application-specific accelerators, unmanned aerial vehicles, and autonomous vehicles). The course integrates fundamental Analog Signal Processing (ASP) and Digital Signal Processing (DSP) theories with circuit design principles critical to mixed-signal IC development. Students will examine:

- Device properties and behavior.
- Circuit topologies and their associated non-idealities.
- Essential building blocks and architecture.
- Design methodologies and practical implementation challenges in data converters, filters, switched-capacitor circuits, and other types of mixed-signal circuits and systems.

By the end of the course, students will have a strong grasp of both theoretical concepts and hands-on design strategies for state-of-the-art mixed-signal ICs.

Course Objectives: ECE 740 is designed for graduate students with prior knowledge of signal processing and circuit theory who wish to deepen their expertise in mixed-signal IC design. The course emphasizes both theoretical understanding and practical design skills applicable to academic research and industry practice. Key Learning Outcomes include:

1. Understand the fundamental trade-offs, constraints, and design considerations in mixed-signal ICs.
2. Apply theoretical knowledge through class projects and design exercises using industry-standard EDA tools such as Cadence, Synopsys, and Mentor, and commercial Process Design Kits (PDKs) such as GF 12nm FinFET, GF 22nm FDX-SOI, TSMC 65nm and TSMC 180nm. **Note that an NDA is required to access the PDKs.**
3. Explore new architectures and topologies beyond classical designs, potentially leading to peer-reviewed **publications** in IEEE CASS and SSCS.

4. Select students may have the chance to fabricate and test their designs at the University of Waterloo, providing real-world experience in **silicon prototyping**.

Through lectures, assignments, discussions, and project-based learning, students will be well-prepared to contribute to both academic research and industrial applications in the field of mixed-signal IC design.

Pre-requisites: ECE 340, ECE 444 Integrated Analog Electronics (or equivalent) and ECE 445 Integrated Digital Electronics (or equivalent). Experience with MATLAB (or Python), Cadence Virtuoso and Synopsys Calibre.

Instructor:	Shiyu Su	shiyu.su@uwaterloo.ca	E5-4016
TA:	Zhengyi Qiu	zhengyi.qiu@uwaterloo.ca	E7-4406
Lecture:	Regular: Wednesday	10:00 – 11:20	EIT-3141
	Regular: Thursday	10:00 – 11:20	EIT-3141
	Make-up: TBD		
Tutorial:	TBD		

Tutorials: You are strongly encouraged to attend tutorials on tool setup and problem solving.

Office Hours: Instructor office hours will be provided by the end of the second week of class.

References:

There is no main textbook. Relevant contents are mainly from IEEE Journal of Solid-State Circuits and Transactions on Circuits and Systems. Supplementary texts include:

- Razavi, Analysis and Design of Data Converters, 2025.
- Razavi, Principles of Data Conversion System Design, 1995.
- van de Plassche, CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, 2003.
- Pelgrom, Analog-to-Digital Conversion, 2010.
- Norsworthy et al., Delta-Sigma Data Converters: Theory, Design, and Simulation, 1996
- A. Williams and F. Taylor, Electronic Filter Design Handbook, 1995.
- Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, 2016.
- A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 2004.
- P. R. Gray et al., *Analysis and Design of Analog Integrated Circuits*, 2001.

Topics to be covered in lectures:

Week	Topic	Assignments	
1	Introduction	Assignment 1	Design Project: Reports + Presentation
2	Signal Processing		
3	ADC Basics		
4	ADC Architectures (I)	Assignment 2	
5	ADC Architectures (II)		
6	DAC Basics		
7	DAC Architectures	Assignment 3	
8	Enhancement Techniques		
9	Anti-aliasing and Reconstruction Filters		
10	Digital Phase-locked Loops (or Digital LDO)		
11	**Guess Lectures from Analog Devices, Inc. (ADI)**		
12	Project Presentations (i.e., Schematic Review)		

Evaluation and Grading:

Assignments	30%	Triweekly
Three assignments will be given after the associated lectures, covering problems and small design projects. **Independent work is required**.		
Design Project	50%	Throughout the term (**5% bonus marks**)
• Mid-term report on algorithm development (10%) • Schematic design review presentation in class (20%) – **All group members must actively present for a similar amount of time**. • Final report (20%) Projects will be completed in **teams of 2–3 students** using TSMC 65nm, TSMC 180nm, GF 12nm, or GF 22nm technologies.		
Final Examination*	20%	University schedule

* Open book and open notes. Write in pen/pencil.

Course Website:

• Course announcements and documents will be posted on **LEARN** (https://learn.uwaterloo.ca).

• Please check LEARN daily for new announcements or set up your LEARN account so that you are informed of new announcements by email.

Piazza:

• The Piazza page for this class is: https://piazza.com/uwaterloo.ca/spring2025/ece740

• Please allow up to 48 hours for a response.

Absence Policies:

• If you miss any one of the exams for any valid reason (e.g. illness supported by a Verification of Illness form that indicates a severe illness) and declare your absence in **Quest**, the weight of that exam will be added to the other exam. If you miss both exams, it will be handled on a case-by-case basis. Note that no make-up tests will be offered.

• The instructor is the final judge of validity for the reason behind your absence.

Additional Information and Policies:

Academic integrity: In order to maintain a culture of academic integrity, members of the University of Waterloo community are expected to promote honesty, trust, fairness, respect and responsibility. [Check the Office of Academic Integrity for more information.]

Grievance: A student who believes that a decision affecting some aspect of his/her university life has been unfair or unreasonable may have grounds for initiating a grievance. Read Policy 70, Student Petitions and Grievances, Section 4. When in doubt, please be certain to contact the department's administrative assistant who will provide further assistance.

Discipline: A student is expected to know what constitutes academic integrity to avoid committing an academic offence, and to take responsibility for his/her actions. [Check the Office of Academic Integrity for more information.] A student who is unsure whether an action constitutes an offence, or who needs help in learning how to avoid offences (e.g., plagiarism, cheating) or about "rules" for group work/collaboration should seek guidance from the course instructor, academic advisor, or the undergraduate associate dean. For information on categories of offences and types of penalties, students should refer to Policy 71, Student Discipline. For typical penalties, check Guidelines for the Assessment of Penalties.

Appeals: A decision made or penalty imposed under Policy 70, Student Petitions and Grievances (other than a petition) or Policy 71, Student Discipline may be appealed if there is a ground. A student who believes he/she has a ground for an appeal should refer to Policy 72, Student Appeals.

Note for students with disabilities: AccessAbility Services, located in Needles Hall, Room 1132, collaborates with all academic departments to arrange appropriate accommodations for students with disabilities without compromising the academic integrity of the curriculum. If you require academic accommodations to lessen the impact of your disability, please register with AccessAbility Services at the beginning of each academic term.