ECE 621: Computer Organization
Winter 2022

December 8, 2021

Course description

Organization and performance of conventional uniprocessors, pipelined processors, parallel processors and multiprocessors; memory and cache structures; multiprocessor algorithms and synchronization techniques; special-purpose architectures.

Class days, times, building, and room number

Class duration January 5, 2022 – April 5, 2022.
[redacted]
Quiz 1 and Quiz 2 dates: TBD
Please consult the tentative schedule for important dates. This has been posted on LEARN.

Instructor information

Instructor: Prof. Hiren Patel, `Email`
Office: [redacted]
Office hours: TBD.
Note: When sending email to the course instructor:

1. Ensure that the email's subject contains 621W22.
2. The email is sent from a University of Waterloo mail server with your official UWid. Email from unofficial addresses (even if sent through) such as `gmail` and the like will not be responded to.

Course websites

- Piazza: We will use this for questions and answers.
- **LEARN**: This website will contain lecture materials, problem sets, and solutions. LEARN **will** be used as the primary medium for communication with the class.
- **https://git.uwaterloo.ca**: Benchmarks, examples and scripts will be posted in git repositories.

Course delivery

- Lectures: Synchronous in-person.

COVID Contingency

In the event that this course must be delivered fully online.

Course textbook

- D. A. Patterson and J. L. Hennessy, Computer Architecture: A Quantitative Approach, 6^{th} Edition, Morgan Kaufmann, 2017.

Course objectives

- Become fluent in the architectures of pipelined high performance processors
- Be competent in the instruction scheduling strategies in integer/floating point pipelines and reducing pipeline stalls due to various hazards
- Multiprocessor performance limitations, distributed cache coherence protocols and multiprocessor synchronization problems.
- Solve design problems related to topics in computer architecture in a timed setting.

Course requisites

Antireq: ECE 429

Evaluation

The course grade will be based on the following components:

Table 1: Marks Distribution

Component	$Scheme_1$	$Scheme_2$
Project	50%	50%
Quiz 1	25%	15%
Quiz 2	25%	35%

There are two types of projects that students can do.

T1: Students (individually) will implement a cycle-accurate 5-stage RISCV pipelined processor. This is the recommended project for non-research students, and those who have limited to no background in the course content. This project is split into 6 deliverables (PD)s. The 50% of the project marks are distributed across the deliverables as follows.

$$(PD_0, PD_1, PD_2, PD_3, PD_4, PD_5) = (2\%, 6\%, 6\%, 6\%, 12\%, 18\%)$$

T2: A student-proposed and instructor-vetted, and approved research project. This option is primarily limited to research students.

The final course mark is obtained as follows.

$$\text{Final Course Mark} = MAX(Scheme_1, Scheme_2)$$

Note:

1. Quizzes are to be done individually. They are closed books, and closed notes. A simple calculator **may** be allowed, but no computers or cellphones.
2. Each quiz will be available for the students to complete for a window of 24 hours. The actual time allotted to taking (writing) the quiz will be shorter than that. It will typically be in the range of 90 minutes to 150 minutes.
3. Review of quizzes must occur within 2 weeks of the return of the respective quiz. The request must be made in writing. You will need to state the questions that should be reconsidered, and reasons for it. Note that later requests for re-assessments will not be honoured.
4. No extensions will be made to PD submission dates. A late PD submission will be worth a maximum of 50% of the marks originally allocated to that PD if it is submitted before the deadline of the next PD. The submission of the late PD after the deadline of the next PD will receive a mark of 0. For example, a late submission for PD_1 can achieve a maximum of 3% only if it is submitted before the deadline for PD_2. After the deadline of PD_2, any submission of PD_1 will receive a grade of 0.

5. Any student missing any of the quizzes will receive a score of 0 for the respective component.
6. Any student missing any of quizzes for legitimate reasons must provide appropriate documentation (e.g. verification of illness form) within 48 hours of the incident affecting the component. If documentation is not provided in the appropriate time period, the student will receive a 0 for the component without further reconsideration.
7. If you miss the quiz 1, and **if appropriate documentation is provided within the appropriate time period, and the instructor has accepted the legitimate reason for missing the quiz**, the quiz weight will be shifted to the next quiz.
8. A student missing only quiz 2, and provides appropriate documentation within the appropriate time period will receive a grade of INC, and the student will have to complete the requirement of the quiz as a final exam for future offering of 621 one year later. No special quizzes will be offered prior to the following year's offering of the course.
9. A student that misses both the quizzes, will need to take all quizzes/examination components (quiz 1 and quiz 2 or midterm exam and final exam) for the next offering of the course one year later.
10. The student must obtain a **minimum of 30% out of 50% on the project component to pass this course**.
11. The student must obtain a **minimum of 25% of the 50% allocated for the combined quizzes to pass this course**.
12. The instructor reserves the right to adjust the weights of any of the quiz, exam and project components, as well as curving the final marks. The instructor also reserves the right to update and adjust the deadlines and schedule.
13. Any violations of academic honesty and integrity policies will result in an automatic failure of the course with a final score of 0.

T1: Project Overview

The project will be completed individually.
Cycle-accurate Implementation of a processor: You will design and implement a cycle-accurate RISCV processor architecture. Further details on the specifics of the architecture and compiler suite used will be provided in class.

T2: Project Overview

In week 3, a tentative project description will need to be provided. Upon approval, specific deadlines will be established.

Topics

Performance metrics, instruction-set architectures, caches, virtual memory, pipelining and branch prediction, superscalar, static and dynamic scheduling, multiprocessors, cache coherency, memory consistency models, hardware multithreading, and on-chip interconnects.

Topic	HP5 Sections
Performance metrics	1.1 – 1.12
Instruction-set architecture	A.1 – A.7, A.9 – A.11
Caches	B.1 –B.3, 2.1 – 2.3
Virtual memory	B.4 – B.7, 2.5 – 2.8
Pipelining and branch prediction	C.1 – C.7, 3.1 – 3.3, 3.9
Superscalar	
Static and dynamic scheduling	3.2, 3.4 – 3.5, 3.11
VLIW/EPIC	3.7
Hardware multithreading	3.12, 3.15
Multiprocessors: Synchronization	5.5
Multiprocessors: Cache coherency	5.1 – 5.4
Multiprocessors: Memory consistency models	5.5.6 – 5.10
Data-level parallelism	4

University Policies

The following statements are a required part of every course outline. You may also want to consult related information at https://uwaterloo.ca/engineering/current-undergraduate-students/academic-support/course-responsibilities, and Petitions and Challenges. The actual policies can be found at: Policies.

Academic integrity: In order to maintain a culture of academic integrity, members of the University of Waterloo community are expected to promote honesty, trust, fairness, respect and responsibility. (Check www.uwaterloo.ca/academicintegrity/ for more information.)

Grievance: A student who believes that a decision affecting some aspect of his/her university life has been unfair or unreasonable may have grounds for initiating a grievance. Read Policy 70, Student Petitions and Grievances, Section 4, Policy 70. When in doubt please be certain to contact the department's administrative assistant who will provide further assistance.

Discipline: A student is expected to know what constitutes academic integrity (check www.uwaterloo.ca/academicintegrity/) to avoid committing an academic offence, and to take responsibility for his/her actions. A student who is unsure whether an action constitutes an offence, or who needs help in learning how to avoid offences (e.g., plagiarism, cheating) or about "rules" for group work/collaboration should seek guidance from the course instructor, academic advisor, or the undergraduate Associate Dean. For information on categories of offences and types of penalties, students should refer to Policy 71, Student Discipline, www.adm.uwaterloo.ca/infosec/Policies/policy71.htm. For typical penalties check Guidelines for the Assessment of Penalties, www.adm.uwaterloo.ca/infosec/guidelines/penaltyguidelines.htm.

Appeals: A decision made or penalty imposed under Policy 70 (Student Petitions and Grievances) (other than a petition) or Policy 71 (Student Discipline) may be appealed if there is a ground. A student who believes he/she has a ground for an appeal should refer to Policy 72 (Student Appeals) www.adm.uwaterloo.ca/infosec/Policies/policy72.htm.

Note for students with disabilities: The Office for Accessability, located in Needles Hall, Room 1401, collaborates with all academic departments to arrange appropriate accommodations for students with disabilities without compromising the academic integrity of the curriculum. If you require academic accommodations to lessen the impact of your disability, please register with the OPD at the beginning of each academic term.