E&CE 637

Digital CMOS Integrated Circuits

E&CE 637 July 2021

Calendar Description:

Design of CMOS digital integrated circuits at the transistor level. Related topics include MOSFET switch and models, logic gate design, transistor sizing, interconnect parasitics, gate delay, timing design, logical effort, static and dynamic logic families, latch and flip-flop elements, adder circuit and architectures.

Prerequisite: E&CE 445
*Project

Detailed Description:

		Lecture Hours
1.	**MOS Transistor - Review** - Static behavior - Parasitic capacitances and dynamic behavior - Short channel effects - Concept of scaling and trends - SPICE MOS models - Process variations & process impact	6
2.	**MOS Inverter** - Properties - Static behavior – switching threshold, Noise margin - Dynamic behavior – capacitance, propagation delay - Power, energy consumption and power-delay, energy-delay products - Layout considerations/design rules	6
3.	**CMOS Combinational Circuits** - Implementation styles Static, ratioed, pass transistor, CPL, dynamic logic - Signal integrity issues in dynamic circuits - Cascading of dynamic circuits - Logic styles for low power & high performance applications	6
4.	**CMOS Sequential Circuit** - Timing metrics for sequential circuits - Static and dynamic sequential flip-flops and latches - High speed pipeline circuits	6
5.	**CMOS Arithmetic Circuits** - Single bit adder circuits - Multi-bit adder circuit and architecture - High speed adders	6

6. **Interconnect Parasitics** 3
   - Capacitive parasitics, modeling, cross talk
   - Resistive parasitics, modeling, IR drop, electromigration
   - Inductive parasitics,

7. **Timing Issues in Digital Circuits** 3
   - Single-phase and two-phase clocking
   - Clock skew and jitter
   - Clock generation and distribution
   - Synchronizers & arbiters

Total 36

Text Book: Digital Integrated Circuit: A Design Perspective, Jan Rabaey, A. Chandrakasan, and B. Nikolic, 2nd Edition, Printice Hall, ISBN 0-13-090996-3.

Project: A group IC design project is an essential component of this course. The project involves transistor-level digital circuit design, simulation and layout.