# E&CE 730- Topic 16
# Embedded Semiconductor Memories

## Calendar Description:

Static and dynamic behavior of MOS transistor short channel effects and scaling trends. Memory architectures and building blocks. SRAM, DRAM, and CAM cell design and analysis. Low-power, low-voltage circuit techniques. Memory yield, redundancy and reliability issues.

**Prerequisite:** ECE 445 or equivalent course
*Project

## Detailed Description:

| | | Lecture hours |
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| 1. | **MOS Transistor & Inverter Review**<br>- Static behavior<br>- Parasitic capacitances and dynamic behavior<br>- Short channel effects<br>- Scaling concept | 6 |
| 2. | **Static Random Access Memory Circuits – I**<br>- Architecture and building blocks<br>- SRAM cell designs and analysis<br>- Peripheral circuits – address decoders, sense amplifiers, pre-charge & equalize | 8 |
| 3. | **Static Random Access Memory Circuits – II**<br>- Variability and SRAM circuits<br>- Low-Voltage, Low-Power SRAMs<br>- Parasitics and Timing Design<br>- Robust circuit design | 8 |
| 4. | **Dynamic Random Access Memory & Content Addressable Memories**<br>- DRAM circuits – cells, sense amplifiers, Timing and control<br>- CAM cell design<br>- Peripheral circuits – matchline sensing, Priority encoder | 6 |
| 5. | **Memory Test and Reliability**<br>- Defects in manufacturing<br>- Memory fault models and test algorithms<br>- Soft errors in memories<br>- Redundancy, Repair and Yield | 8 |
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| | Total | 36 |

**References:**

(i) Lecture Notes
(ii) A. Pavlov, and M. Sachdev, CMOS SRAM – Circuit Design and Parametric Test in Nano-scaled Technologies, Springer, ISBN 978-1-4020-8362-4

(iii) J. Rabaey et. al., “Digital Integrated Circuits: A Design Perspective, 2nd edition, Prentice Hall, 2003, ISBN 0-13-090996-3

**Project:** An individual project is an essential component of this course.