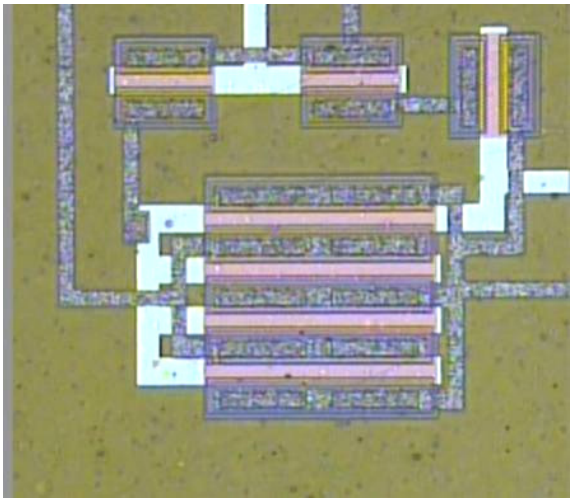
Research Review
2002-2005



Instability compensated AMOLED pixel circuit on plastic

Amorphous Silicon Device & Integrated Circuit (α-SiDIC) Group

Electrical & Computer Engineering

University of Waterloo

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Preface

This report reviews the research activities of the Amorphous Silicon Devices and Integrated Circuits (α-SiDIC) group in the period 2002-2005.

The group continues to enjoy significant growth in terms of personnel, number of projects, and laboratory infrastructure. The diversity of research projects has expanded, along with offerings of several new advanced level courses in large area electronics, ranging from electronic materials and processing to devices and integration. Major project areas include thin film transistor integration on rigid and flexible substrates, including fabrication of novel device structures, active matrix backplanes for organic light emitting diode (OLED) displays, biomedical x-ray imaging and photon counting, and photovoltaics, including flexible solar cells. Construction of the new device fabrication laboratory is now complete and installation of new state-of-the-art tools and relocation of existing equipment is currently underway.

The group has worked extremely hard over the last 2-3 year period coping with construction of the new lab, equipment installation, and new projects. We are very pleased with the outcome in terms of quality of results and intellectual property generation in a number of areas related to large area electronics. Over this period we received two best paper awards: 2002/2003 IEE Institution Premium Award for Best Paper in Devices, Circuits, and Systems (for TFT integration on glass and plastic) and the Michael B. Merickel Award in Medical Imaging 2001 (for active pixel sensors in digital fluoroscopy). A. Nathan was awarded the NSERC E.W.R. Steacie Fellowship and the Canada Research Chair in 2001 and 2004, respectively. PhD students Karim S. Karim and Peyman Servati received NSERC Doctoral Prizes in 2003 and 2004, respectively, and Anil Kumar, Flora Li, and Kapil Sakariya were awarded the 2004 CITO Research Excellence Scholarship. Anil and Kapil also received the 2004 Martin Walmsley Fellowship for Technological Entrepreneurship.

We gratefully acknowledge the support of our research sponsors and the commitment of the University towards this initiative, and look forward to the exciting times ahead! Special thanks goes to Dr. Peyman Servati and Jeff Chang who edited this Research Review.

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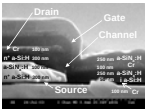
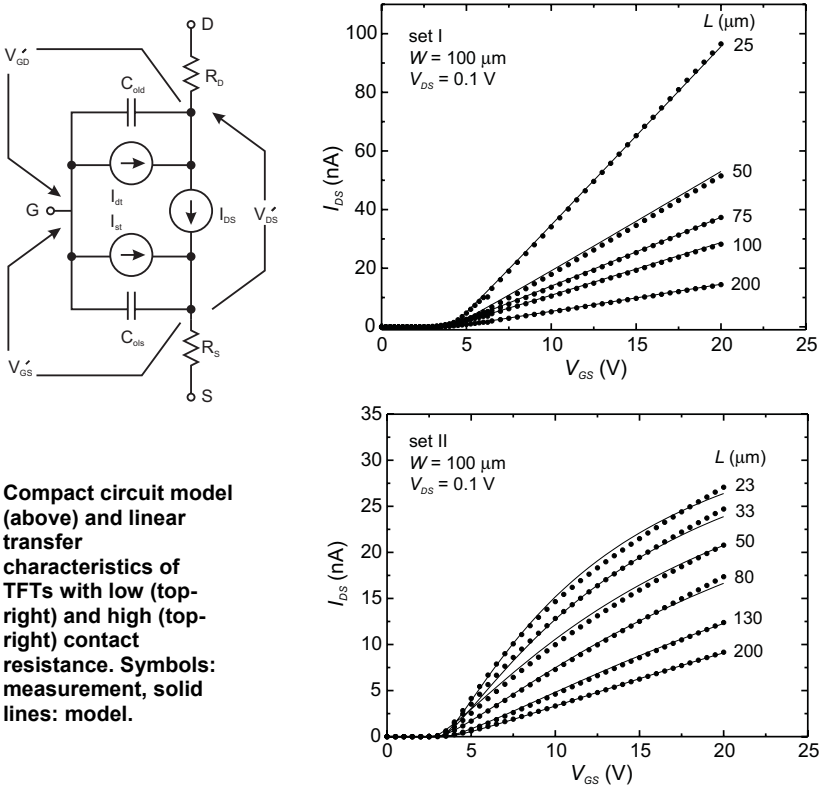
1 Thin Film Transistors



1.1 TFT Compact Modeling and Parameter Extraction

The growing demand for TFT backplanes with complex analog functions on rigid and flexible substrates necessitates compact, yet accurate, models for TFT operation. Such models not only facilitate computer-aided design (CAD) of pixel circuits but can also be used to examine process conditions for improving device performance. Here, parameter extraction methods that can relate device characteristics to physical material properties are critical. We have developed compact models and associated extraction techniques that include impact of non-idealities such as contact resistance and interface properties. For instance as seen in the figure below, contact resistance directly impacts the linear transfer *I-V* characteristics that are commonly used for extraction of field effect mobility μ_{FE}. We have systematically examined the influence of contact resistance on device parameters such as μ_{FE}, since it can vary by orders of magnitude due to process variations. The models are implemented in VerilogA hardware description language, which comes as a standard feature in most circuit simulation environments, and can be used for CAD of pixel circuits.

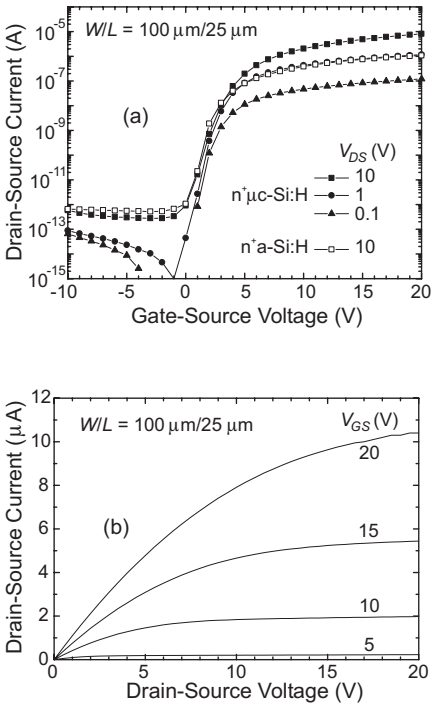


Compact circuit model (above) and linear transfer characteristics of TFTs with low (top-right) and high (top-right) contact resistance. Symbols: measurement, solid lines: model.

1.2 Highly Doped Microcrystalline Silicon for TFT Contact Layers

Compared to its amorphous counterpart, highly doped microcrystalline silicon (n^+μc-Si:H) is attractive due to its much higher conductivity and doping efficiency. As a result, n^+μc-Si:H films provide better quality contacts in a-Si:H TFTs. In our laboratory, we prepared n^+μc-Si:H films using conventional RF 13.56 MHz PECVD in a multi-chamber deposition system. High conductivity (25 $\Omega^{-1}cm^{-1}$) and high crystallinity (66 %) for 50 nm n^+μc-Si:H films were achieved with 99.6 % H_2 dilution of SiH_4 and 10 W RF power.

The figures depict transfer and output current-voltage character-istics of a TFT with the n^+μc-Si:H ohmic contact layer. The TFT shows a device mobility of 0.9 cm^2/Vs, a threshold voltage of ~3V, an ON/OFF current ratio of above 10^7, a subthreshold slope of 0.5 V/dec, and a leakage current of the order of 10^{-13} A. In addition, no evidence of current crowding at low drain-source voltages is observed, which implies that the n^+μc-Si:H ohmic contact seems to be very effective, not only in blocking the hole leakage current at negative gate voltages, but also in reducing the source and drain contact resistances. Note that the ON current of TFTs is improved by a factor of ~5 compared to TFTs with n^+a-Si:H contacts. In addition, we believe that atomic H radicals and/or ions in our high H_2 dilution process conditions for n^+μc-Si:H films serve to remove contaminants, including the native oxide and any other process residues from the a-Si:H surface.

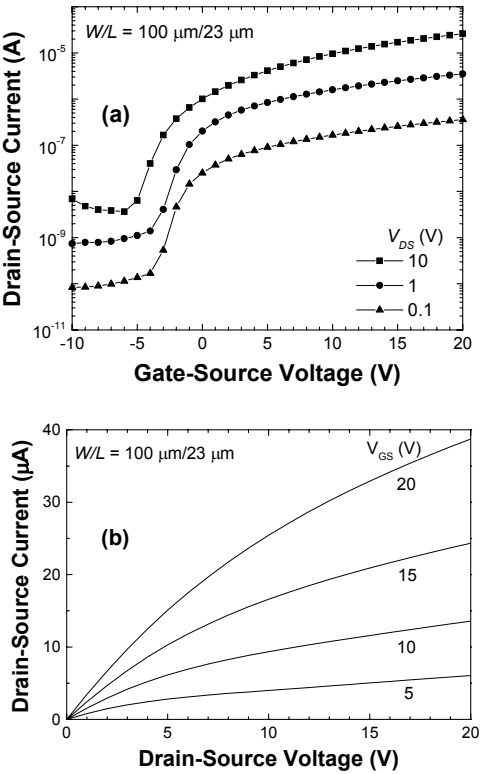


Transfer (top) and output (bottom) current-voltage characteristics of n^+μc-Si:H contact TFT.

1.3 Bottom-Gate Microcrystalline Silicon TFTs

Microcrystalline silicon (μc-Si:H) has gained significant importance in large area electronics as an alternative to a-Si:H due to its higher carrier mobility and higher stability. Indeed, the μc-Si:H TFT is expected to deliver far better performance than its amorphous counterpart. However, the small grain size (a few tens of nm), and poor quality at grain boundaries at low thicknesses, are obstacles in achieving device grade μc-Si:H films for high performance TFTs. In our laboratory, undoped μc-Si:H films were prepared using conventional RF 13.56 MHz PECVD in a commercial multi-chamber system. A 80 nm undoped μc-Si:H film for use as a channel layer in TFTs showed a dark conductivity of 10^7 S/cm and a crystalline volume fraction of 80%. Here, we have used bottom-gate inverted structure because it is widely used in pixelated arrays.

Figures show the transfer and output current-voltage (*I-V*) characteristics, respectively, of a μc-Si:H TFT. The μc-Si:H TFT shows a field effect mobility of 2.5 cm^2/Vs and a threshold voltage of 1.6 V. Interestingly, the field effect mobility is a factor of 2-3 higher than that of a-Si:H TFTs. However, the ON/OFF current ratio (~10^4) is low compared to a typical a-Si:H TFT. The reasons for the high OFF current are believed to be due to the defect states at the grain boundaries in the channel material. But, the μc-Si:H TFT has a high ON current of around 40 μA (at V_{DS} = V_{GS} = 20 V), compared to that of the a-Si:H TFT (~10 μA), with no visible signs of current crowding.

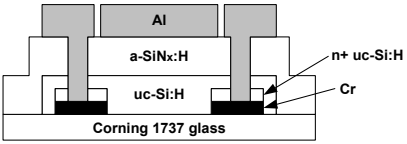


Transfer (top) and output (bottom) current-voltage characteristics of a bottom-gate inverted μc-Si:H TFT.

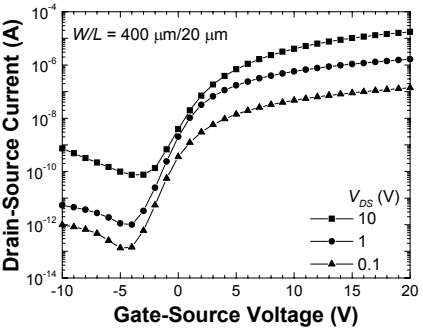
1.4 Top-Gate TFTs

Top-gate μc-Si:H TFTs have been demonstrated to have high mobility and more importantly, CMOS capability. However, most research results published to date have been obtained using non-standard deposition techniques. Fabrication of top-gate μc-Si:H TFTs is still a challenging task using a standard PECVD technique. Here, we show preliminary results of top-gate μc-Si:H TFTs fabricated at 250ºC using standard 13.56 MHz PECVD system.

The cross section of a fabricated top-gate TFT is shown on the right. Here, we used a 80 nm μc-Si:H as a channel layer and a 300 nm a-SiN_x:H as a gate dielectric. The transfer *I-V* characteristics of a top-gate staggered μc-Si:H TFT is also illustrated. The field effect mobility is 0.6 cm^2/Vs, which is similar to that of a-Si:H TFTs. The threshold voltage and subthreshold slope are around 4.4 V and 1.4 V/decade, respectively. The ON-current in the TFTs is generally determined by the channel layer (≤ 20 nm) at the uppermost part of the μc-Si:H, near the a-SiN_x:H interface. It is therefore assumed that this low mobility results from plasma damage to the interface between the μc-Si:H channel and a-SiN_x:H gate dielectric during the initial a-SiN_x:H deposition. On the other hand, the TFTs show a high ON/OFF current ratio of ~10^6. In our TFTs, the OFF-current is 1.3×10^{-13} A (3.25×10^{16} A/μm) and 7.4×10^{-11} A (1.85×10^{13} A/μm) at drain-source voltage of 0.1 and 10 V, respectively. Such low OFF current values indicate low defect and impurity levels in the μc-Si:H channel layer.



Schematic cross section of a fabricated top-gate staggered μc-Si:H TFT.



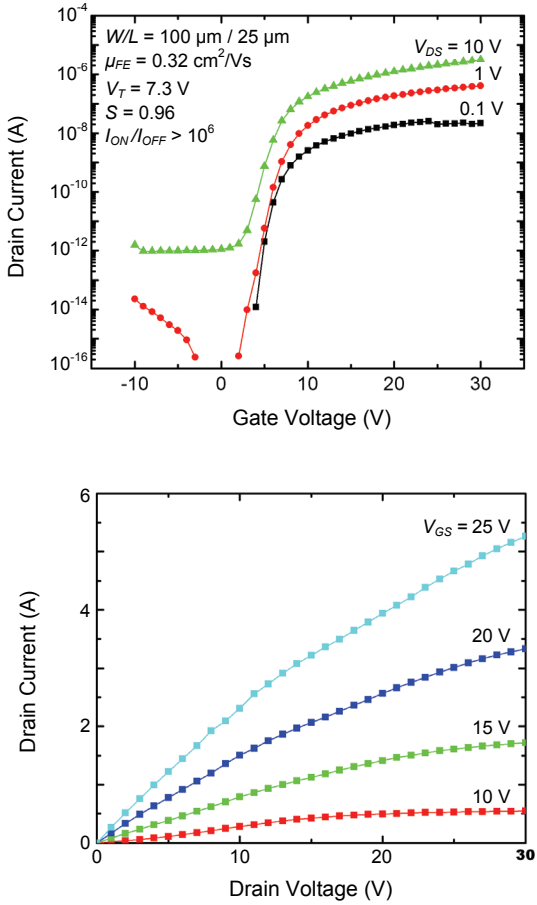
Transfer characteristics of a top-gate staggered μc-Si:H TFT.

1.5 Nanocrystalline Silicon TFTs

The nanocrystalline silicon (nc-Si:H) TFT is a promising alternative to the amorphous silicon (a-Si:H) TFT as it offers increased mobility and improved stability.

We fabricated bottom-gate TFTs using pulsed PECVD in collaboration with MVSystems Inc. Pulsed PECVD can produce material at a higher growth rate, and reduced powder particle formation. The bottom-gate process is a standard process and was used to provide a direct comparison with a-Si:H bottom-gate TFTs.

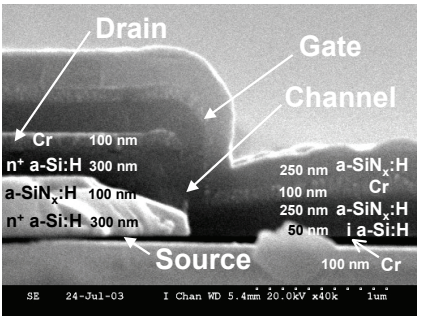
The first trial of these TFTs shows performance on par with a-Si:H transistors as seen in the figure. Further optimization of this material and the fabrication process is necessary to improve the extracted parameters.



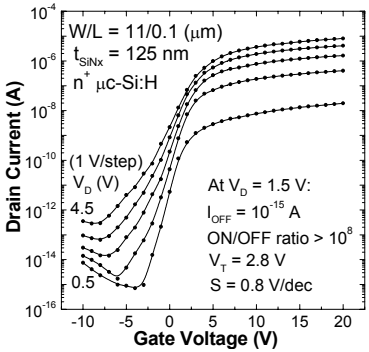
Transfer (top) and ouput (bottom) *I-V* characteristics of nc-Si:H TFTs.

1.6 Vertical Thin Film Transistors

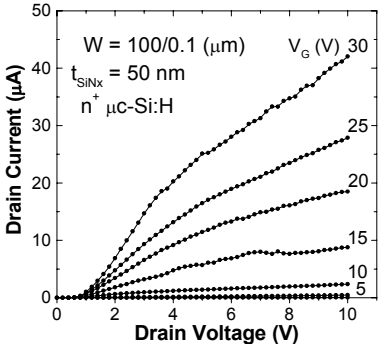
The vertical thin film transistor (VTFT) is attractive for realization of short-channel TFTs since it is not constrained by lithography. Here, the channel length is defined by the drain-source insulator thickness. We have developed a 0.1-μm channel length a-Si:H VTFT process using standard 5- to 10-μm lithography. This is the shortest channel TFT ever reported. The device has an ON/OFF current ratio of more than 10^8 which compares with lateral TFTs. However, its parasitic overlap capacitance is orders of magnitude smaller and is less than 50 fF.



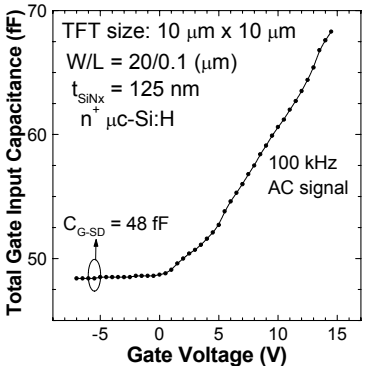
Cross-section of 0.1-μm VTFT.



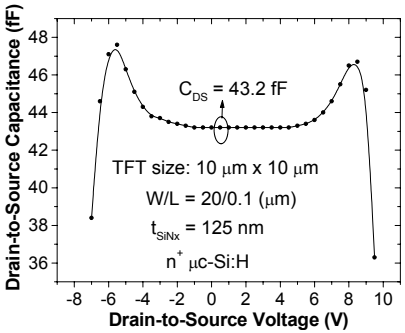
Transfer characteristics.



Output characteristics.



Gate-input C-V characteristics.



Drain-to-source C-V characteristics

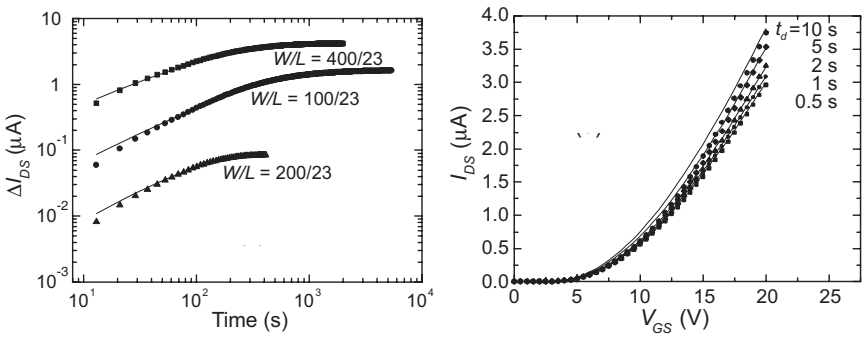
1.7 Bias-Induced Long Term Transient in Amorphous Silicon TFTs

In this work, we investigate and model the anomalous transient increase of the TFT drain current in a time scale (of the order of hundreds of seconds) where the threshold voltage shift is not prominent. Such a long term transient in the terminal characteristics can be critical for analog applications of the TFT. We believe the mechanism responsible for such behaviour is a configurational relaxation of Si dangling bond defects following change in their charge states. Based on the defect relaxation mechanism, we have proposed a time dependent drain current model to predict the transient response of the TFT in the forward above threshold regime of operation. The parameters associated with the model are physically based and have strong dependence on the TFT geometry. The measurement data are in good agreement (see Fig. below) with simulation results with a discrepancy of less than 5%.

According to the model, the drain current increase can be written as,

$$\Delta I_{DS}(t) = \mu_{FE}\zeta C_i^{\alpha-2}\frac{W}{L}(V_{GS}-V_{Ti})^{\alpha-1}Q_{deep}(0)\left[1-\exp\left(-(t/\tau)^{\beta}\right)\right]x_{cm}$$

where V_{Ti} is the initial threshold voltage, $Q_{deep}(0)$ is the initial trapped charge per unit area, τ is the relaxation time, β is a constant such that $\beta < 1$, and other parameters bear their usual meaning.



Modeling of the long term transient: increase in drain current with time under constant drain and gate bias (V_{DS} = V_{GS} = 20 V) (left) and (b) transfer characteristics with different delay time t_d (right). Symbols: measurement data; solid lines: simulation.

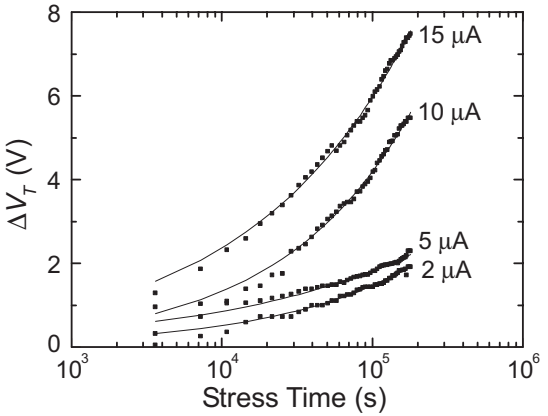
1.8 Constant Current Stress Metastability of Amorphous Silicon TFTs

Amorphous silicon (a-Si:H) active matrix organic light emitting diode (AMOLED) pixel circuits use the current mirror topology to compensate for threshold voltage shift (ΔV_T). In these circuits, the driver TFTs are subjected to constant current stress. In order to predict the performance and lifetime of these pixel circuits, ΔV_T of the driver TFT under constant current stress needs to be modeled. In this work, we have investigated the ΔV_T of inverted staggered a-Si:H TFTs under various levels of current stress (2 μA to 20 μA) for 50 hours, at both room and elevated (75˚C) temperatures. We have proposed a model for the ΔV_T under constant current stress where the shift in V_T follows a power law with time:

$$\Delta V_T = \frac{\left(\frac{I_{DS}}{K}\right)^{\frac{1}{\alpha}}}{1+\frac{1}{\alpha}}\left(\frac{t}{t_o}\right)^{\beta}$$

Here, I_{DS} is the stress current, K a constant for a given TFT size and fabrication process, α the power parameter in the drain current equation of a-Si:H TFT, t_o the characteristic trapping time of carriers and β the power parameter.

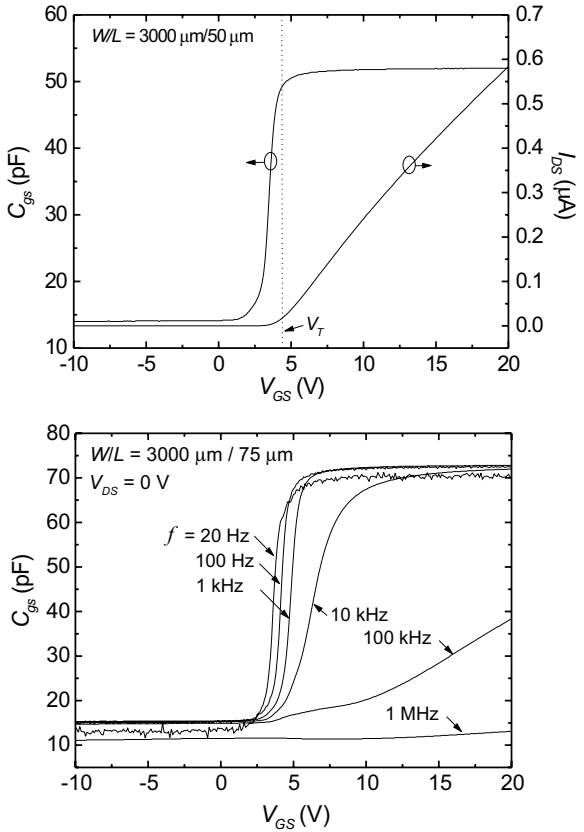
The model shows good agreement with the measurement data.



Threshold voltage shift as a function of time for different stress currents at room temperature. symbols: measurement data; solid line: model.

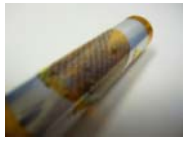
1.9 TFT Dynamic Modeling

The intrinsically low carrier mobility and the high overlap capacitance of TFTs lead to slow transients in these devices. We have developed accurate capacitive models for TFTs that include different charge components such as trapped carriers in tail and deep states, trapped carriers at interfacial states, and free carriers. The model is capable of predicting the switching behaviour of device capacitance (see figure below) when the gate voltage increases from negative to positive voltages. Due to the presence of deep and interfacial states, the increase in capacitance precedes the current rise. In addition, the change in channel charge with drain bias in linear and saturation regimes must be taken into account. Capacitance-voltage characteristics are measured at different frequencies to investigate the device frequency response and the role of different charge components on the transient behaviour.



Measurement results for capacitance-voltage (and comparison to current-voltage characteristics) (top) and capacitance-voltage-frequency measurements (bottom).

2 Flexible Electronics

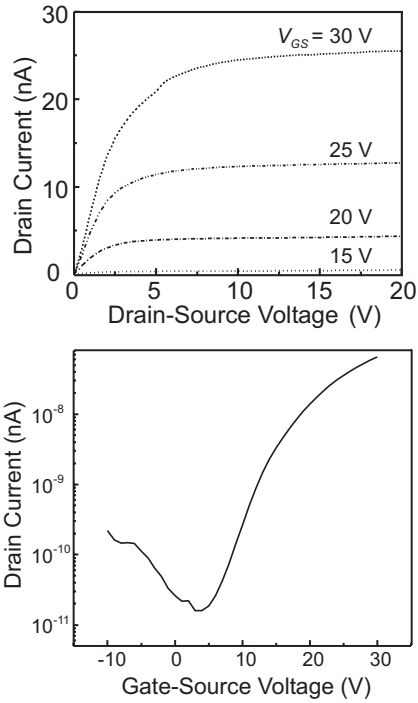


2.1 Low Temperature Amorphous Silicon Nitride

Fabrication of TFTs on flexible plastic substrates for large-area imagers and displays has been made possible by lowering the deposition temperature, which reduces the thermal deformation of plastic substrate; and greatly facilitates substrate preparation and device patterning. Furthermore, at extremely low deposition temperatures, a much wider variety of low-cost substrates, plastics or otherwise, are available for integration.

Low-temperature amorphous silicon nitride (a-SiN_x) films have been optimized for low current leakage, with the application of TFTs on plastics in mind. The optimal film had a resistivity of ~10^{16} cm, breakdown strength of ~10 MV/cm, low hydrogen content (17 at.%), and was N-rich ([N]/[Si] ~ 1.56).

TFTs were fabricated, and the desired low leakage through the a-SiN_x gate dielectric was observed. A W/L=100/25 TFT has an I_{off} current below 10^{-11} A for a source-drain voltage as high as 10 V.



Output (top) and transfer (bottom) characteristics of 75°C TFT with *W*/*L*=100/25 µm.

2.2 Low Temperature Amorphous Silicon Oxide

The aim of this research is to develop low temperature gate dielectric/passivation dielectric for μc-Si and poly-Si based devices and circuits compatible with plastic substrates.

PECVD amorphous silicon oxide (SiO_x) films were fabricated by conventional 13.56 MHz glow discharge decomposition of silane and nitrous oxide mixture at 75ºC, 120ºC and 250ºC using an industrial parallel plate reactor (Plasma Therm 790 series). Helium, nitrogen and argon were used as diluent gases.

Chemical composition and bonding in the films were studied by FTIR spectroscopy. The absorption peak at 1075-1080 cm^{-1} observed in the spectrum of each film corresponds to SiO_2 stretching mode. No presence of SiH stretching or NH-stretching vibrations was found in the FTIR spectra of the samples.

Film uniformity was varied from 2% to 6% for 6"x6" area. The deposited films have compressive stress that varied from 0.063 GPa to 0.117 GPa. The respective film density is in the range 1.35 g/cm^3 to 1.69 g/cm^3.

The electronic properties were studied using MOS capacitors with 200 nm thick SiO_x. The dielectric permittivity was in the range 2.03 and 3.57. A dielectric breakdown at 9 MV/cm was observed for the films deposited at 120ºC. The films deposited at higher temperatures were characterized by a lower leakage current density; $3.7x10^{-10}$ A/cm^2 for the sample deposited at 250ºC, $9x10^{-9}$ A/cm^2 for 120ºC, and $2.2x10^{-8}$ A/cm^2 for 75ºC at 5 MV/cm.

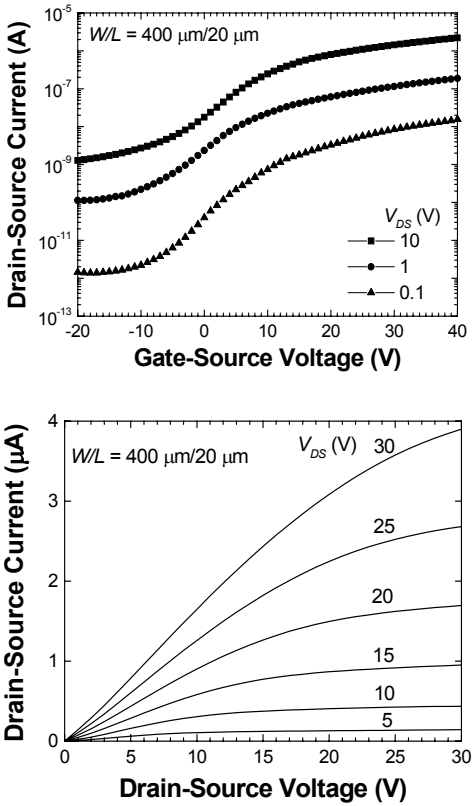
a-Si:H based TFTs were fabricated using the low temperature oxide as gate dielectric. The TFTs demonstrate threshold voltage (3.02-4.12 V) and mobility (0.12-0.59 cm^2/Vs).

Parameters of 75ºC TFTs

L (μm)	I_{on} (nA)	V_T (V)	S (V/dec)	μ (cm^2/Vs)	I_{on}/I_{off}
25	87.6	3.36	2.28	0.120	$8.99x10^2$
75	61.4	4.12	1.31	0.487	$5.47x10^2$
100	87.3	3.95	1.27	0.589	$1.43x10^3$
200	36.2	3.02	1.03	0.593	4.62

2.3 75°C Nanocrystalline Silicon TFT

Nanocrystalline silicon (nc-Si:H) films can be deposited on flexible, lightweight, unbreakable, and inexpensive plastic substrates at low temperatures (~150°C) without degrading its intrinsic material properties. This enables realization of high mobility TFTs and possibly peripheral driver circuitry for fully flexible active-matrix organic light emitting displays (AMOLEDs). In this work, intrinsic and n^+ nc-Si:H films were deposited using conventional RF 13.56 MHz PECVD in a single chamber system at very low temperature (75°C). Optimized films were achieved at a moderate RF power density regime (~100 mW/cm^2) with a growth rate of 3–4 nm/min. The 80-100 nm intrinsic and n^+ nc-Si:H films show a dark conductivity of about 10^{-7} S/cm and 0.3 S/cm, respectively, and a corres-ponding crystallinity of around 80% and 72%. Top-gate staggered TFTs fabricated using the optimized intrinsic and n^+ nc-Si:H films as channel layers and ohmic contacts, show a field effect mob-ility of 0.026 cm^2/Vs, a threshold voltage of 3 V, and an ON/OFF current ratio of ~ 10^4 (see Figs.). The high subthreshold slope observed can be attributed to poor inter-face integrity between the nc-Si:H channel and a-SiN:H gate dielectric. Nevertheless, the results demonstrate the feasibility of very low temperature TFTs and the need for further research to improve material and device performance.

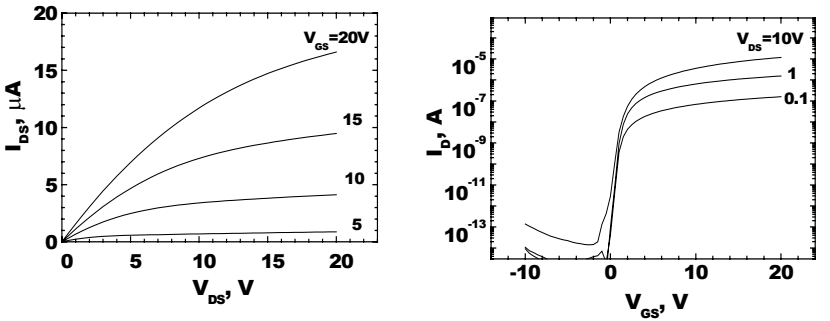


Transfer (top) and output (bottom) characteristics of nc-Si:H TFT.

2.4 High Performance Amorphous Silicon TFTs on Plastic Substrates

High ON-current capability for a-Si TFTs is important for applications such as AMOLED displays. It's required for both high light output from the display and long-term stability of operation. In flexible displays with a-Si active matrix, good performance of transistors has to be achieved with a very limited thermal budget of the fabrication process.

Deposition regimes for TFT layers have been optimized for the process temperature of 150ºC, which is compatible to a broad range of plastic substrate materials including, polyimide, PES, PEN and others. The a-Si TFTs shown here were fabricated on polyimide foils. The process dependent TFT performance parameters are listed in the table. As seen, the characteristics of devices on plastic are as good as high quality TFTs on glass fabricated at 300ºC.



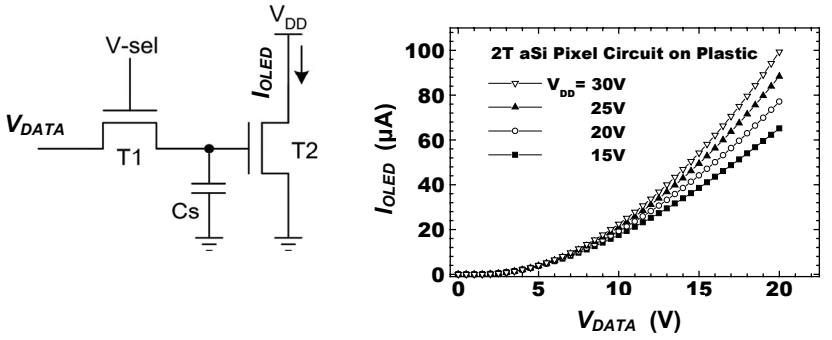
Output (left) and transfer (right) characteristics of a-Si TFT on plastic substrate.

Performance parameters of a-Si TFTs on glass and plastic substrates.

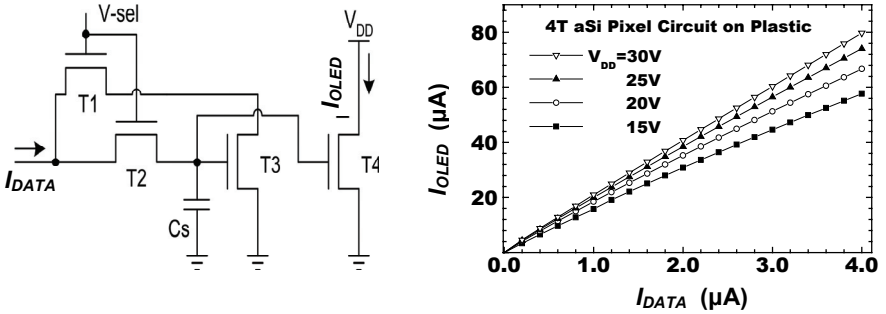
Parameters	300ºC process (glass)	150ºC process (plastic)
Threshold voltage V_T (V)	2.3-2.5	2.5-3.5
Field-effect mobility μ_{eff} (cm^2/Vs)	1.1-1.2	1.0-1.2
Contact resistance $R_{SD}.W$ (MΩ·mm)	2-5	3-10
Subthreshold slope S (V/dec)	~0.3	~0.3
OFF current I_{OFF} (A)	$\sim 10^{-14}$	$\leq 10^{-13}$
ON/OFF ratio	$\sim 10^{9}$	10^{8}-10^{9}

2.5 Voltage- and Current-Programmed Pixel Driver Circuits on Plastic for AMOLED Displays

Various TFT pixel circuits have been fabricated on plastic substrates using the new 150ºC a-Si TFT process. Schematic representation and characteristics of voltage-programmed 2T-circuit and current programmed 4T circuit are shown below. High output current, broad dynamic range and good drive current control have been achieved for both voltage-programmed and current programmed pixel circuits.



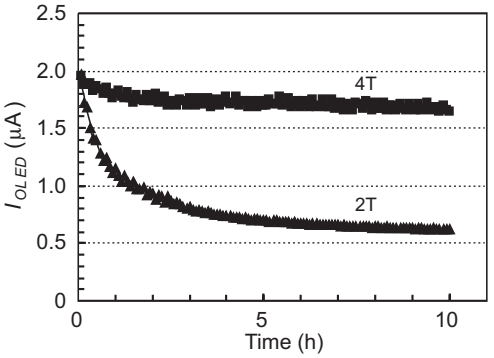
Schematic photomicrograph, and input-output characteristics of 2T OLED pixel circuit on plastic substrate.



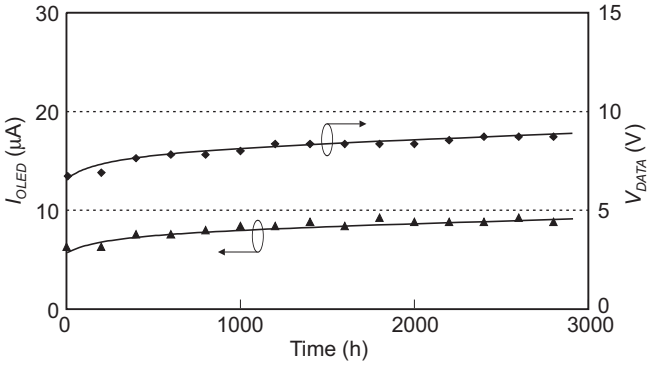
Schematic photomicrograph and input-output characteristics of 4T OLED pixel circuit on plastic substrate.

2.6 Stability of Amorphous Silicon Pixel Driver Circuits on Polyimide Foils

A comparison of the behaviour of drive current in a-Si 2T and 4T pixel circuits on polyimide foils demonstrates the advantage of 4T current-driven circuit, which compensates for threshold voltage shift in the drive TFT. Long term operational stability of 4T circuit under higher current load shows that after 3000 hrs of operation, the input-node voltage is still quite low, which means the life-time of the circuit far exceeds 3000 hrs.



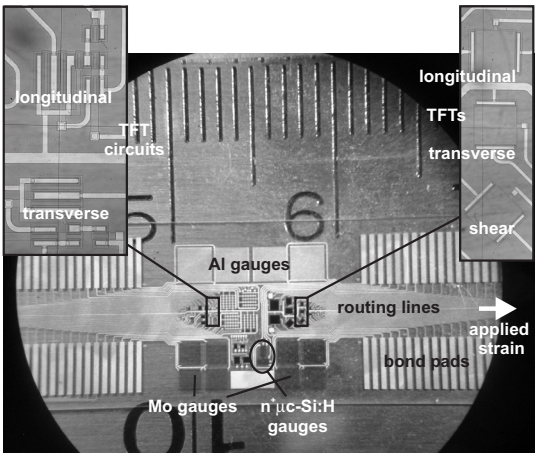
Change in OLED current in 2T and 4T circuits on plastic over 10 hours of operation.

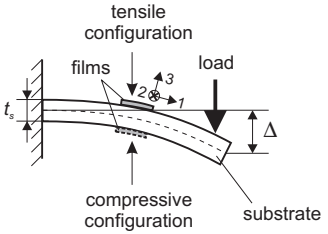


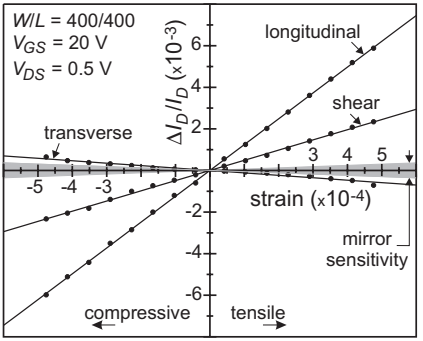
Change in OLED current and input-node voltage for 4T circuit over 3000 hours of operation.

2.7 Mechanically Strained TFTs

Aside from technological challenges associated with fabrication of TFTs on flexible substrates, stable electrical operation of TFT circuits under mechanical stress induced by substrate bending is imperative. The induced tensile or compressive stress modifies device parameters such as field effect mobility and thus leads to shifts in current. To examine the shifts in current we performed beam deflection experiments in both tensile and compressive configurations (see figure below) on a-Si:H TFTs and TFT circuits. In situ strain gauges were included in the sample for monitoring the strain longitudinal and transverse strain components. The shifts in current are observed to be dependent on the current orientation with respect to the direction of the applied strain. The longitudinal TFTs experience the highest shifts, while the transverse ones had the lowest. The 4T circuit included in the sample showed suppressed sensitivity to the applied strain due to its current mirror architecture. As a result, this circuit can provide immunity to bending induced stress in flexible AMOLED displays.



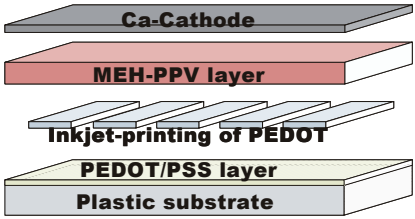




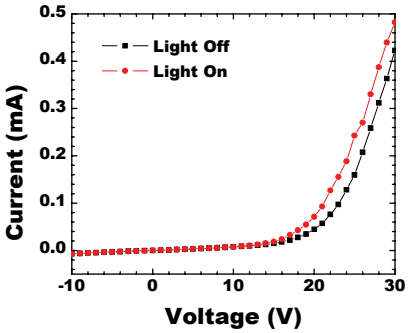
Photomicrograph of sample (top), and TFT and mirror current shifts under mechanical stress induced by beam deflection technique (bottom).

2.8 Patterning Techniques for Fabrication of Polymer Electronics

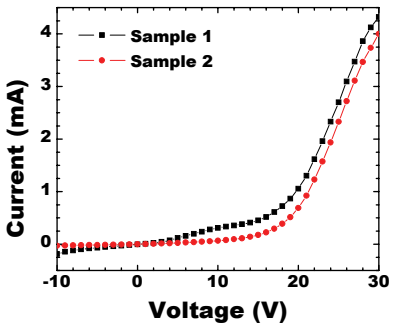
Inkjet printing has been evaluated as a very viable patterning technique for the fabrication of low-cost organic thin-film electronics on flexible substrates. On the other hand, plotting, which is a very promising alternative for some application, has been demonstrated for the first time in our laboratory. The plotting technique is simple and convenient, and the desktop plotter hardware is able to handle a broad range of solvents for polymers. There are no issues with clogging of nozzles or other parts of the hardware. Polymeric thin films deposited/ patterned by the plotter are continuous and homogenous. Unlike inkjet printers, desktop plotters do not impose topological constraints on the substrate and thus can handle a variety of substrates, including glass and plastic. Polymer light emitting diodes (PLEDs) have been fabricated from inkjet printing and from plotting. Although inkjet printing offers relatively small feature sizes and currently meets the resolution requirements for high information content displays, the plotting technology is favourable in other application areas (e.g., electronic labelling) where resolution requirements are less stringent.



Cross section of PLED.



Current-voltage characteristics of inkjet-printed PLED.

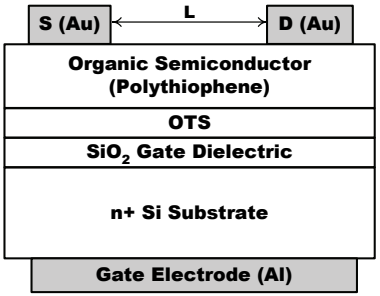


Current-voltage characteristics of two plotted PLEDs.

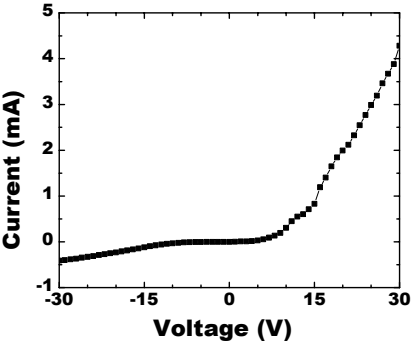
2.9 Organic TFT Materials and Interfaces

Preliminary experiments on solution-processible organic thin film transistors (OTFTs) considered polythiophene as the active semiconducting layer (see cross-sectional structure below). Octadecyltrichlorosilane (OTS, CH_3-$(CH_2)_{17}$-$SiCl_3$) self-assembly monolayer (SAM) is used as the surface treatment agent for the gate dielectric (SiO_2) prior to polymer deposition. Optimization of the deposition parameters reveals that good-quality uniform OTS layer on SiO_2 can be obtained at ambient (non-vacuum) conditions by immersion under sonication. Regioregular and regiorandom polythiophene in chloroform are spin-coated on OTS-treated oxidized silicon substrate and on glass substrate. The film properties are evaluated using SEM and with electrical measurements. Regiorandom polythiophene on OTS-treated SiO_2 surface exhibits conductivities in the range of $1.13 \times 10^{-3}\ \Omega^{-1}\ cm^{-1}$. However, the Au-polythiophene contact shows Schottky barrier characteristics (see characteristics below).

Top-contact OTFT structures on oxidized and nitrided silicon, glass and plastic wafers are currently being investigated along with other surface treatment agents (e.g., TX-100, HDMS, high molecular weight silanes) in combination with different solution-deposited organic semiconductors.



Cross section of top-contact OTFT.



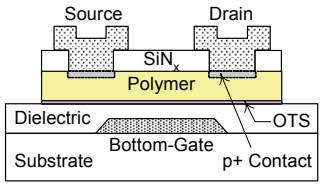
Current-voltage characteristics of regio-random polythiophene spin-coated on OTS-treated SiO_2 surfaces with gold contacts.

2.10 Organic TFT Architectures

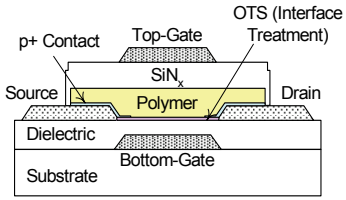
Research in organic thin film transistors (OTFTs) is gaining momentum in recent years because of the numerous features that are attractive for potentially low-cost applications in large-area displays, flexible electronics, smart cards, and sensors. To properly characterize the properties of organic semiconductor materials and develop functional organic devices, different OTFT structures and circuits are being designed and fabricated in our laboratory. OTFT architectures that are currently under investigation include the top-gate, bottom-gate, and dual-gate configurations. Polythiophene is used as the organic semiconductor layer, and different material systems are examined. We consider, for example, SiO_2, SiN_x, and organic dielectric materials for the gate dielectric; Au, Al, Cr, ITO, and Mo for the electrodes/contacts; and glass, plastic, Si and oxidized-Si wafers for the substrate. Fabrication and measurements are performed in atmospheric conditions. A customized lithography process has been developed to fabricate high resolution OTFT test structures, and preliminary devices demonstrate promising results.

The systematic evaluation of OTFTs with various architectures and geometries provide an effective means to study the organic material properties, gain insight into the transport mechanism, characterize the density of states at the interfaces, so as to comprehend the physics and operation of OTFTs. Present design challenges for high performance OTFTs include optimization of the organic-dielectric interface using proper interface treatment techniques, development of highly-doped contact layers to reduce contact resistance, and examination of passivation and encapsulation strategies to address issues related to material degradation.

Our research concentrates on the fabrication of simple OTFT circuits, including inverter, oscillator, current mirror/source, amplifier, and driver circuit. The underlying objective is to develop functional OTFT devices that are suitable for circuit integration applications in active-matrix displays and imagers, and in other low-cost, flexible, and large area organic electronics.

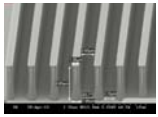


Bottom-gate OTFT.



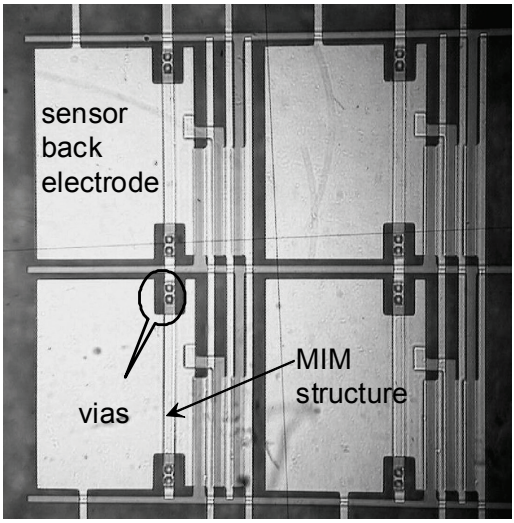
Dual-gate OTFT.

3 Process Integration



3.1 Low-k Dielectrics

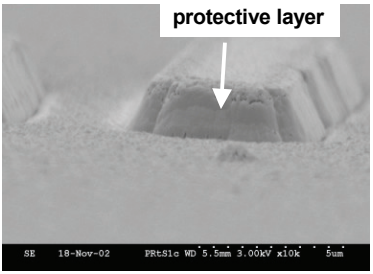
For improved image quality with active matrix TFT-based imaging arrays, it is important to maintain a high fill factor i.e., the fraction of the pixel occupied by the image sensor. A high fill factor can be achieved using a vertical pixel architecture, where the sensor element is placed on the top of TFT backplane and is separated by a dielectric film. We have studied the properties of polymeric photosensitive benzocyclobutene (PBCB) dielectrics. It is an attractive spin-on material for applications as an inter-layer dielectric between transistor and sensor. This material can be patterned by simple photolithographic process, where it acts as a negative resist. Other advantages of PBCB films include: low curing temperature (<250°C), high degree of planarization (60-90%), and low stress (~25 MPa) compared to PECVD dielectric films. The processing of PBCB has been fine tuned to achieve a reliable via opening with proper sidewall angle for via hole metallization for good metal contact. Electrical measurements on test Me/PBCB/Me-structures showed low leakage current (~10^{-10}-10^{-9} A/cm^2), high dielectric strength (>2 MV/cm), and small via resistance (~2-3 Ω/via).



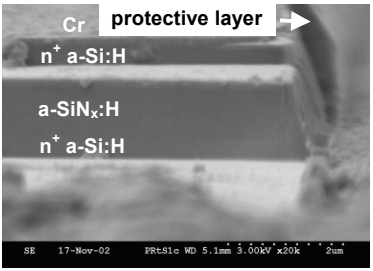
Top view of Al/low-k/Al array-like test structure fabricated on glass substrate.

3.2 Residue Removal in CF_4/H_2 Plasma Etching

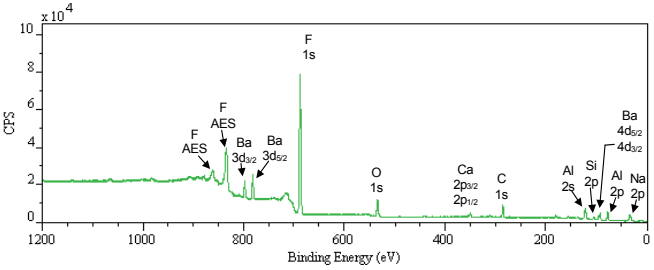
The formation of a sidewall-blocking layer in CF_4/H_2 plasma etching can secure a vertical etch profile, but this layer must be removed after etching. X-ray photoelectron spectroscopy (XPS) studies of this protective layer indicate that it consists of metallic fluoropolymer composites. The C 1s photoelectron emission line shows multiple peaks, which are identified to be CF_x bonding structures. After removal of the protective layer by an organic solvent, the C 1s line is shifted back to its elemental location. Cleaned n^+/nitride/n^+ structures have been demonstrated by sectioning. This cleaning step after dry etching is very critical for high performance devices, e.g., vertical thin film transistors.



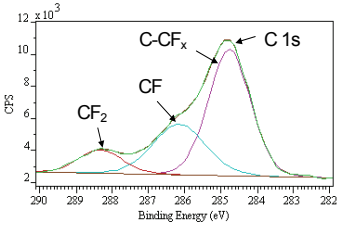
Sidewall protective layer formed after CF_4/H_2 plasma etching.



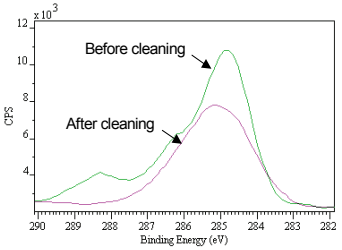
500 nm thick protective layer.



Chemical composition of protective layer.



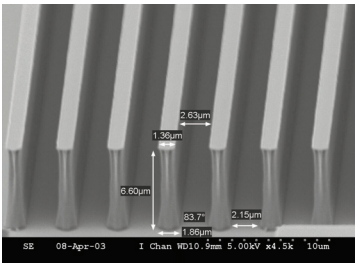
CF_x bonding of protective layer.



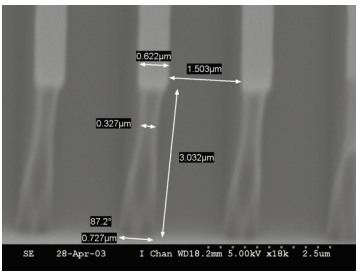
C 1s line before and after cleaning.

3.3 High Aspect-Ratio (AR) Photolithography

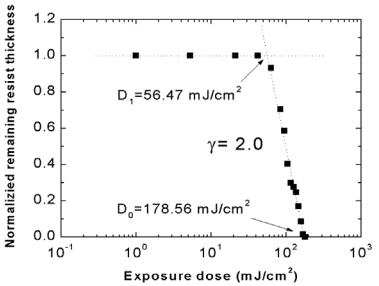
We have developed an optimized thick film photoresist process to compensate for issues such as step coverage, linewidth variations, and high dry etch resistance for a-Si:H devices, such as vertical thin film transistors (VTFTs) that have significant substrate topography (1 μm or higher). Using an e-beam chrome photomask, coupled with contact printing and precise process control, we were able to achieve 2 μm lines-and-spaces from a 6.6 μm resist (AR = 3.55) or 1 μm lines-and-spaces from a 3-μm resist (AR = 4.17) with profile angles larger than 84°. The critical steps in lithography are analyzed along with process models to describe their effects on the resist characteristics for reproducibility.



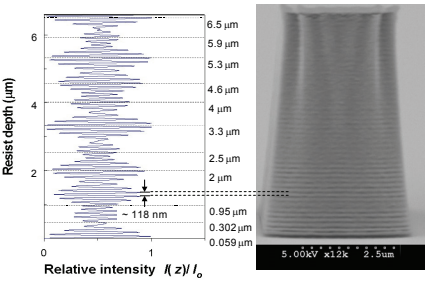
2 μm lines-and-spaces.



1 μm lines-and-spaces.



Positive resist contrast *γ* curve.



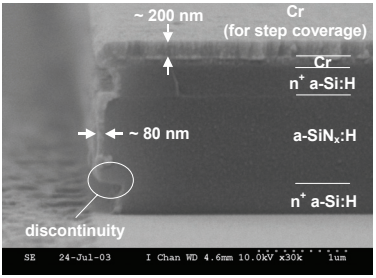
Resist standing wave profile.

Equation for resist standing wave profile after exposure/development steps:

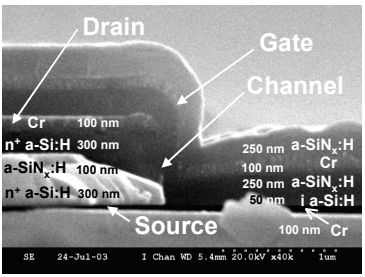
$$\frac{I(z)}{I_o} \approx \frac{1}{3}\left[\left(\sin(\frac{2\pi n}{\lambda_{g-line}}z)\right)^2 + \left(\sin(\frac{2\pi n}{\lambda_{h-line}}z)\right)^2 + \left(\sin(\frac{2\pi n}{\lambda_{i-line}}z)\right)^2\right]$$

3.4 Thin Film Deposition on Non-Planar Topographical Surfaces

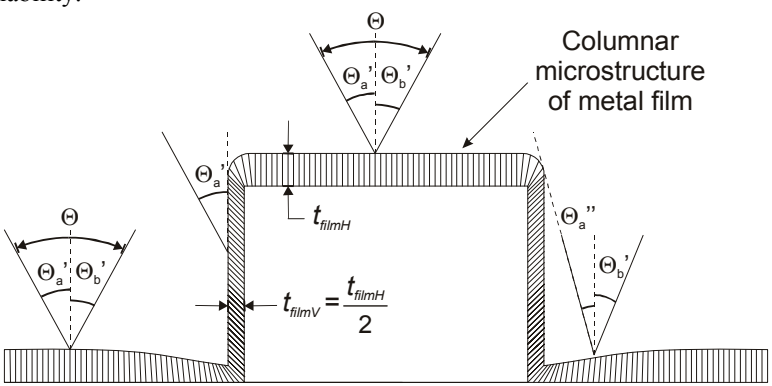
Substrate surfaces are rarely flat during most fabrication processes, but contain significant non-planarity in topography that is formed by various material patterns. Physical sputtering and PECVD techniques for thin film deposition are particularly sensitive to the substrate topography. Etched material profiles that are not well controlled can have a negative impact on the process reliability. It can be demonstrated that the thicknesses of thin films on a 90° vertical surface deposited by these techniques are approximately half that on the horizontal surface. The conformality of thin film step coverage is governed by the plasma-surface kinetics. The device fabrication process must be designed in accordance with the physical nature of these plasma processes to ensure process reliability.



Step coverage of sputter-deposited Cr film on a "zig-zag" profile.



Step coverage of sputter-deposited and PECVD films on a 90° step.

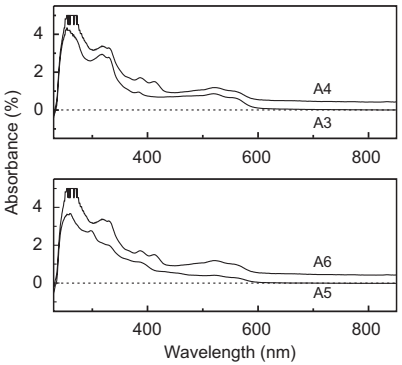


Sputtered metal flux and metal film coverage on a vertical step.

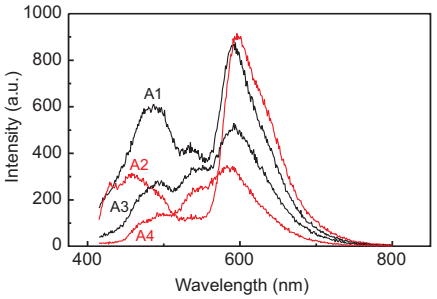
4 OLED Displays

4.1 Aacene-Anthracene Copolymers for Full Color OLED Displays

Solution processible copolymers based on acene-anthracene comonomeric units were synthesized for color organic light emitting diode (OLED) displays. All copolymers showed high processability and resistance to aerial oxidation. The color tuning in these polymers is achieved by controlling the molar ratios of reactants to oxidant during synthesis. Structural evaluation was done by SEM. Diffraction studies reveal the presence of 40% crystalline and 60% amorphous volume fracture within the copolymeric matrix. The electroluminescence (EL) efficiency varies with the anthracene concentration present along acene structure units.



UV-visible spectra of A3, A4, A5 and A6 copolymers in chloroform solvent.



EL - spectral response of copolymers at an excitation wavelength of 418 nm.

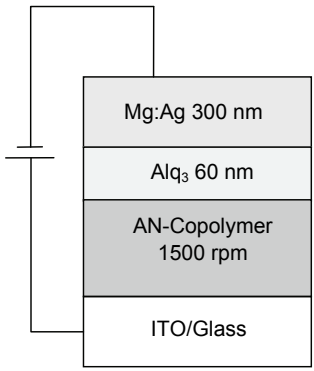
Various physical properties of synthesized copolymers.

Copolymers	M_Z (g/mol)	M_W (g/mol)	M_n (g/mol)	P.D.	Thermal Stability
A1	820	540	405	1.3	206ºC
A2	895	415	235	1.77	210ºC
A3	1150	640	390	1.64	210ºC
A4	1985	655	325	2.01	392ºC
A5	1005	505	300	1.68	375ºC
A6	1335	505	225	2.24	210ºC

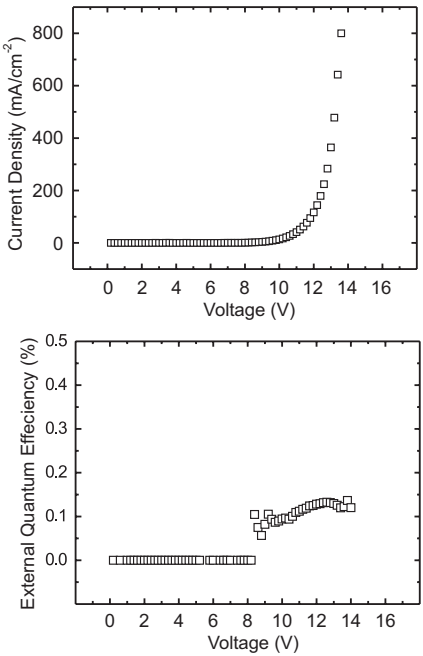
4.2 Synthesis of Anthracene-Naphthalene Copolymers for Green OLEDs

A well-defined alternative technique based on statistical combination of anthracene-naphthalene (AN) monomers for synthesis of highly soluble light emissive green copolymer was developed.

The copolymer is thermally stable up to 335ºC with complete absence of the glass transition phase. Both SEM and XRD reveal a complete amorphous nature with globular morphology. The highly processible nature eludes to the suitability of this copolymer for the fabrication of double and multilayered OLED device structures by using solution-casting techniques. A change in light emission characteristics was observed with increase in potential. The device provides green emission at 10 V, which switches to bright yellow-white emission at 13 V.



Double-layer device configuration for (AN)-OLED copolymer.

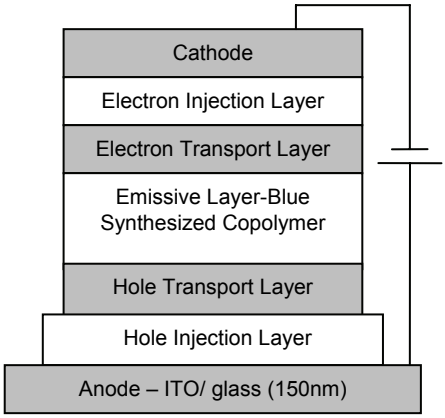


Current-voltage characteristics (top) and external quantum efficiency (bottom) as a function of bias voltage of (AN) double layer OLED-device.

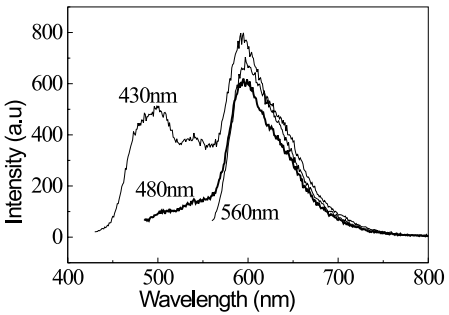
4.3 Anthracene Short Chain Copolymers for Blue OLEDs

Short-chain anthracene-polyacene based copolymer, that acts as a blue emitter for light emitting devices has been developed by using a modified Kovacic synthesis. Structurally, the copolymer exhibits an amorphous character, followed by its thermal stability up to 208ºC. An increase in electroluminescence efficiency was observed due to resistance over aerial oxidation. The statistical arrangement of monomeric units within the copolymeric matrix provides a keto-free defect structure. A well-defined solvatochromic behavior was observed for the copolymer.

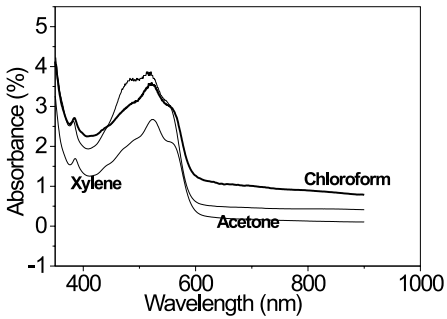
Preliminary experiments considered anthracene copolymer as an emissive layer for blue OLEDs. The device operates at 6 volts. Evaluation of the electrical characteristics and device parameters are in progress.



Multilayer device structure for blue OLED.



EL-spectral response of blue copolymer at an excitation wavelength of 430, 480, and 560 nm.

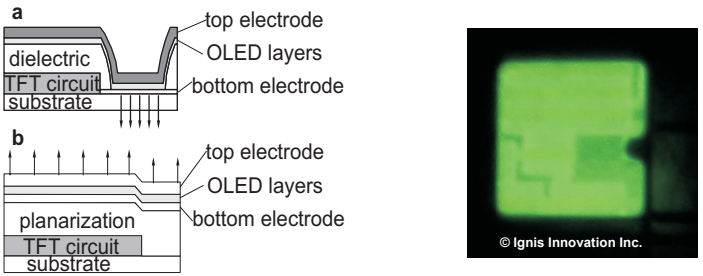


Solvatochromic behaviour of blue copolymer in the presence of different solvents.

4.4 Integration of Amorphous Silicon TFT and OLED for Active-Matrix OLED Displays

In active-matrix organic light emitting diode (AMOLED) displays, each pixel is controlled by a driver circuit made of thin-film transistors (TFTs). Pixel architectures for the AMOLED can be divided into bottom- or top-emitting (see below). In the former, the TFT circuitry and OLED are placed side-to-side, and the pixel aperture ratio is rather low (15-40 %), and decreases as pixel size is scaled down. With the latter, since the OLED can be integrated on top of TFT circuitry, the aperture ratio is much greater (70-80%) and is less sensitive to pixel size scaling. Top-emitting vertically integrated architectures are preferred, given the area usage of TFT circuitry in a-Si technology.

Since the OLED layers are very thin (~10 nm), smoothness of the substrate and bottom electrode is critical for high OLED efficiency and high device/pixel yield. Proper surface quality can be achieved with the help of a planarization layer, which is deposited on top of TFTs and serves as the substrate for OLED bottom electrode. Here, a low-permittivity polymer dielectric is employed by spin-coating a photosensitive precursor followed by photolithographic patterning and thermal polymerzation. The planarization dielectric provided a smooth substrate profile with low surface roughness ~1nm. Since the interconnection between TFT and OLED has to be made through the planarization layer, polymer processing was optimized for desirable pattern profile and low contact resistance of through-vias. A reliable via opening down to 10-20 μm in size and with contact resistance of ~2-3 Ω/via has been achieved. A photograph of an operating TFT-OLED pixel is shown below. A bright emission and good brightness control have been obtained at supply voltage below 10 V, which implies that good quality OLEDs can be integrated on top of a planarized TFT backplane.

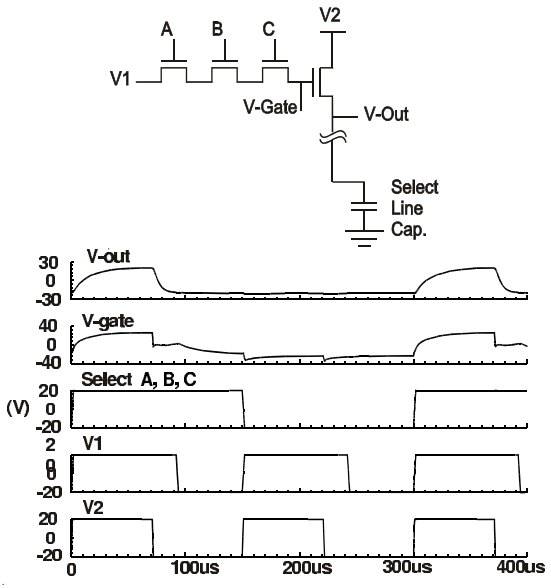


Bottom-emitting (left-a) and top-emitting (left-b) pixel architectures and microscope image of top emitting 4T AMOLED pixel (right – courtesy of Ignis Innovation Inc.).

4.5 Amorphous Silicon Demultiplexer

With the development of organic light emitting diodes (OLEDs), there is considerable interest in both active and passive matrix flat-panel OLED displays. As is well known, gate-drivers are needed for selectively addressing different pixels of an array. The typical gate-drivers consist of demultiplexer (demux) and buffers. In conventional displays gate-drivers are implemented in crystalline-Si CMOS technology, which necessitates a large number of output pads in the pixel-array consequently increasing its cost. Amorphous silicon gate-drivers pave way for the integration of gate-driver with the a-Si backplane array and thus obviate the need for high pin-count external drivers. More specifically integrating the demux onto the display board reduces the pin-count of the backplane from 2^N (the number of gate-lines in the array) to N (number of select signals of demux). The reduced pin-count not only reduces the system cost significantly but also enhances the reliability of the system by minimizing the number of leads and bonding.

The schematic of a pass-transistor based ΔV_T invariant demux is shown below. Here, the holistic R-C load of a QVGA array is considered for realistic loading at the output node. The dynamic performance characteristics for the demux is also illustrated. We use a bipolar pulse for attaining the ΔV_T invariance of the demux-characteristics.

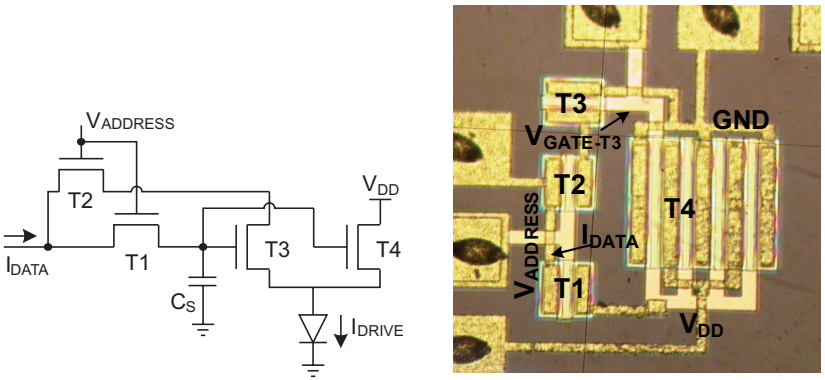


Schematic (top) and transient performance (bottom) of a pass-transistor based a-Si:H demux.

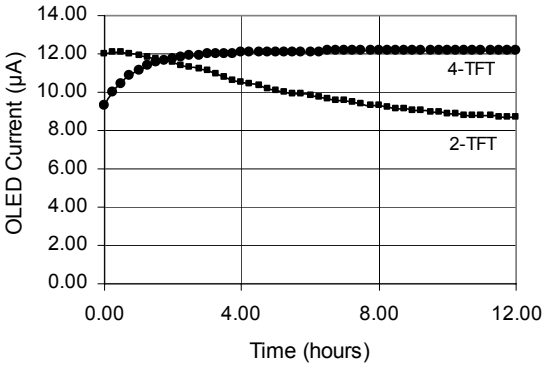
4.6 Current Programmed Pixel Circuits

A TFT circuit behind every pixel in an AMOLED display is needed to control the brightness of each pixel. Conventional 2-TFT circuits cannot compensate for V_T shift in the TFTs, due to which the display brightness degrades by about 30% over a few hours of operation. We have developed 4-TFT current programmed V_T shift compensating pixel circuits that overcome this problem and provide long-term display brightness stability.

The circuits work on the current mirror principle, therefore can be designed to attenuate or amplify the data current. They offer low power consumption, adequate programming times for 60 frames/second operation, and temperature/mechanical stress invariant operation.



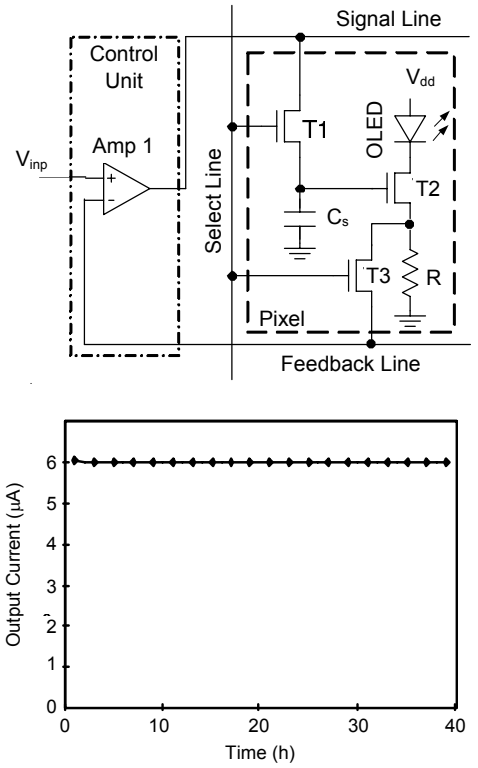
4-TFT circuit schematic and its photomicrograph.



Stability comparison of conventional 2-TFT and new 4-TFT circuits.

4.7 Voltage-Programmed Feedback Pixel Circuit for OLED Displays

An a-Si:H pixel circuit with voltage feedback for active-matrix organic light-emitting diode displays has been developed. It has been shown that by applying the feedback method, it is possible to provide very accurate current for the OLED despite shifts in TFT device parameters. As illustrated in the figure, the circuit comprises three TFTs, a storage capacitor, and a feedback resistor made of microcrystalline n^+a-Si:H. The control unit is common for each column and in the simplest form, it is a differential amplifier. DC measurements show that the output current of the circuit remains constant within 0.3% of its original value despite more than 2.5 V shift of the threshold voltage of the driving transistor. Fig. 2 shows the current stability of the pixel circuit for more than 40 hours in the presence of 2.5 V shift of threshold voltage of T2. Measurements also show that the microcrystalline feedback resistor of the pixel is stable enough to be used as the feedback element.

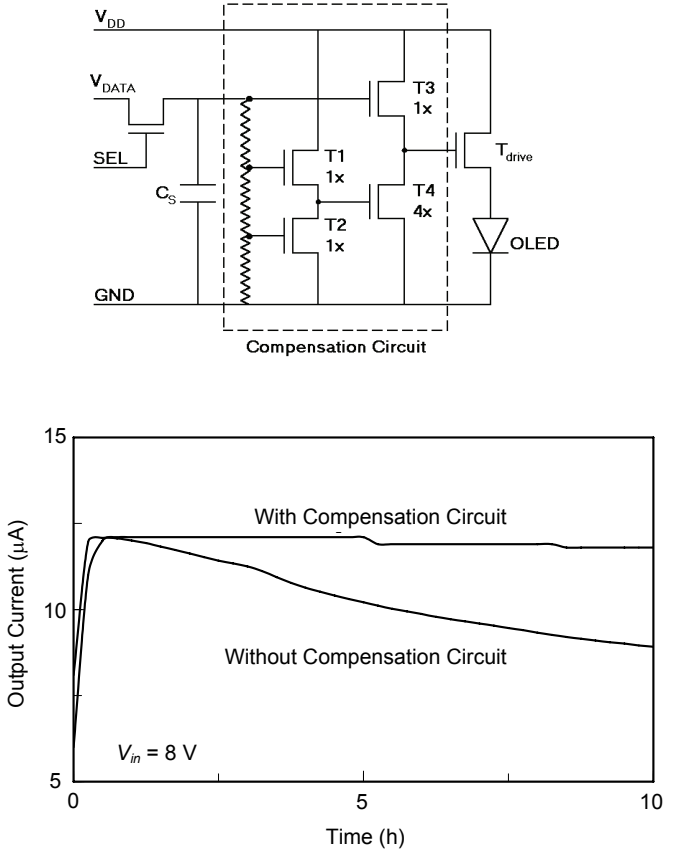


Schematic (top) and output current stability (bottom) for feedback pixel circuit.

4.8 Open Loop Voltage-Programmed Pixel Circuit

Pixel drivers for AMOLED displays require a stable current output. Therefore we need to design a compensation circuit which can track the V_T shift in the drive TFT and provide a constant current to the OLED.

The compensation circuit shown below makes use of the fact that the threshold voltage shift of a TFT is a strong function of the applied gate voltage. The circuit reflects its input as the gate voltage of the drive TFT and uses the threshold voltage shift in the TFTs T1, T2, T3 and T4 to track the threshold voltage of the drive TFT, thereby providing a constant overdrive. The performance of this circuit is also illustrated below.

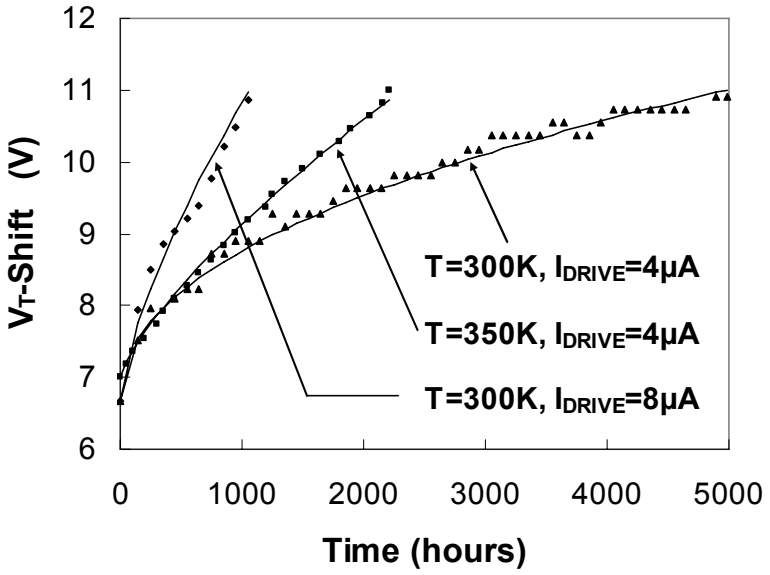


Schematic of open loop voltage-programmed compensation circuit (top) and comparison of OLED current transient characteristics with and without the compensation circuit (bottom).

4.9 Acceleration Factor for Circuit Testing

A lifetime of 20000 hours is generally considered as the minimum requirement before a commercial AMOLED display can be manufactured. However, is impractical to test any circuit for that duration, hence accelerated testing methods have to be used. Unlike the well characterized CMOS VLSI testing, there is no standard method to perform accelerated stress tests on a-Si:H circuits.

Since V_T shift in TFTs is the main reason for pixel circuit failure, the temperature and dependence of the V_T shift in TFTs under constant current stress was modeled. **Error! Reference source not found.**The model was used to calculate a time-dependent acceleration factor. Fig. 4.8.1 demonstrates that acceleration factors of up to 5 can be obtained by operating pixel circuits at higher temperatures or higher current stresses.



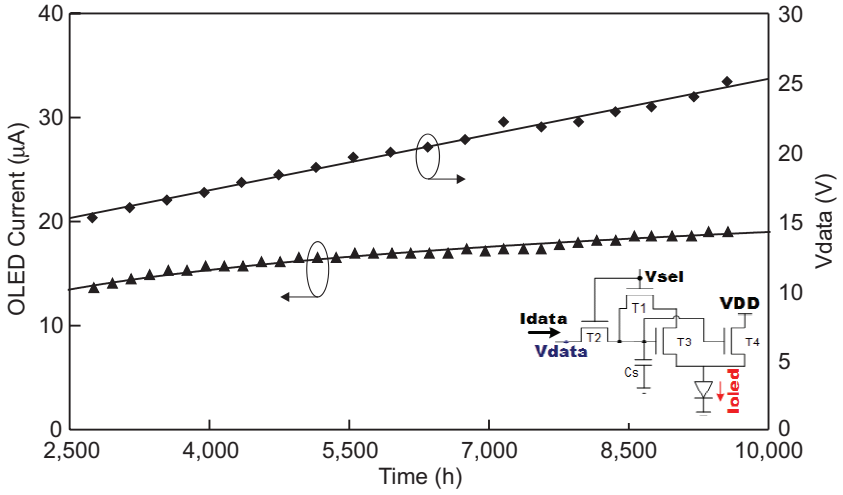
Accelerated testing of AMOLED pixel circuits.

4.10 Lifetime Testing of a-Si Pixel Circuits

The primary issue that must be addressed in a-Si backplane design is the compensation for V_T shift. The 4-TFT circuit architecture is such that the input data current is replicated at the OLED (see below). Therefore any factors that change the performance of the TFT (including V_T shift, temperature, and mechanical stress) will not affect the relationship between input and output currents. In addition, judicious choice of biasing conditions of the current mirror allows for a controlled increase in OLED current to compensate for OLED degradation.

TFT circuits were fabricated using a 300°C process. The circuits were then diced and bonded into ceramic packages. Testing the circuits in discrete form allows access to all nodes for diagnostic purposes. Due to the large parasitic capacitances involved with packaging a discrete pixel circuit and using a current driver based on discrete ICs, the pixel was operated at 8.3 Hz instead of the targeted 60 Hz, which would be easily achievable in an array due to lower parasitics. The voltage at the IDATA node (i.e. VDATA) was also monitored and plotted on the same figure.

Test data shows operation for nearly 10,000 h at high current levels, and the circuit continues to operate. The current level is high to accelerate the test; the actual current levels for a similar pixel would be closer to 1.5 µA. Factoring in the accelerated aging due to high current, this test is equivalent to over 30,000 h at 1.5 µA.

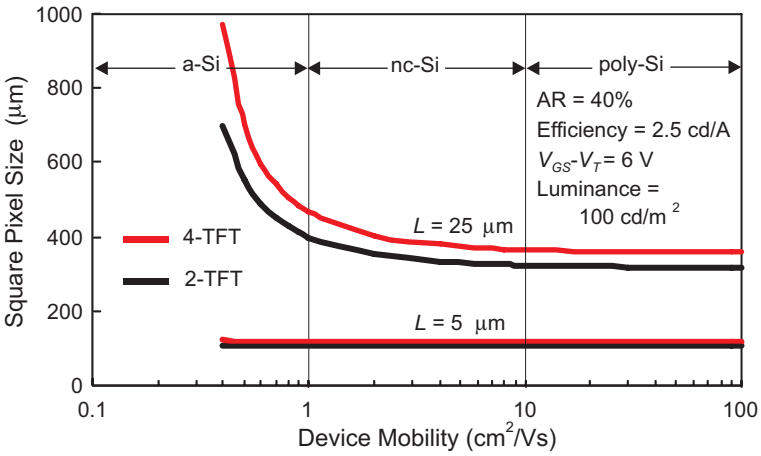


Lifetime test of 4T pixel circuit and schematic (inset).

4.11 Mobility Considerations for a-Si TFT Based AMOLED Backplanes

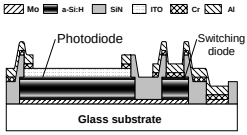
Recent advances in active matrix OLED (AMOLED) displays have shown increasing interest in amorphous silicon (a-Si) thin film transistor (TFT) backplanes. Several prototypes have been demonstrated that prove the viability of a-Si as an alternative to the relatively new and expensive low temperature polysilicon (LTPS). The a-Si backplane for AMOLEDs takes advantage of the vast installed infrastructure of the ubiquitous AMLCD technology, thus enabling much lower manufacturing costs and rapid commercial deployment.

The low mobility limitation of the a-Si TFTs, (which places unfavourable limits on pixel size and aperture ratio (AR) particularly for bottom-emitting pixel architecture) has been dispelled by impressive advances in the OLED device efficiencies recently. Hence, the application space for a-Si based AMOLED now ranges from small full colour cell phone displays to HDTV screens. For a 4-TFT fully compensating bottom-emitting pixel circuit, the sensitivity of device mobility on pixel size is illustrated in the figure below. It is evident that for most applications, mobility is no longer the limiting factor for a-Si, because the interconnect area is the dominant factor. The maximum dot-per-inch (DPI) attainable for bottom emitting pixels with a reasonable aperture ratio of 40%-60% for a commercial process can be as high as ~200. Here the difference between the attainable aperture ratio for a-Si and poly-Si is less than 5%.



Pixel size as function of device mobility.

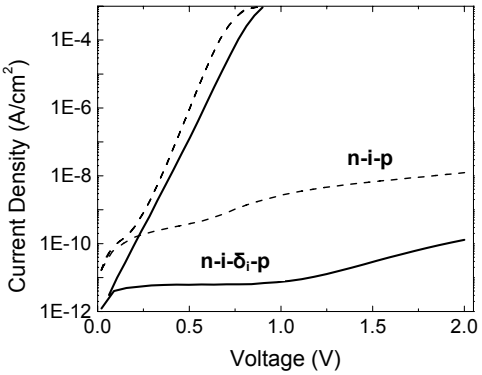
5 Optical and X-Ray Imaging



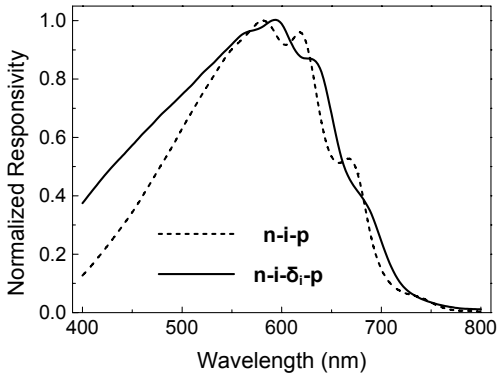
5.1 Novel n-i-δ_i-p Photodiode

A novel n-i-δ_i-p photodiode, which combines the advantages of a-Si:H and a-SiC:H/a-Si:H p-i-n photodiodes in terms of reverse dark current and extrinsic quantum efficiency has been developed.

It is found that introduction of a thin graded layer and an undoped a-SiC:H buffer (δ_i-layer) between the i(a-Si:H) and p(a-SiC:H) layers reduces the leakage current and decreases interface recombination. A δ_i-layer thickness of 4 nm is found to be optimal for the 2 eV bandgap a-SiC:H alloy. The observed dark current density of 8 pA/cm^2 at reverse bias of 1V is close to the fundamental lower limit set by carrier emission from deep levels in the a-Si:H bulk as evaluated from the time-dependence of dark current. The n-i-δ_i-p photodiode with optimized δ_i-layer thickness has a good transient response, with low image lag at low light intensities, as well as enhanced short-wavelength responsivity, thus making it suitable for low-level light detection and imaging applications.



***J-V* characteristics of n-i-p and n-i-δ_i-p heterostructures.**

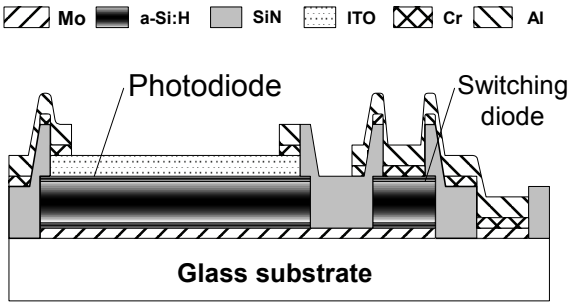


Spectral responses of the a-Si:H n-i-p diode and n-i-δ_i-p heterostructure.

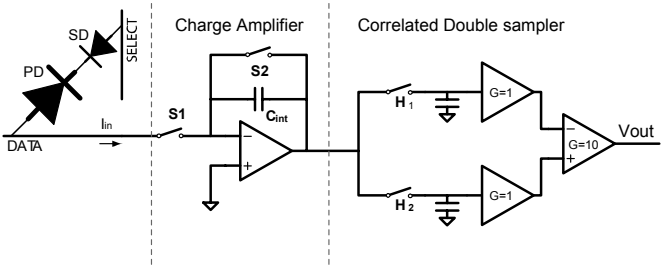
5.2 Two-Dimensional Photodiode Array

A two-dimensional a-Si:H-based *n-i-p* photodiode array with single-switching diode readout has been developed. Utilization of the a-Si:H switching diodes for signal readout makes it simpler than conventional active-matrix-arrays with TFT switches, and the number of masks required in lithography have been reduced to six. The device design and fabrication are optimized to minimize the level of the leakage current. The sensing diodes have a reverse dark current density of ~0.5 nA/cm^2 at -5V bias, which is among the lowest ever reported. The ON/OFF current ratio for the 200x200 μm^2 switching diode is ~2×10^6. The external quantum efficiency of the photodiodes with 25nm a–SiC:H p-layer is up to 85 % in the range 560 to 580 nm, and ~30% at 400 nm.

A 3x4 pixel array prototype has been successfully tested using a specially designed readout system, where pre-amplification, double sampling and a final amplification are performed at each column. The detector shows good linearity over several voltage decades and the ability to detect extremely low light levels.



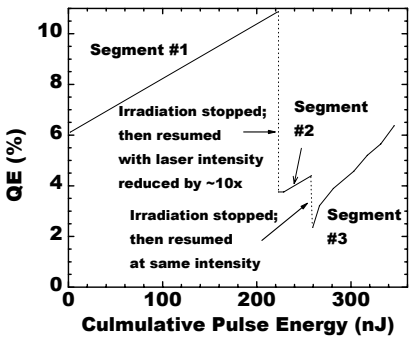
Cross section of sensing pixel.



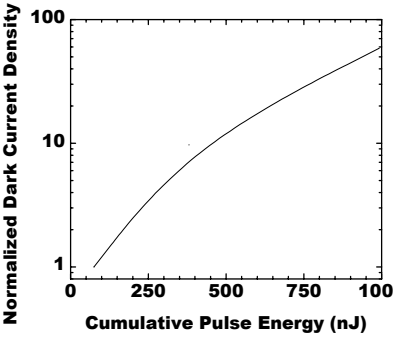
Block diagram of single readout channel.

5.3 Deep-UV CCD Imaging: Degradation Mechanisms

With an increasing number of industrial applications shifting to intense deep-UV laser sources, high performance deep-UV sensors for inspection and process control applications are in demand. The most notable example of deep-UV imaging is in photolithography and semiconductor inspection systems, where sensors are needed to image deep sub-micron features. Deep-UV sensitive CCD image sensors have been developed; however, their long-term stability is still a major concern. Experimental results suggest that careful control of the oxide thickness and the Si-SiO_2 interface quality are critical for realizing CCD sensors with high responsivity and stability for deep-UV imaging. When samples of thinned front-illuminated linear CCD sensors are exposed to F_2 (λ = 157 nm) excimer laser radiation, fluctuation in the extrinsic quantum efficiency (QE) and a substantial upsurge in the dark current density are observed as a function of exposure dose. The visible QE, dark current, and charge conversion efficiency (CCE) are also permanently altered by the deep-UV irradiation. These instabilities can be attributed to a variety of UV-induced effects that modify the optical and electrical properties of the SiO_2 layer and Si-SiO_2 interface, resulting in reversible and permanent shifts in CCD performance. Optimization of the overlying oxide thickness and the Si-SiO_2 interface quality are necessary in order to realize CCD image sensors with the desired performance, radiation tolerance, and stability at deep-UV wavelengths. Investigation of DUV enhancement and radiation hardening techniques (e.g., nitridation and fluorine doping of the SiO_2) for CCD sensors is also critical in order to drive additional advancements in this area.



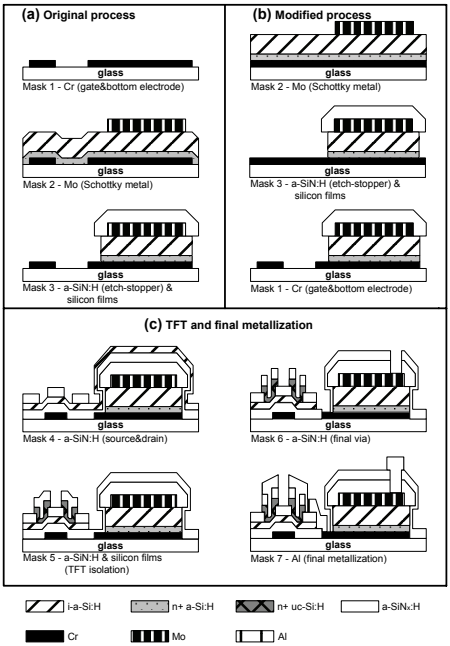
Fluctuations of extrinsic QE at 157 nm.



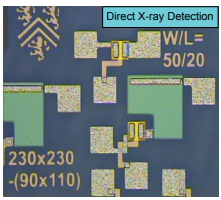
Normalized dark current density as a function of exposure to 157 nm radiation.

5.4 Process Integration of X-Ray Direct Detection Pixel

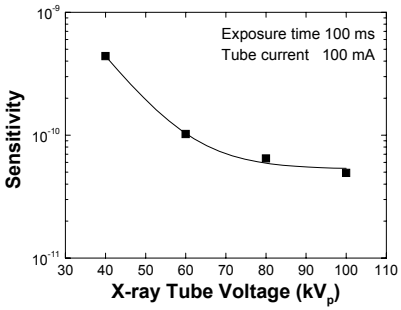
We have previously developed a direct X-ray detection scheme based on a Mo/a-Si:H Schottky diode structure for low-energy X-rays. Here, an alternate strategy to reduce mechanical stress issues pertinent to the process integration of Mo/a-Si:H Schottky diodes and TFTs is presented. The previous approach was to minimize the intrinsic stress in the Mo layer through appropriate process conditions and film thickness. But this was over a narrow process latitude and with compromised X-ray sensitivity. Alternatively, the mechanical stress in the Mo can be reduced by reducing and/or avoiding the extrinsic stress exerted on the Mo by the underlying films through a different masking sequence in the fabrication. This modified process allows for a more flexible design of the Mo layer for enhanced X-ray sensitivity, while maintaining the mechanical integrity of the various layers. The fabricated pixel shows high detection efficiency at low X-ray tube voltages.



(a) Original and (b) modified Mo/a-Si:H Schottky diode, and (c) a-Si:H TFT and final metallization processes.



Photomicrograph of an X-ray detection pixel.

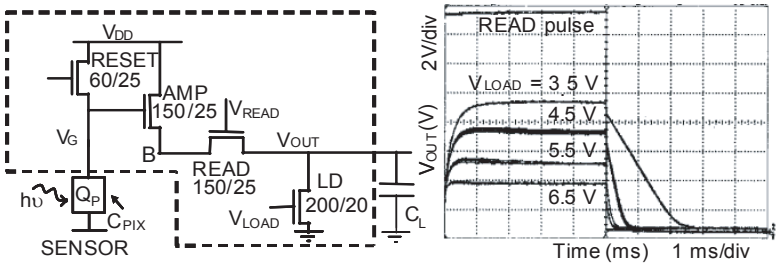


X-ray sensitivity vs. X-ray tube voltage.

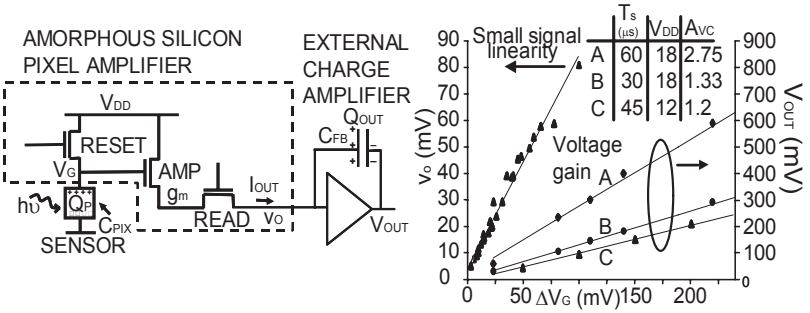
5.5 Active Pixel Sensor for X-Ray Detection

Mammography or diagnostic breast x-ray imaging has the requirements of small pixel size (50 μm) and high-density large area arrays (3600 x 4800 pixels). The voltage mediated active pixel sensor (V-APS), which uses an active transistor within the pixel to drive the output column data bus may be suitable for this application due to its relative ease of integration with on-panel multiplexers. The figure below illustrates a V-APS pixel with an on-chip active load TFT in saturation.

While the V-APS offers the advantage of direct integration with an on-panel multiplexer, its implementation in a-Si technology is unsuitable for real time performance medical imaging applications such as fluoroscopy. Hence, the current mediated active pixel sensor (C-APS) (see figure below) is employed to produce amplified current output to drive an external charge amplifier. Its signal linearity and gain demonstrate the feasibility for medical imaging modalities.



V-APS with active load and readout time measurements.

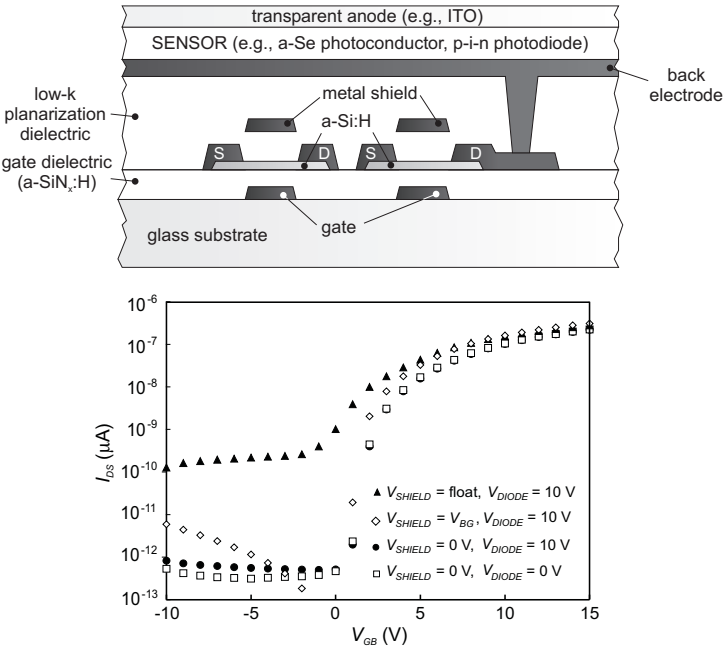


C-APS readout circuit schematic and small signal performance.

5.6 Vertically Integrated a-Si:H Active Pixels for X-Ray Detection

In large area flat panel x-ray imagers, it is important to ensure that the fill factor is high enough to provide sufficient charge collection. Conventional imagers are based on a co-planar architecture where the sensor and readout circuitry are placed adjacent to one another. Thus, increasing the on-pixel density of TFTs or scaling down pixel sizes reduces the fill factor. To avoid any degradation in fill factor, the pixel can be vertically integrated with the sensor, which follows from a fully overlapped electrode concept. However, the continuous back electrode can give rise to parasitic capacitances. One possible effect of the back electrode is to induce a parasitic channel in the a-Si layer of an overlapped TFT during its OFF state, giving rise to a larger leakage current I_{DS}. To minimize or eliminate this leakage, a dual gate TFT architecture is employed, in which the voltage on the top gate (metal shield) can be chosen to minimize the charge induced in the (parasitic) top channel.

The cross section of a fully overlapped architecture and its TFT transfer characteristics are shown in the figure below. The lowest values of leakage current are obtained when the TFT second gate bias V_{SHIELD} is set to either 0 V or to the TFT bottom gate V_{GB}.

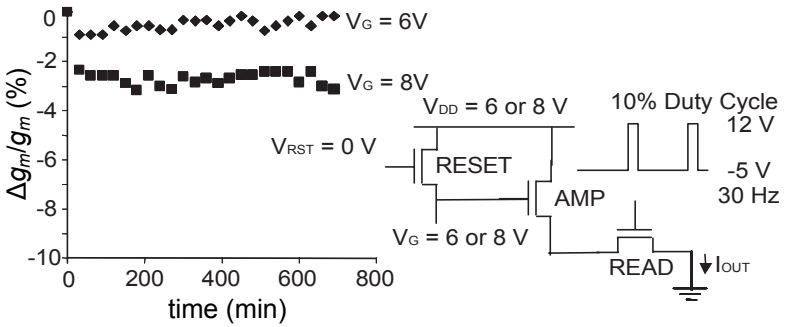


Fully overlapped architecture and TFT transfer characteristics (V_{DS} = 1 V).

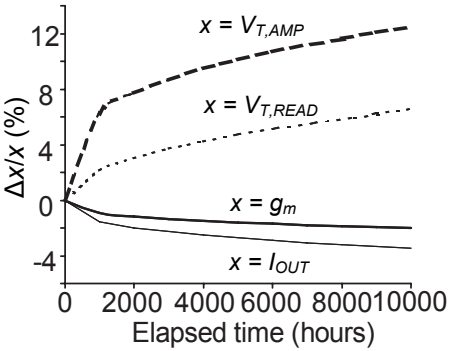
5.7 ΔV_T Compensated a-Si:H Pixel Amplifier for Fluoroscopy

The current mediated amorphous silicon active pixel architecture (C-APS) advances the state-of-the-art by offering a large area real time imaging solution for fluoroscopy. However, the threshold voltage shift ΔV_T of the a-Si:H TFT gives rise to new design challenge in order to maintain sufficient pixel transconductance g_m, which varies over time.

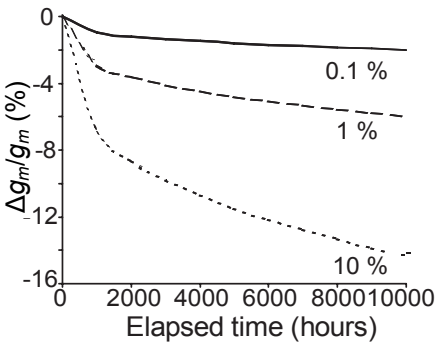
For the C-APS architecture, the characteristic ΔV_T of the a-Si READ and RESET TFT switches is minimized by appropriate bipolar TFT bias voltages in the ON and OFF states. Due to intrinsic feedback, the READ TFT has a compensatory effect on the g_m of the pixel readout circuit. As shown in the figure below, g_m is expected to decrease only by less than 2% over the lifetime of the array. The figure illustrates how reduction in duty cycle will mitigate the ΔV_T, thus low leakage currents can be coupled with small duty cycles to give a relatively small shift in C-APS g_m, and consequently, the gain.



Variation in g_m for the pixel circuit over time.



Percentage change in V_T of READ and AMP TFTs, g_m, and output current of APS readout circuit.



Percentage change in g_m for different duty cycles.

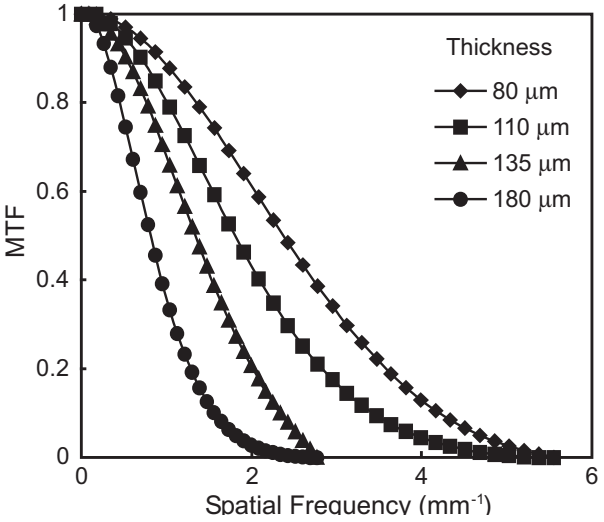
5.8 MTF Measurements of Gd_2O_2S:Tb Based Phosphor Films Coupled With Photodetectors

The Gd_2O_2S:Tb based phosphor coupled with photodetectors has been widely used in digital x-ray imaging applications. One of the key issues associated with the phosphor film is spatial resolution. The spatial resolution of phosphor films can be characterized by measurement of the modulation transfer function (MTF).

The MTF describes the modulation in signal amplitude in the image of a sinusoidally varying object as a function of the object spatial frequency. The MTF, $T(u)$ is given by the modulus of the Fourier transform of the line spread function (LSF), $l(x)$,

$$T(u) = \left| \int_{-\infty}^{\infty} l(x) e^{-2\pi i u x} dx \right|,$$

where u is the spatial frequency of the image. The results depicted in the figure show a degradation of spatial resolution as the phosphor film thickness increases. In thicker films, the optical photons generated inside the phosphor film need to travel larger distances to the detector. Here, they get scattered in the process to increase the isotropy in propagation path thereby reducing the spatial resolution.

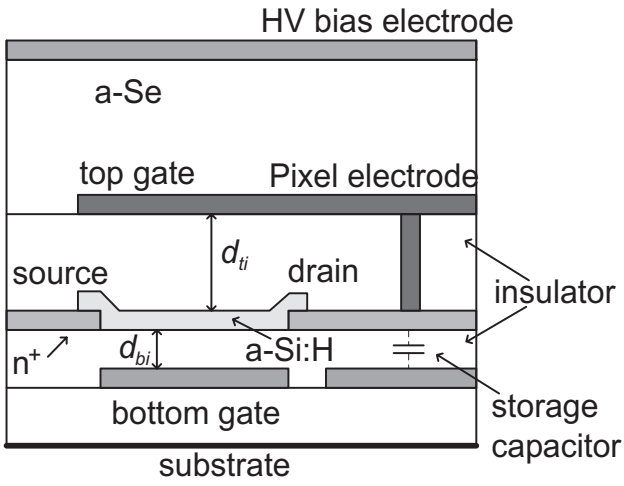


MTF of phosphor films as a function of film thickness for a phosphor grain size of 2.5 μm.

5.9 Digital Radiology Using Active Matrix Readout With High Voltage Protection

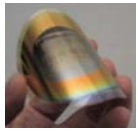
Direct radiographic detection employs a layer of X-ray sensitive photoconductor such as amorphous selenium (a-Se) to directly convert the incident X-rays to charge. A positive high voltage of several thousand volts is applied to the top surface of a-Se in order to establish an electric field for electron-hole separation. The electric field in the Se layer can be 1-10 V/μm. Holes created by X-rays are driven by the electric field to the bottom electrode, where the detection of charge is done through a-Si:H active matrix readout array. Hence, the bottom electrode is susceptible to damage during prolong suspended detector scan or accidental over-exposure. A high voltage build up at the pixel electrode can lead to dielectric breakdown in the a-Si:H readout circuits, rendering the detector unusable.

The use of dual-gate thin-film transistor (TFT) in the pixel readout circuits has been proposed for protecting the active matrix from high voltage damage (see figure below). Under normal operating conditions, the bottom gate performs as an ordinary single gate TFT, and the top gate is not turned ON. However under undesirable detection conditions, the top gate acts as a protection gate that automatically turns ON the TFT before the electrode reaches a damaging value and overrides the bottom gate control. The threshold voltage V_T of top and bottom gates are controlled by their corresponding gate dielectric thickness (d_{ti} and d_{bi}) to minimize leakage current at the TFT OFF state.



High voltage protection pixel with the use of dual-gate TFT.

6 Photovoltaics



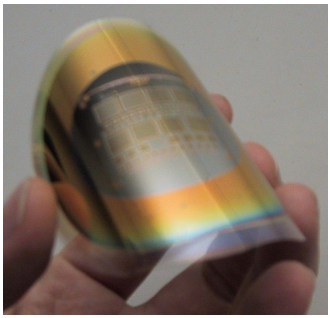
6.1 Low Temperature Amorphous and Nanocrystalline Silicon Solar Cells

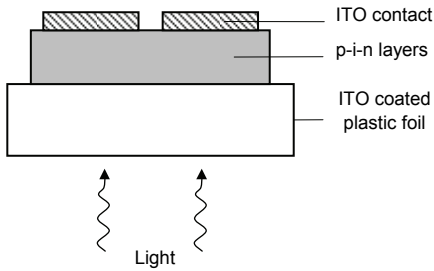
We have developed a-Si:H and nc-Si deposition process at 75ºC for flexible solar cells on low-cost plastic foils. The aim of this work is to fabricate thin film solar cells on large area by roll-to-roll technology for portable applications as well as light-weight and cost-effective solar power generation arrays. The a-Si:H layer absorbs the high-energy part of the solar spectrum whereas the nc-Si acts as the red- and infrared absorber. All films were deposited using conventional RF 13.56 MHz PECVD in a single chamber system.

The a-Si:H deposited at 75ºC has an optical bandgap between 1.68 eV and 1.90 eV, hydrogen concentration ranging between 8 at.% to 9.5 at.% that is predominantly bonded in monohydride form. The microstructure parameter *R* varies between 0 and 4.6. These parameters can be adjusted by deposition conditions. The dark- and photoconductivity values are 3.2×10^{-9} S/cm and 3.8×10^{-5} S/cm, respectively. Post-deposition thermal annealing at temperatures above the deposition temperature but below 150ºC appear to strongly improve the electronic properties.

Optimal electronic properties in a-Si:H deposited at 75ºC is often accompanied by high compressive stress (0.2 to 0.5 GPa), which frequently results in peeling the films off the substrates.

Undoped nc-Si deposited at 75ºC has a crystallinity above 60% in 20 nm thick film, and above 80% in 100 nm thick film with a crystallite grain size of about 10 nm. The dark conductivity is about 3×10^{-7} S/cm. Thermal annealing at 150ºC increases this value by approximately one order of magnitude. This effect is attributed to hydrogen rearrangement at the grain boundaries, which reduces the energy barrier there.



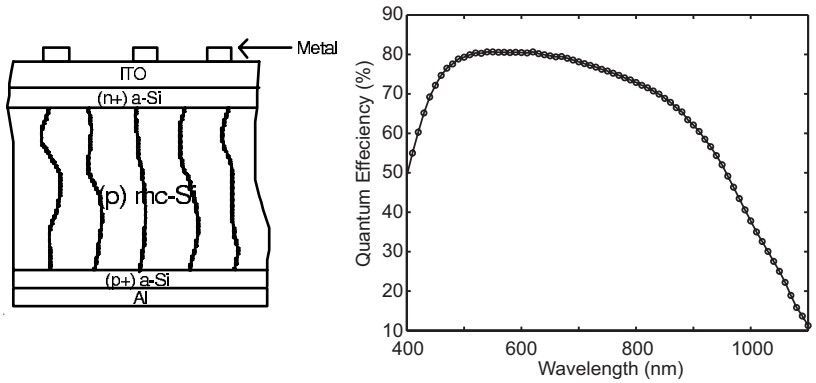


Photograph of solar cell on plastic and schematic cross section.

6.2 Amorphous Silicon/Multicrystalline Silicon Heterojunction Solar Cells

Cost reduction is an important issue in the fabrication of silicon (Si) photovoltaic (PV) cells, where the material cost accounts for nearly half of the overall cost. Materials like multicrystalline silicon (mc-Si), silicon ribbons, etc., offer a cost effective option for Si PV cells compared to single crystalline Si. In most of those materials, however, the presence of a large number of grains (mm to cm scale), grain boundaries, and crystallographic defects necessitates defect passivation. Defect passivation by atomic hydrogen is a very efficient method. However, this imposes a temperature (T) limit for any post-passivation processes such as p-n junction diffusion at high-T. Implementation of amorphous Si (a-Si)/crystalline Si heterojunctions in place of diffused homojunctions in defective Si can keep the process temperature low thereby preserving the defect passivation. In this project we target two main goals: (i) developing appropriate gettering and hydrogenation techniques to improve minority carrier life time in low cost mc-Si substrates (ii) developing a robust low temperature a-Si/mc-Si heterojunction technology for photovoltaic applications.

Plasma hydrogenation is employed to passivate crystallographic defects close to the heterojunction. This process is expected to improve fill factor of the solar cells. Passivation of defects deep inside the mc-Si substrate is performed by the plasma immersion ion implantation technique to improve minority carrier lifetime in bulk mc-Si. This process is expected to improve the spectral response of solar cells in infrared regime.



Heterojunction solar cell structure and measured quantum efficiency a 1 cm^2 solar cell.

6.3 Low Temperature Solar Cells

This project addresses fabrication of a-Si:H based solar cells on flexible plastic foils for wearable electronics.

A p-i-n structure was deposited on glass substrate covered with ITO. The thicknesses of the p-, i- and n-layers were 30 nm, 300 nm and 30 nm, respectively. Aluminum contacts were deposited on top, then an ITO contact was opened using RIE. The maximum processing temperature was 75°C.

The spectral quantum efficiency, and dark and illuminated *I-V* characteristics were measured.

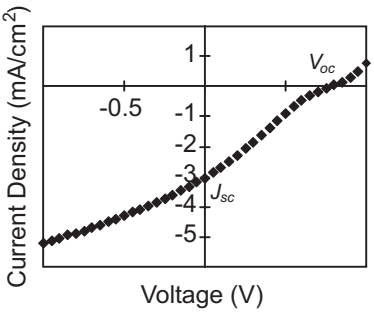
The spectral quantum efficiency (QE) demonstrates a maximum at a wavelength of 450-500 nm. It should be noted that the maximum QE shifts to higher wavelength with increase in the annealing temperature. The annealing at 150°C improves QE from 0.25 to 0.45 at 0 V bias, and from 0.30 to 0.60 at 1 V bias. The improvement in QE can be explained by the dangling bonds annealing in the bulk i-layer.

The wavelength of the QE maximum is lower than it was observed for an amorphous silicon solar cell (with an i-layer of about 600 nm), and can be attributed to its smaller i-layer thickness (300 nm).

The illuminated *I-V* characteristics were used for determining the solar cell parameters, which are the short circuit current I_{sc}, open circuit voltage V_{oc}, and fill factor $FF = P_{max}/I_{sc}V_{oc}$. The performance of the 75°C solar cell is presented in the following table. As can be seen, annealing improves I_{sc} and P_{max}, while no improvement in V_{oc} is observed.

Normalized solar cell parameters.

$T_{annealing}$ (°C)	I_{sc} (mA/cm^2)	V_{oc} (V)	P_{max} (mA/cm^2)	*FF*
No annealing	2.26	0.65	0.36	0.25
120	3.28	0.8	0.65	0.25
150, 1hr	3.7	0.75	0.72	0.26
150, 6hrs	5.16	0.78	0.96	0.24



***I-V* characteristics of a-Si:H solar cell deposited at 75ºC.**

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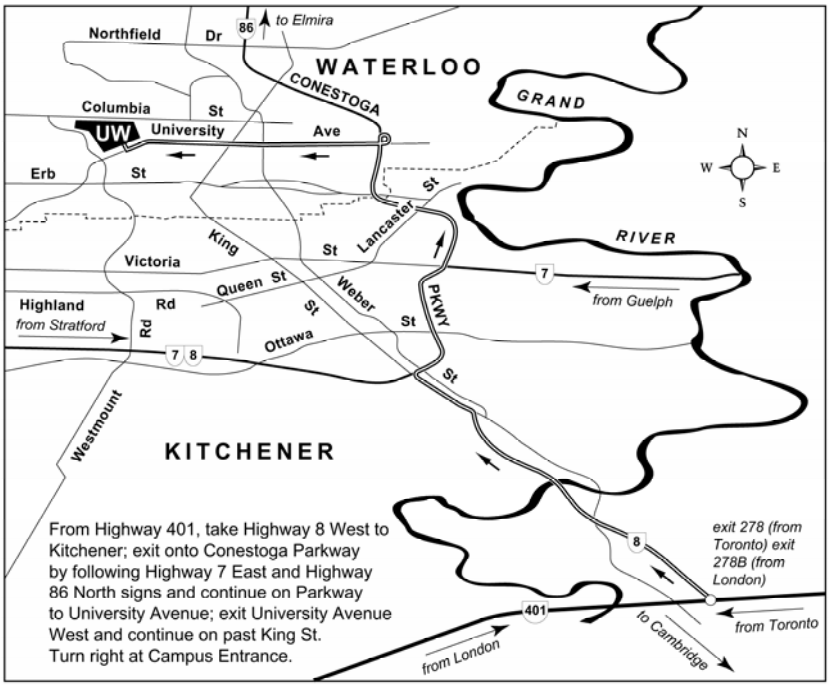

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