EMTP, Transient Stability and Power Flow Models and Controls of VSC Based FACTS Controllers

by

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Abstract

This thesis gives an overview of the emerging FACTS technology with emphasis on the STATCOM, SSSC and UPFC controllers. The basic operating principles of the controllers are explained in this thesis, together with the main circuit configurations, functions and general control strategies. The thesis proposes and describes transient stability and power flow models of the STATCOM, SSSC and UPFC. The proposed models accurately represents behavior of the controllers in quasi steady state operating conditions, and are adequate for transient and steady state analyses of power systems. The models are validated with the help of the Electromagnetic Transient Program (EMTP), where detailed models of the controllers are implemented and compared to the suggested stability models. Also, a comparison of different control strategies for the UPFC is given, together with a novel, efficient and simple controls for this controller. A realistic 11-bus power system is used throughout the thesis to validate proposed models and compare different control strategies. The controllers are simulated under different operating conditions using both, the detailed and "reduced", models.

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List of Symbols

V_{dc}	dc voltage
I_{dc}	dc current
P_{dc}	energy stored in dc capacitor
P_{ac}	energy going in/out of VSC
m_f	frequency modulation ratio
m_a	amplitude modulation ratio
α, β	angle of the converter output voltage w.r.t. reference voltage
v_d	voltage component in phase with reference voltage
v_q	voltage component in quadrature with reference voltage
i_{sed}	current component in phase with reference voltage
i_{seq}	current component in quadrature with reference voltage
$R_L^{'}$	transmission line total resistance
$L_L^{'}$	transmission line total inductance
v_{sh}	shunt converter output voltage
v_{se}	series converter output voltage
X	coupling transformer leakage reactance
C	dc capacitor capacitance
m_{sh}	amplitude modulation ratio of shunt VSC
m_{se}	amplitude modulation ratio of series VSC
a_{sh}	turns ratio of shunt coupling transformer
a_{se}	turns ratio of series coupling transformer

Chapter 1.

INTRODUCTION

1.1 General Introduction

In today's highly complex and interconnected power systems, sometimes made of thousands of buses and hundreds of generators, there is a great need to improve electric power utilization while still maintaining reliability and security. Available power generation, usually not situated near a growing load center, is subject to regulatory policies and environmental issues. In order to meet the ever-growing power demand, utilities prefer to rely on already existing generation and power export/import arrangements instead of building new transmission lines that are subject to environmental and regulatory policies. On the other hand, power flows in some of the transmission lines are well below their thermal limits, while certain lines are overloaded, which has as an overall effect of deteriorating voltage profiles and decreasing system stability and security. In addition, existing traditional transmission facilities, in most cases, are not designed to handle the control requirements of complex, highly interconnected power systems. This overall situation requires the review of traditional transmission methods and practices, and the creation of new concepts which would allow the use of existing generation and transmission lines up to their full capabilities without reduction in system stability and security. Another reason that is forcing the review of traditional transmission methods is the tendency of modern power systems to follow the changes in today's global economy that are leading to deregulation of electrical power markets in order to stimulate competition between utilities.

1.1.1 Flexible AC Transmission

Power flow is a function of transmission line impedance, the magnitude of the sending and receiving end voltages, and the phase angle between the voltages. By

controlling one or a combination of the power flow arguments, it is possible to control the active, as well as the reactive power flow in the transmission line.

In the past, power systems were simple and designed to be self-sufficient. Active power exchange of nearby power systems was rare as ac transmission systems cannot be controlled fast enough to handle dynamic changes in the system and, therefore, dynamic problems were usually solved by having generous stability margins so that the system could recover from anticipated operating contingencies.

Today, it is possible to increase the system loadability and hence security by using a number of different approaches. It is a usual practice in power systems to install shunt capacitors to support the system voltages at satisfactory levels. Series capacitors are used to reduce transmission line reactance and thereby increase power transfer capability of lines. Phase shifting transformers are applied to control power flows in transmission lines by introducing an additional phase shift between the sending and receiving end voltages.

In past days, all these devices were controlled mechanically and were, therefore, relatively slow. They are very useful in a steady state operation of power systems but from a dynamical point of view, their time response is too slow to effectively damp transient oscillations. If mechanically controlled systems were made to respond faster, power system security would be significantly improved, allowing the full utilization of system capability while maintaining adequate levels of stability. This concept and advances in the field of power electronics led to a new approach introduced by the Electric Power Research Institute (EPRI) in the late 1980. Called Flexible AC Transmission Systems or simply FACTS, it was an answer to a call for a more efficient use of already existing resources in present power systems while maintaining and even improving power system security. In [1], the authors introduced this new concept, initiating a new direction in power system research.

1.2 Basic Principles of Active and Reactive Power Flow Control

Active (real) and reactive power in a transmission line depend on the voltage magnitudes and phase angles at the sending and receiving ends as well as line impedance. To facilitate the understanding of the basic issues in power flow control and to introduce the basic ideas behind VSC-based FACTS controllers, the simple model given in [26] and shown in Figure 1.1(a) is used. The sending and receiving end voltages are assumed to be fixed and can be interpreted as points in large power systems where voltages are "stiff". The sending and receiving ends are connected by an equivalent reactance, assuming that the resistance of high voltage transmission lines is very small. The receiving end is modeled as an infinite bus with a fixed angle of 0^0.

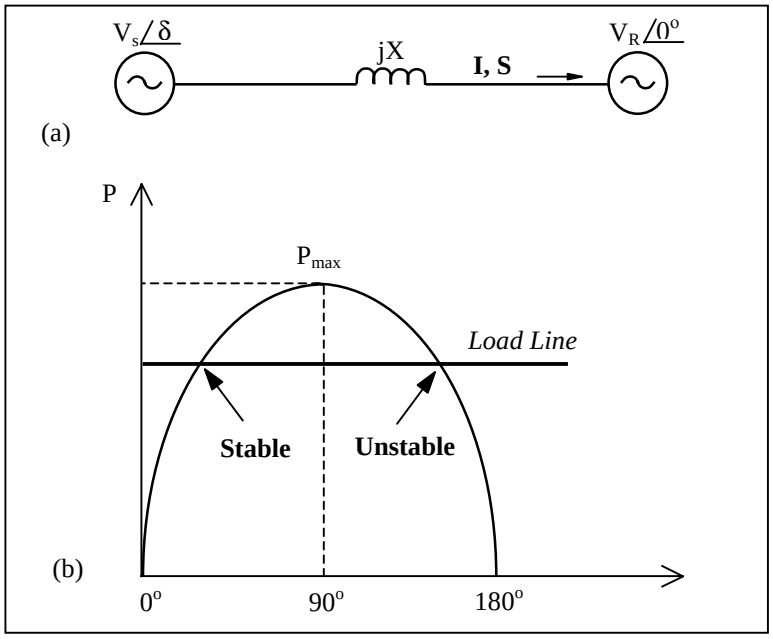


Figure 1.1 – (a) Model for calculation of real and reactive power flow
(b) Power angle curve for (a)

Complex, active and reactive power flows in this transmission system are defined, respectively, as follows:

$$\mathbf{S}_R = P_R + jQ_R = \mathbf{V}_R \mathbf{I}^* \tag{1.1}$$

$$P_R = \frac{V_S V_R}{X} \sin \delta \tag{1.2}$$

$$Q_R = \frac{V_S V_R \cos \delta - V_R^2}{X} \tag{1.3}$$

Similarly, for the sending end:

$$P_S = \frac{V_S V_R}{X} \sin \delta = P_{max} \sin \delta \tag{1.4}$$

$$Q_S = \frac{V_S^2 - V_S V_R \cos \delta}{X} \tag{1.5}$$

where V_S and V_R are the magnitudes (in RMS values) of sending and receiving end voltages, respectively, while δ is the phase-shift between sending and receiving end voltages.

The equations for sending and receiving active power flows, P_S and P_R, are equal because the system is assumed to be a lossless system. As it can be seen in Figure 1.1.(b), the maximum active power transfer occurs, for the given system, at a power or load angle δ equal to 90^0. Maximum power occurs at a different angle if the transmission losses are included. The system is stable or unstable depending on whether the derivative $dP/d\delta$ is positive or negative. The steady state limit is reached when the derivative is zero.

In practice, a transmission system is never allowed to operate close to its steady state limit, as certain margin must be left in power transfer in order for the system to be able to handle disturbances such as load changes, faults, and switching operations. As can be seen in Figure 1.1(b), the intersection between a load line representing sending end

mechanical (turbine) power and the electric load demand line defines the steady state value of δ; a small increase in mechanical power at the sending end increases the angle. For an angle above 90^0, increased demand results in less power transfer, which accelerates the generator, and further increases the angle, making the system unstable; on the left side intersection, however, the increased angle δ increases the electric power to match the increased mechanical power. In determining an appropriate margin for the load angle δ, the concepts of dynamic or small signal stability and transient or large signal stability are often used. By the IEEE definition, dynamic stability is the ability of the power system to maintain synchronism under small disturbance, whereas transient stability is the ability of a power system to maintain synchronism when subjected to a severe transient disturbance such as a fault or loss of generation [27]. Typical power transfers correspond to power angles below 30^0; to ensure steady state rotor angle stability, the angles across the transmission system are usually kept below 45^0 [26].

Closer inspection of equations (1.2) and (1.4) shows that the real or active power transfer depends mainly on the power angle; inspection of equations (1.3) and (1.5) shows that the reactive power requirements of the sending and receiving ends are excessive at high angles and high power transfers. It is also possible to conclude that reactive power transfer depends mainly on voltage magnitudes, with flows from the highest voltage to the lowest voltage, while the direction of active power flows depends on the sign of the power angle.

Equations (1.2) to (1.5) show that the power flow in the transmission line depends on the transmission line reactance, the magnitudes of sending and receiving end voltages and the phase angle between the voltages. The concepts behind FACTS controllers is to enable control of these parameters in real-time and, thus, vary the transmitted power according to system conditions. The ability to control power rapidly, within appropriately defined boundaries, can increase transient and dynamic stability, as well as the damping of the system. For example, an increase or decrease of the value of transmission line reactance X, as can be seen from equations (1.2) and (1.4), increases or decreases the value of maximum power transfer P_{max}. For a given power flow, a change

of X also changes the angle between the two ends. Regulating the magnitudes of sending and receiving ends voltages, V_S and V_R, respectively, can also control power flow in a transmission line. However, these values are subject to tight control due to load requirements that limit the voltage variations to a range between 0.95 and 1.05 p.u., and hence cannot influence the power flows in a desired range. From the equations of reactive power flow, (1.3) and (1.5), it can be concluded that the regulation of voltage magnitude has much more influence over the reactive power flow than the active power flow.

Of the FACTS controllers of interest here, the STATCOM has the ability to increase/decrease the terminal voltage magnitude and, consequently, to increase/decrease power flows in the transmission line. The SSSC controls power flow by changing the series reactance of the line, whereas the UPFC can control all these parameters simultaneously, i.e., the terminal voltage magnitude, the reactance of the transmission line and the phase angle between the sending and receiving end voltages.

It was shown that FACTS controllers can be used to control steady state active and reactive power flow, but it should be also noted that these fast controllers could have pronounced, positive impact on transient and dynamic conditions in a power system if designed properly. By appropriately using these FACTS controllers, it is possible to, for example, increase damping in power system. In [28], damping of power oscillations, caused by a nearby fault, is achieved by using feedback control to efficiently modulate active power flow on the transmission line through a UPFC. It is documented fact that the core of voltage instability is lack of reactive power support in a power system [26]; the STATCOM has the ability to control reactive power absorption/generation, and since its time response is very fast, sometimes even less than one cycle, it can be used to effectively prevent this problem.

1.2.1 Thyristor-Based FACTS Controllers

Developments in the field of high voltage power electronics have made possible the practical realization of FACTS controllers. By the 1970s, the voltage and current rating of GTOs had been increased significantly making them suitable for applications in high voltage power systems [2]. This made construction of modern Static Var Compensators (SVCs), Thyristor Controlled Series Capacitors (TCSCs), Thyristor Controlled Phase Angle Regulators (TCPARs), and many other FACTS controllers possible. A fundamental feature of the thyristor based switching controllers is that the speed of response of passive power system components such as a capacitor or a reactor is enhanced, but their compensation capacity is still solely determined by the size of the reactive component. For example, a SVC requires fully rated reactors and capacitors to absorb or generate reactive power, and a thyristor based electronic circuit rated for the sum of the maximum inductive and capacitive currents and voltages to control voltage magnitude in a power system. This arrangement has speeded up the response of the controller to approximately 1 cycle but the SVC still shows behavior similar to that shown by mechanically switched capacitor and reactor banks, as the reactive power generation changes with the change of the line voltage [3, 4, 5].

Series capacitors are connected in series with transmission lines to compensate for the inductive reactance of the line, increasing the maximum transmittable power and reducing the effective reactive power loss. Power transfer control can be done continuously and rather fast using, for example, the Thyristor Controlled Series Capacitors (TCSCs), making it very useful to dynamically control power oscillations in power systems [6]. However, the problem with these devices is that that it can form a series resonant circuit in series with the reactance of the transmission line, thus limiting the rating of the TCSC to a range of 20 to 70 % the line reactance. It has been also noted that since the line current is a function of the impedance and phase angle, the compensating voltage is also a function of these parameters, making the reactive power demand of the transmission line a direct function of the transmitted active power.

The TCPAR is used to control the power flow in a transmission line by controlling the magnitude of the injected voltage component in quadrature to the line current and thus control the phase angle between the sending and receiving end voltages. It is made up of two thyristor-controlled tap-changing transformers, resulting in high series impedance. A consequence of this relatively high impedance is that a TCPAR can consume significant amounts of reactive power at high power transfer levels; hence, a large power source must be located close to this device to insure adequate voltage regulation during contingencies. Although the use of thyristor switches can increase the speed of the TCPAR, the inherent high reactance of TCPAR can be a significant problem. Considering this issue, it is not surprising that the phase angle regulators have been infrequently used in power systems, even though they provide the system operator with certain degree of control over transmission line flows, which cannot be matched by any other existing device [7, 8, 9].

1.2.2 GTO-Based FACTS

A normal thyristor, which is basically a one-way switch, can block high voltages in the off-state and carry large currents in the on-state with only small on-state voltage drop [10]. The thyristor, having no current interruption capability, changes from on-state to off-state when the current drops below the holding current and, therefore, has a serious deficiency that prevents its use in switched mode applications. With the development of the high voltage, high current Gate Turn-Off thyristors (GTOs), it became possible to overcome this deficiency. Like the normal thyristor, a gate current pulse can turn on the GTO thyristor, while to turn it off, a negative gate-cathode voltage can be applied at any time. This feature and the improved ratings of GTOs made possible the use of Voltage-Sourced Converters (VSC) in power system applications [11].

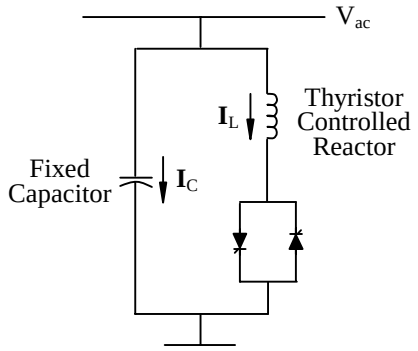
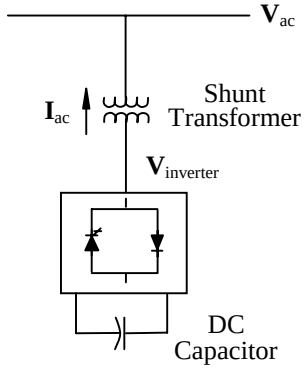
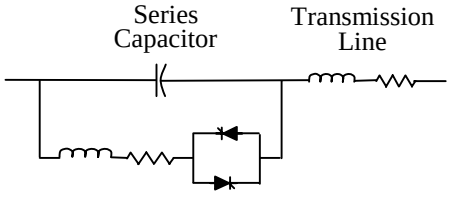
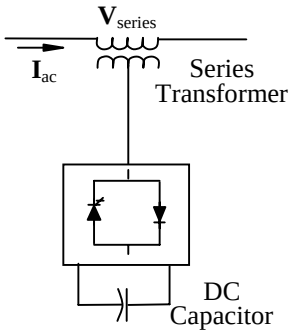
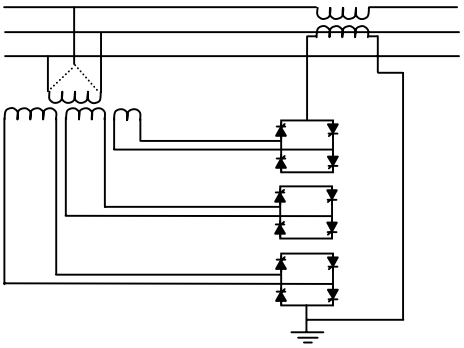
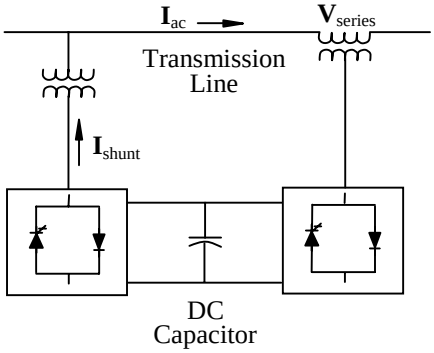
Voltage-sourced converters employ converters with GTOs or other turn-off devices, diodes and a dc capacitor to generate a synchronous voltage of fundamental frequency

and controllable magnitude and phase angle. If a VSC is connected to the transmission system via a shunt transformer, it can generate or absorb reactive power from the bus to which it is connected. Such a controller is called Synchronous Static Compensator or STATCOM and is used for voltage control in transmission systems [12]. The major advantage of a STATCOM, as compared to a SVC, is its reduced size, sometimes even to less than 50 %, and a potential cost reduction achieved from the elimination of capacitor and reactor banks as well as other passive components required by the SVC. Because of its smaller size, the STATCOM can be placed in large metropolitan areas where space is at a premium [13, 14]. For example, the complete STATCOM system installed at the Tennessee Valley Authority (TVA) Sullivan Substation is housed in one building of 27.4 m x 14.6 m; all of the related STATCOM equipment is located indoors, while the main transformer that connects the STATCOM to the transmission system is located outdoors [15].

If a VSC is employed as a series device by connecting it to the transmission line via a series transformer, it is called a Static Synchronous Series Compensator or simply SSSC. This controller can also generate or absorb reactive power from the line to which is connected and in that way change the series impedance of the line. It is convenient to think of the SSSC as being comparable to a continuously variable series capacitor or inductor, and, therefore, can be used to control the power flow in the transmission line [16,17].

A Unified Power Flow Controller (UPFC) can control transmission line impedance, voltage and phase angle. It has the capability of controlling with two-degrees of freedom, i.e. it can control inverter output voltage magnitude and phase angle and only the current rating of the device limits its output capabilities. This new device offers utilities the ability to control voltage magnitude in the system, control power flows, both steady-state and dynamic, on predefined corridors, allowing secure loading of transmission lines up to their full thermal capability [18, 19, 20, 21]. A summary of different FACTS controllers is given in Table 1.1

Table 1.1 – Summary of Different FACTS Controllers

	Thyristor Based Controllers	**VSC Based Controllers**
Shunt Compensation		
Series Compensation		
Phase Shifting		

A comparison of a VSC approach with the more conventional compensation method of employing thyristor switched capacitors and reactors shows the VSC's superior performance. The VSC's approach has a versatile applicability, smaller physical size, and can employ both reactive and real power compensation to counteract dynamic disturbance. It should be also mentioned that the VSC's compensation is independent of transmission system conditions, and that the real and reactive power of the transmission system can be controlled independently. Reference [18] provides an extensive discussion

of VSC-based FACTS controllers, particularly of the UPFC. A comparison of the UPFC with more conventional but related power flow controllers, such as TCSC and TCPAR, can be found in [19].

1.3 Shunt Reactive Power Compensation

Fixed or mechanically switched capacitors and reactors together with synchronous compensator have long been employed to increase steady state power transmission by controlling the voltage profile along the transmission lines. It has been demonstrated in [5, 13, 43] that both the transient and steady state stability (i.e., first swing stability and damping) of a power system can be enhanced if the compensation device can react quickly by using solid-state, thyristor switches and electronic control.

1.3.1 Static Var Compensator (SVC)

Advances in high power thyristor technology and electronics circuitry have prompted the development of controllable static var sources, often called var generators. Static Var Compensators or SVCs were developed in the late 1960s to provide fast, continuous or step like voltage control for large, fluctuating industrial loads, such as electric arc furnace [5]. They are primarily used to rapidly control voltage at a weak point in power transmission and large industrial networks. A controller regulating the ac system voltage with respect to a reference voltage with some droop characteristic varies the SVC current and reactive power. The droop value is selected according to the desired sharing of reactive power generation among various sources, as well as other needs of the system such as providing for an adequate margin for transient voltage stability.

Thus, a SVC presents a steady state and dynamic voltage–current characteristic as shown in Figure 1.2. The active control range of Figure 1.2 clearly defines the SVC operating range, showing the unfavorable characteristic of losing reactive support with decreasing terminal voltage in the capacitive range. The conventional SVC has no means

to transiently increase its var generation since the value of its maximum capacitance and the magnitude of the ac system voltage strictly determine the maximum capacitive current it can draw. The SVC has an increased transient rating in the inductive region only.

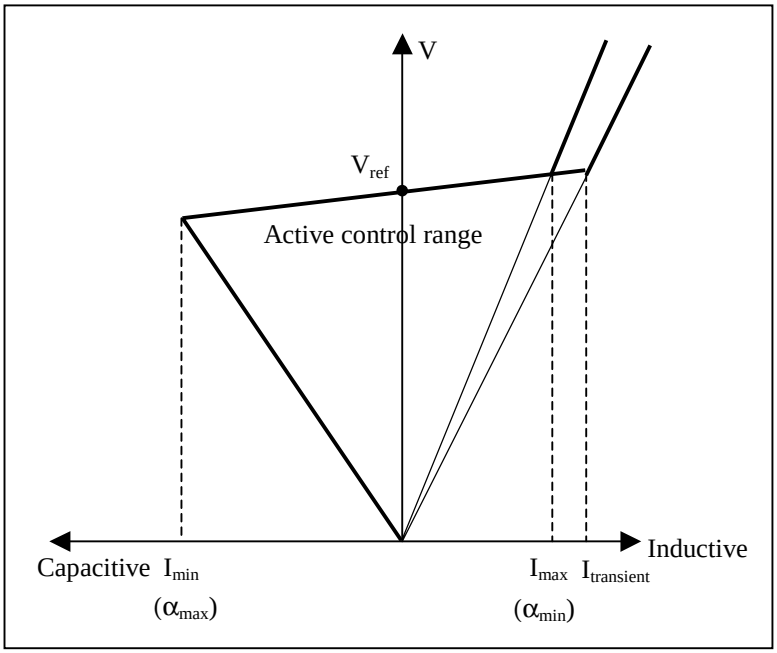


Figure 1.2 –Static var compensator (SVC) V – I characteristic

The capacitor banks in a SVC are rated for full capacitive output, whereas the reactor banks are rated for full inductive output; the coupling transformer and electronic circuit could be dimensioned to withstand the sum of the maximum capacitive and inductive output. It should be emphasized that the SVC capacity for compensation is solely determined by the size of its reactive components implying significant physical size and maintenance.

A SVC can control only one of the three principal parameters, voltage, phase angle, or impedance, which determines the power flow in ac power systems [42]. Therefore, it does not posses the capability to independently control active and reactive power in the transmission line.

1.3.2 STATCOM

The STATCOM V–I characteristic is shown in Figure 1.3. This characteristic shows the STATCOM ability to support a very low system voltage; down to about 0.15 per unit, which is the value associated with the coupling transformer reactance [2]. This is in strong contrast with that of a SVC, which at full capacitive output becomes an uncontrolled capacitor bank. A STATCOM can support system voltage at extremely low voltage conditions as long as the dc capacitor can retain enough energy to supply losses.

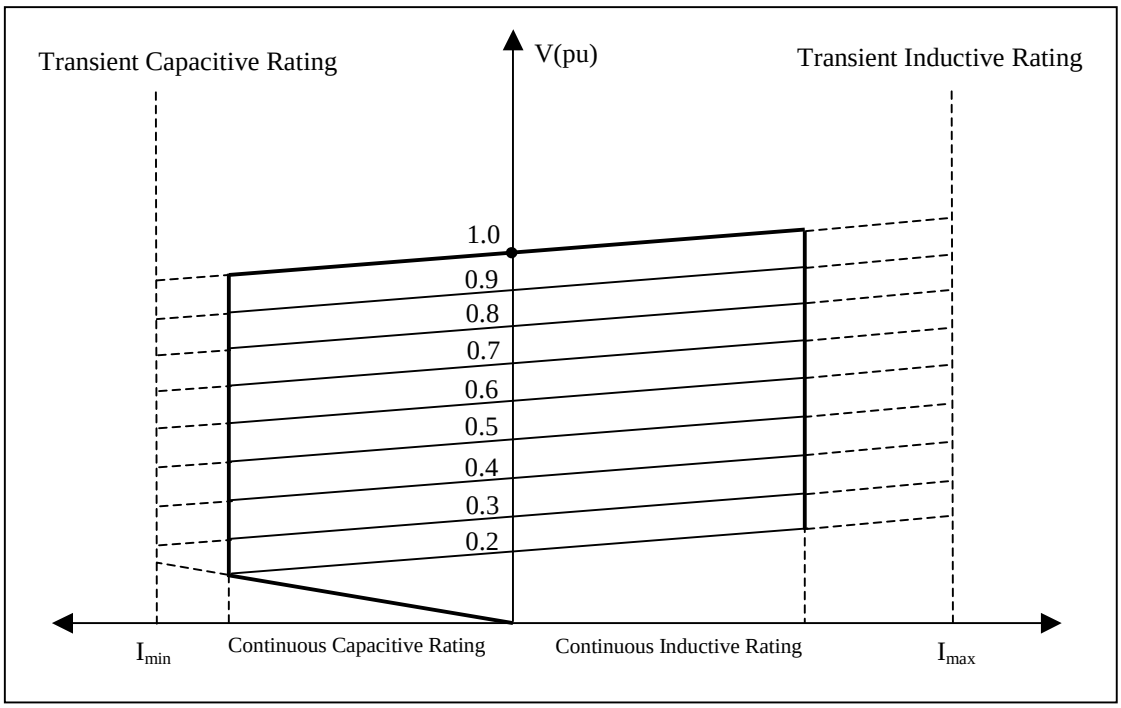


Figure 1.3 – STATCOM V- I characteristic

The STATCOM also has increased transient ratings in both capacitive and inductive regions. The overload capability is about 20 % for several cycles in both regions. It is also worth noticing that the inductive transient current rating is slightly larger due to fact that the GTOs, in the inductive region, are naturally commutated and hence the amount and duration of this temporary overload capability is limited by the maximum current of

the free-wheel diode. The capacitive transient rating is determined by the maximum current turn-off capability of the GTO thyristors.

1.3.3 Comparisons

Figure 1.4 shows a simple two-machine power system compensated at the midpoint by a STATCOM (Figure 1.4 (a)) and a SVC (Figure 1.4 (b)). For comparison, equivalent P-δ characteristics are shown for both controllers. As the output var rating of the controllers change, the P-δ characteristic shifts from the basic curve with no compensation to the curve with maximum midpoint compensation. The basic P-δ characteristic is defined by equation

$$P = \frac{V_R V_S}{X} \sin \delta = \frac{V^2}{X} \sin \delta \qquad (1.6)$$

assuming that the sending and receiving end voltage magnitudes are equal, i.e., $V_S = V_R = V$. The curve with maximum midpoint compensation is then represented by equation

$$P = 2 \frac{V^2}{X} \sin \frac{\delta}{2} \qquad (1.7)$$

The three curves between no compensation and maximum compensation curves correspond to three different controller outputs, from small to maximum output. The comparison between these curves for the STATCOM and SVC clearly shows that the STATCOM behaves as an ideal compensator until the maximum output current is reached. From this point, i.e., region $\pi/2 \le \delta \le \pi$, the STATCOM ability to provide maximum capacitive current independent of the system voltage and phase angle δ is

clearly an asset. The SVC response in the same region is characterized by a sharp decrease, as opposed to the STATCOM mild decline in transmitted power.

It can be also assumed that STATCOM would present better dynamic characteristics in a power system, since it has the ability to quickly react to a disturbance, typically within a few milliseconds. The STATCOM reactive power output inherently changes to compensate for changes in ac system bus voltages even before the control system response. In the SVC, the output current and bus voltage are highly dependent on the external network impedance, which is sensitive to resonance in the transmission system [14].

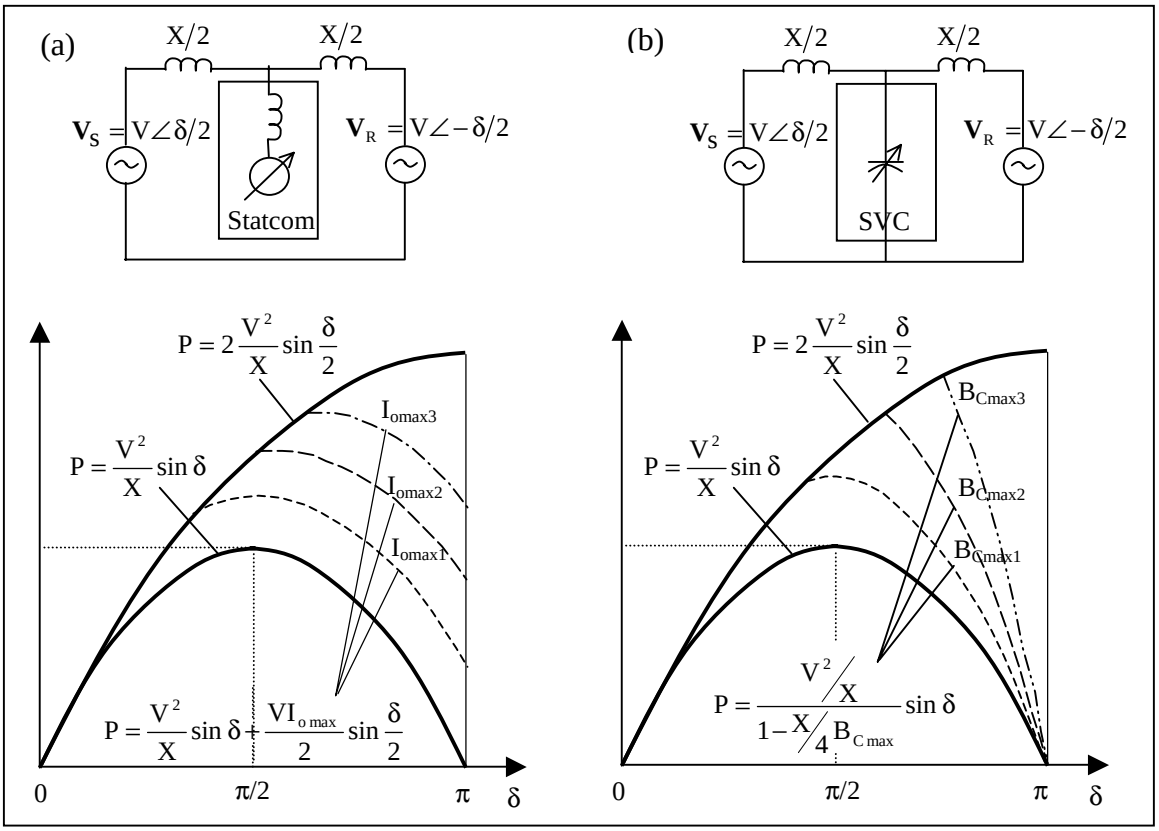


Figure 1.4 – P-δ characteristics with and without compensation:
(a) STATCOM's response, and (b) SVC's response [11]

Figure 1.5 shows the responses of both a STATCOM and a SVC to a fault that forces the real power P in the line to zero for the duration of the fault. This fault forces the sending end machine to accelerate, as it is unable to change its mechanical power set point in such a short period of time. This causes an increase in the machine torque angle from δ_o to δ_1 at the moment of fault clearance, resulting in an increase in the transmitted power, leading to a deceleration of the sending end machine, but the torque angle continues to increase due to the inertia until the machine loses all its kinetic energy gained during the fault. As it can be seen in Figure 1.5, the transient stability margin provided by a STATCOM placed at the midpoint of the power system is bigger than the margin obtained from a SVC in the system. This confirms superior performance of a STATCOM compared to a SVC with similar ratings.

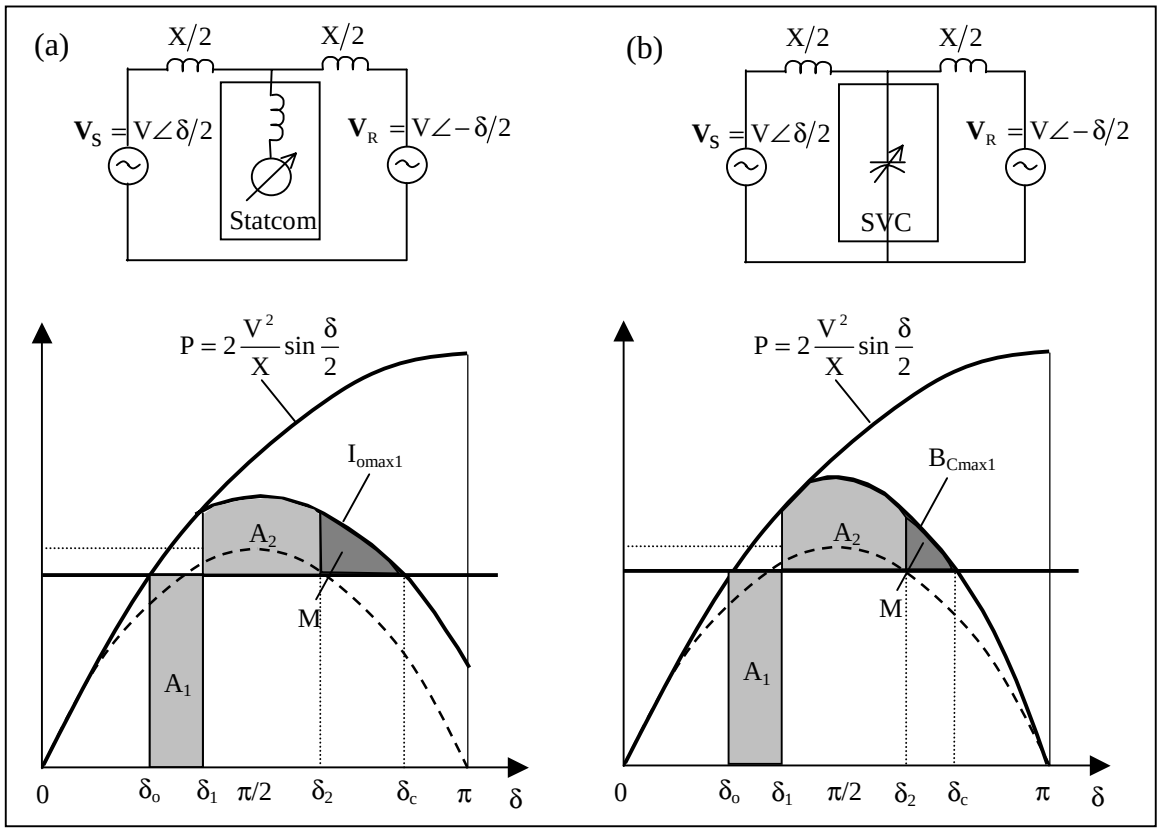


Figure 1.5 – Equal Area Criterion:
(a) STATCOM's margin, and (b) SVC's margin [11]

In general, a reduction of more than 50 % in the physical size of installation can be expected when a STATCOM is compared to a SVC. Furthermore, it has been shown that for steady state reactive support, a STATCOM is capable of supporting higher loads (some authors suggest 15 to 30 %) than what would be possible with a SVC of comparable Mvar rating [14]. It seems it is reasonable to assume that the number of STATCOM applications to power systems will continue to grow with the superior performance more than offsetting the high capital cost. Moreover, the choice will be further enhanced with the projected decrease in the cost of power electronic devices.

1.4 Series Reactive Power Compensation

Series reactive power compensation consists of controlling the reactive impedance of a transmission line to control line power flow. Series capacitive impedance was initially introduced to decrease the total line reactance and thus increases the power on the line; the series compensation in this case is fixed so there is no control over the transmittable power.

In the 1980s, the basic Thyristor Controlled Series Capacitor (TCSC) controller based on semiconductor switches was proposed to allow controllable series reactive power compensation. In this controller, one or more capacitor banks, each shunted with a thyristor-controlled reactor, are employed. The thyristor-controlled reactor variable current circulates through the capacitor bank affecting the compensating voltage; this current is a function of the conduction angle of the thyristor switch. The thyristor-controlled reactor can also be used to alter the low frequency impedance of the TCSC and to prevent subsynchronous resonance. In 1992, a GTO Thyristor Controlled Series Capacitor (GTCSC) was proposed. In both schemes, the final objective is to control the amount of series capacitive impedance by appropriate switching of the semiconductor devices.

The transmitted power in the TCSC or GTCSC compensated line can be expressed as:

$$P_{comp_{TCSC}} = \frac{V_S V_R}{X_L(1-k)} \sin\delta \qquad (1.8)$$

where $k = \frac{X_C}{X_L}$, and X_L is the transmission line reactance; δ stands for the transmission angle between the sending and receiving end voltages.

In 1989, the use of the VSC in series reactive power compensation was proposed, leading to the SSSC controller [52]. The SSSC can generate a controllable compensating capacitive or inductive voltage, which implies that the amount of transmittable power can be increased as well as decreased from the natural power flow. The SSSC output voltage is independent of the line current, as opposed to the voltage across the TCSC, which is a function of the line current that is a function of the transmission angle. Therefore, when the transmission angle changes, which varies in a power system, the compensating voltage of the TCSC also changes. Another SSSC advantage over the TCSC is that the SSSC cannot form a classical resonant circuit with the inductive line impedance that would lead to subsynchronous resonance problems.

The transmitted power in the SSSC compensated transmission line is a function of the injected voltage V_{pq} and, assuming a lossless transmission line, it can be expressed as:

$$P_{comp_{SSSC}} = \frac{V_S V_R}{X_L} \sin\delta + \frac{V_R V_{pq}}{X_L} \cos\frac{\delta}{2} \qquad (1.9)$$

Figure 1.6 shows the normalized power P versus angle δ plots as a function of V_{pq} and X_C. Comparison of the corresponding plots for the transmitted powers for SSSC and TCSC compensated transmission lines indicates that the series capacitor increases the transmitted power dependent on δ, while the SSSC can increase/decrease it independent of δ.

In [16], the authors present an economic comparison between the SSSC and TCSC series compensators. The ratio of the maximum range of attainable var output to the VA rating of the equipment is used as an indicator of cost effectiveness. The results show that the SSSC can double the series var compensation range per VA, accounting for the SSSC equal capacitive and inductive range; the TCSC is not able to provide symmetrical capacitive and inductive reactive compensation without additional power circuit elements. For every var of capacitive compensation, the TCSC capacitor banks and thyristor switches ratings have to be doubled, with respect to the SSSC. On the other hand, the SSSC requires a coupling transformer and a dc storage capacitor, whereas the TCSC is coupled directly to the transmission line. Thus, for the time being, the preliminary cost evaluation carried out by the authors indicates that the SSSC would be generally more cost effective than the TCSC. The SSSC cost is expected to go down even further in the future due to strong research and development in the semiconductor industry, which will lower the cost of the semiconductor switches.

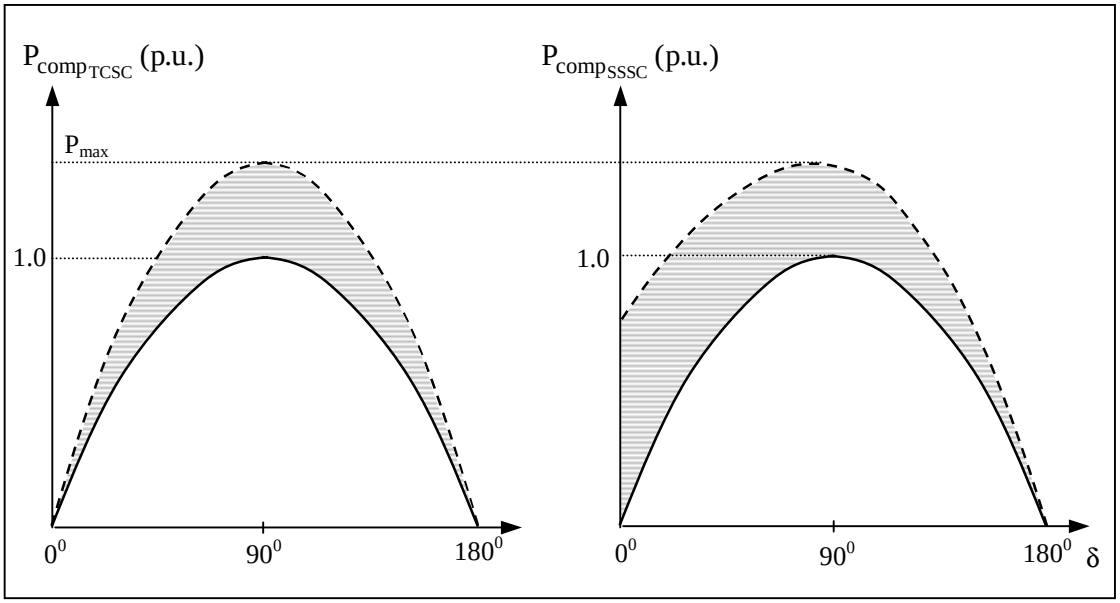


Figure 1.6 – Transmitted power versus transmission angle

1.5 Power Flow Control Using a UPFC

The UPFC is intended for real-time control and dynamic compensation of ac transmission systems. It has the ability to simultaneously and selectively control all of the parameters affecting flowing of the power in a transmission line, namely; voltage, impedance and phase angle. The UPFC can fulfill all these functions by adding the injected voltage $\mathbf{V_{SR}}$ to the sending end terminal voltage. The magnitude and phase angle of the series injected voltage $V_{SR}\angle\beta$ are control variables whose values depend on the control objective.

The control objectives may vary depending on intended the UPFC application. Figure 1.7(a) corresponds to a simple two-machine power system without compensation. The power flow is a function of the voltage magnitude of sending and receiving ends, the impedance of the transmission line and the power angle δ. The maximum transmitted power P_{max} occurs at $\delta=90^0$.

The UPFC can independently control both reactive and real power flow, and thus, can be used to regulate the system voltage profile. Figure 1.7(b) corresponds to the case where the UPFC is placed in the middle of a transmission line and the UPFC series branch is not operational, i.e., the UPFC operates as a STATCOM ($\mathbf{V_{SR}}=0$). The shunt converter generates the capacitive current needed to keep the midpoint voltage at $\mathbf{V_p=V_S=V_R}$. The power curve for this case shows that the maximum power occurs at $\delta=180^0$, and has an amplitude twice as large as that for the case without compensation.

Figure 1.7(c) depicts the case where the shunt converter is not operational and the series converter behaves as a SSSC. Thus, the series injected voltage $\mathbf{V_{SR}}$ acts as a series capacitor, resulting in increased transmission line current and the real power. The maximum power P_{max} depends on the degree of series compensation k ($0 \le k \le 1$). The maximum power P_{max} can be also decreased but injecting the series voltage that is phase with the transmission line inductance.

The UPFC can also behave as a phase shifter by controlling the amplitude of the series injected voltage so that the effective phase angle between the sending and receiving end voltages is controlled (Figure 1.7(d)). In this case, to get the desired power flow, the both converters must be operational and there is real power flow across the dc capacitance.

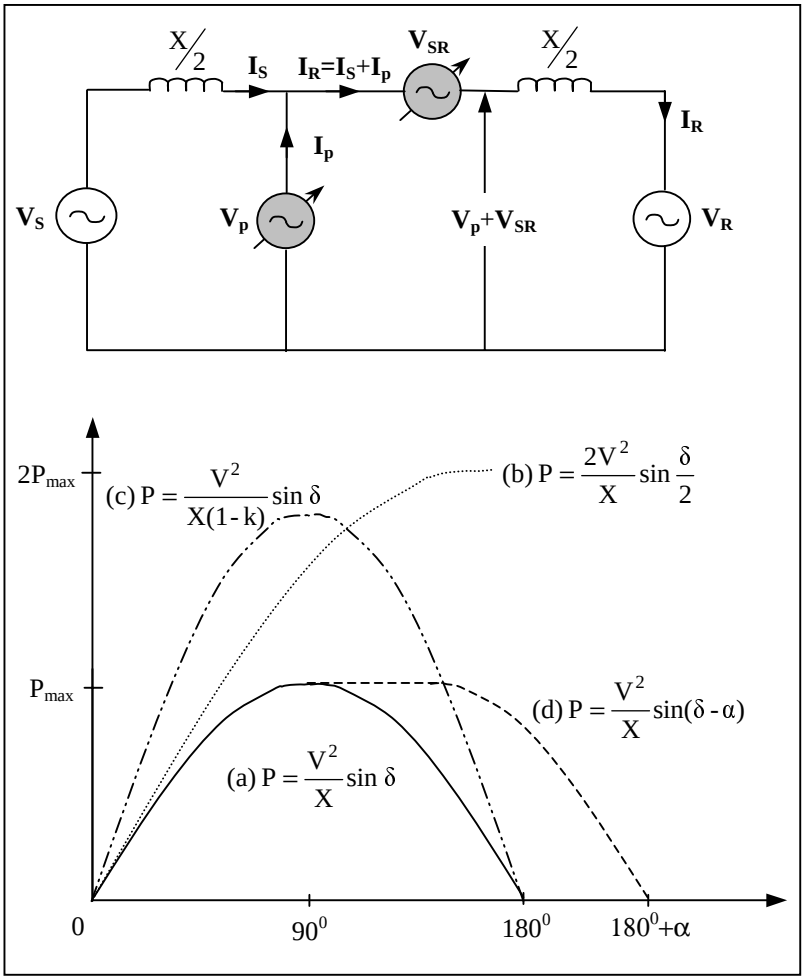


Figure 1.7 – Two-machine power system with a UPFC

For the system depicted in Figure 1.7, the transmitted real and reactive power at the receiving end can be expressed as follows:

$$P_R - jQ_R = \mathbf{V_R}\left(\frac{\mathbf{V_S} + \mathbf{V_{SR}} - \mathbf{V_R}}{jX}\right)^* = \mathbf{V_R}\left(\frac{\mathbf{V_S} - \mathbf{V_R}}{jX}\right)^* + \frac{\mathbf{V_{SR}^*}\mathbf{V_R}}{-jX} \qquad (1.10)$$

Hence, the following equations for the real and reactive power flow are:

$$P_R = P_{uncomp} + P_{comp} = \frac{V_R V_S}{X}\sin(\delta) - \frac{V_R V_{SR}}{X}\cos\left(\frac{\delta}{2} + \beta\right) \qquad (1.11)$$

$$Q_R = Q_{uncomp} + Q_{comp} = \frac{V_S V_R}{X}(1 - \cos(\delta)) - \frac{V_R V_{SR}}{X}\sin\left(\frac{\delta}{2} + \beta\right) \qquad (1.12)$$

where $\mathbf{V_S} = V_S \angle \delta/2$ and $\mathbf{V_R} = V_R \angle -\delta/2$.

The real power in the uncompensated transmission line can be expressed as:

$$P_{uncomp} = \frac{V_R V_S}{X}\sin(\delta) \qquad (1.13)$$

while the reactive power in the uncompensated transmission line is given by

$$Q_{uncomp} = -\frac{V_S V_R}{X}(1 - \cos(\delta)) \qquad (1.14)$$

On the other hand, from equations (1.11) and (1.12), the real and reactive power for the compensated line using the series voltage injection can be expressed:

$$P_{comp} = -\frac{V_R V_{SR}}{X}\cos\left(\frac{\delta}{2} + \beta\right) \qquad (1.15)$$

$$Q_{comp} = \frac{V_R V_{SR}}{X} \sin\left(\frac{\delta}{2} + \beta\right) \tag{1.16}$$

Equations (1.11) and (1.12) show that the real and reactive power flow are affected not only by the change of the injected voltage but also by the location of the UPFC and the phase angle between the sending and receiving end voltages. The maximum transmittable power is increased when the UPFC is located closer to the midpoint of the transmission line. Since the injected voltage angle β is controllable between 0 and 2π at any transmission angle δ, it follows that both compensated real and reactive powers are controllable between $-\frac{V_R V_{SR,max}}{X}$ and $\frac{V_R V_{SR,max}}{X}$. This implies that the minimum and maximum real and reactive power flow in the transmission line are [42]:

$$P_{uncomp} - \frac{V_R V_{SR,max}}{X} \le P_R \le P_{uncomp} + \frac{V_R V_{SR,max}}{X} \tag{1.17}$$

$$Q_{uncomp} - \frac{V_R V_{SR,max}}{X} \le Q_R \le Q_{uncomp} + \frac{V_R V_{SR,max}}{X} \tag{1.18}$$

From equations (1.17) and (1.18), it follows that the power control region is a circle with a centre defined by coordinates (P_{uncomp}, Q_{uncomp}) and a radius $\frac{V_R V_{SR,max}}{X}$. The boundary circle can be described by the following equation [67]:

$$\left(P_R - P_{uncomp}\right)^2 + \left(Q_R - Q_{uncomp}\right)^2 = \left(\frac{V_R V_{SR,max}}{X}\right)^2 \tag{1.19}$$

1.6 Proposed Research

1.6.1 Motivation

The need for flexible and fast power flow controllers in transmission systems is expected to grow in future. The integration of FACTS controllers in power system will increase in view of continuing improvements in GTO and other semiconductor technology. A collaboration of EPRI, TVA and the former Westinghouse Science and Technology Center resulted in a development of a ± 100 Mvar STATCOM which is already in service on the TVA 161 kV transmission system [15]. It has been reported in [21, 22, 23] that the American Electric Power Co. (AEP), a utility serving seven eastern US states, has already installed the first demonstrative UPFC; this UPFC was developed jointly by EPRI and the Westinghouse Electric Corp. A ± 320 MVA, 138 kV UPFC was commissioned for the AEP at the end of 1997. Another project involving a ± 200 MVA, 345 kV VSC is currently under development [24, 25]; the controller is called a Convertible Static Compensator and it is about to be installed by the New York Power Authority (NYPA).

The implementation of any of the new FACTS controllers is not an easy task. Although they offer substantial advantages for steady state and dynamic operation by controlling the power flow in the transmission line, it brings major challenges in power electronics, device control and protection design. There are some issues that must be addressed in contemplating the installation of a new FACTS controller:

- The initial task is to identify clearly the potential applications and benefits for the designated utility. In order to accomplish this task, a number of possible sites should be investigated.

- After an appropriate steady state model for the device has been developed, steady state power flow simulations should be performed to determine the rating and benefits of the controller in a number of chosen sites.

- Dynamic and transient stability simulations should be performed to evaluate the behavior of the controller under certain operating conditions. Various control schemes should be evaluated to find the most beneficial one.

1.6.2 Research Objectives

FACTS application studies require careful planning and coordination in the specification, design and operating stage of a project. As a prerequisite, it is essential that a suitable plan, which identifies the purpose, objective, methodology and criteria for the studies, is prepared. Before meaningful results can be expected from application studies, representative models for the transmission system and relevant FACTS controllers need to be established and verified.

This means that analytical tools that enable the full potential of these controllers to be studied should support emerging FACTS technology. These tools used to determine steady state, dynamical and transient behavior of FACTS controllers consist mainly of physical and digital simulations. Physical simulations of a reduced system, for example TNA studies, allow adequate representation of the real controller, with real time control and performance of some system components. However, its application is limited, due to restrictions in terms of the extent of the ac system representation, and it may be uneconomical depending on availability and overhead costs.

On the other hand, digital simulations have become increasingly reliable for assessing both steady state and dynamic performance of a power system, due to the development of general purpose simulation programs, providing cost effective and feasible ways to model the system. This does not mean that physical simulations are completely outdated; in fact simulator studies are often undertaken before the actual installation.

In current practice, power flow programs are used in planning studies to assess steady state power flows and voltages in a power system for specified terminal and bus conditions. Additionally, these studies provide initial conditions for transmission system dynamic and transient stability studies. The power flow results are also used to establish steady state ratings and to identify appropriate locations for installing a particular FACTS controller to best meet study goals, and to reduce the number of alternatives under investigation. Simplified and reliable models, which take into account steady state limits of the transmission system and FACTS controllers, are essential, so that preliminary assessments of the technical and economic benefits associated with each of the alternatives being studied can be done.

Stability studies such as dynamic and transient stability studies are typically performed during the planning stage to identify limiting conditions, and to assess the extent to which a FACTS controller may enhance dynamic performance of a power system. Typical studies would include voltage stability, control strategies as well as fault response. Accepting that a particular FACTS controller should be accurately modeled, so that all dynamic and control limits of the device are properly represented, the main research objectives and contributions of this thesis are:

- The discussion in detail of the modeling and simulation of VSC-based FACTS controllers, i.e., STATCOM, SSSC and UPFC. The basic functions of the controllers are established by comparing them with other FACTS controllers.

- The implementation of detailed three phase models of the STATCOM, SSSC and UPFC in the Electromagnetic Transient Program (EMTP), including control circuits with firing pulses for each of the semiconductor valves. These models are used as a bench mark to validate proposed fundamental frequency models for stability studies.

- Fundamental frequency models of the STATCOM, SSSC and UPFC are proposed and their validation is carried using the EMTP. To demonstrate the full potential of the controllers under dynamic conditions, a realistic 11-bus test system is used to

simulate a three-phase fault in close proximity to the particular controller under investigation. The validity and applicability of the models for different kinds of dynamic studies are discussed, particularly in voltage stability and balanced fault studies, as the developed models are symmetrical.

- Steady state models of the STATCOM, SSSC and UPFC are developed according to the fundamental frequency models. These models properly reflect the steady state operation of the controllers, including all operating limits.

1.7 Thesis Outline

In Chapter 2, the VSCs are briefly explained, together with main circuit configurations, functions and general control strategies. Simple six-pulse, twelve-pulse and PWM-controlled VSCs are modeled in EMTP and their basic output waveforms are shown. This chapter gives a technical introduction into FACTS technology and the main research is presented later in this thesis.

Chapter 3 concentrates on the use of a solid-state VSC for shunt compensation in a power system. This shunt connected FACTS controller is called Synchronous Static Shunt Compensator or simply STATCOM. The operating principles and the EMTP implementations of twelve-pulse and PWM STATCOM are explained in Chapter 3. Also, the respective control systems are designed and explained in this chapter.

Chapter 4 addresses the problem of controlling and modulating power flow in a transmission line using a SSSC. The EMTP simulation studies, which include a detailed representation of the twelve-pulse and PWM-controlled SSSC, are conducted and results are given in this chapter.

The main objective of Chapter 5 is to explain a Unified Power Flow Controller (UPFC) operation and its modeling in EMTP. The theory and design of various control

functions of the UPFC are also presented along with the EMTP simulation results of a PWM-controlled UPFC. A novel control objective for the series converter of a UPFC is given here, as well as the comparison between three different control objectives and designs for the series converter control.

Chapter 6 concentrates on describing and validating transient stability and power flow models of the STATCOM, SSSC and UPFC. Final conclusions on the research presented in this thesis are given in Chapter 7.

Chapter 2.

BASIC OPERATING PRINCIPLES OF VOLTAGE-SOURCED CONVERTERS

2.1 Introduction

The main objective of this chapter is to give an insight in the operating principles of Voltage-Sourced Converters (VSC) and no new theory or operation improvement is presented at this stage. The VSC operation is briefly explained, together with main circuit configurations, functions and general control strategies. The EMTP is used to provide basic VSC waveforms for six-pulse, twelve-pulse and PWM operation of a VSC.

2.2 High Power Gate Turn-Off Semiconductor Devices

It should be noted that there are two basic categories of self-commutating converters; a Voltage-Sourced Converter (VSC), which is fed with a dc voltage source across its dc terminals, and a Current Source Converter (CSC), which has a dc current source connected to its dc side. Their output waveforms are different too; a VSC generates voltage at its ac terminals, while a CSC has a current as its generated output. In general, these converters behave as voltage or current sources capable of generating output waveform of different magnitude and phase angle. In CSC, direct current always is unidirectional while the power reversal takes place through reversal of dc voltage polarity, to achieve this the CSC implementation requires semiconductor switches with symmetrical bi-directional voltage blocking capability. On the other hand, in a VSC, the dc voltage always has one polarity while the power reversal is achieved by reversal of dc current and, therefore, the VSC requires only unidirectional voltage blocking. For reasons of performance and economics, voltage source converters are preferred over

current source converters for FACTS application and, in this thesis, only voltage source converters will be used and discussed.

It should be noted that in order to be able to produce the desired output waveforms, the semiconductor switches in the VSC must have an intrinsic turn-off capability, or an auxiliary circuit has to be provided to produce "forced commutation". These fully controllable semiconductor switches are also called bimodal switches in which current flow can be both initiated and extinguished by gate control. In 1981, force-commutated thyristors were used to develop a first 20 Mvar static var compensator for experimental purposes. Later, significant advances in GTO thyristor development and the voltage and current ratings of the available devices have made it possible to built a first 1 Mvar demonstration model of static var compensator that was, at the time, called the Advanced Static Var Generator (ASVG) [12]. This ASVG used GTO thyristors in a voltage-sourced converter scheme to produce reactive power without the large capacitor or reactor banks usually required by conventional static var compensators.

The voltage and current capabilities of the GTO have been increasing continuously and, today, high power GTOs up to 6000 V and 6000 A ratings are commercially available [2]. To obtain the power ratings of VSC typically required for transmission system applications, presently available GTOs of limited current ratings have to be operated with a high dc voltage and, therefore, must be connected in series. The hard drive GTO technology allows the robust connection of a relatively high number of GTOs in series to form a turn-off valve required for high voltage VSC. The disadvantages of GTO thyristors are high switching losses and significant losses in required snubber circuits, thus the switching frequency is limited to a maximum frequency of about 300 to 500 Hz [29]. However, new advances in high power semiconductor switches have brought a whole family of new semiconductor switches with turn-off capabilities such as Insulated Gate Bipolar Transistors (IGBT), MOS Turn-Off Thyristor (MTO), Emitter Turn-Off Thyristor, and Integrated Gate-Commutated Thyristors (IGCT).

The IGBT is of some importance to FACTS controllers, since it has progressed to become a choice in a wide range of low and medium power applications going up to a few tens of megawatts. The advantages of this semiconductor device are its fast turn-on and turn-off capabilities, and thus can be used in Pulse Width Modulation (PWM) converters operating at high frequency. On the other hand, being a transistor device, it has higher forward voltage drop, but low switching losses and good current limiting capability.

The evolution of the GTO into MTO, ETO, and IGCT has introduced a family of new turn-off thyristor devices to consider in FACTS applications. The MTO has been recently invented by Silicon Power Corporation and has a good potential for use in medium to high power industrial and FACTS applications. It uses transistors to assists in turn-off capability and, therefore, has low switching losses. It also overcomes the limitations of the GTO regarding its drive power, snubber circuits, and dv/dt limitations [30].

The ETO has been recently developed at Virginia Power Electronics Center and incorporates the virtues of the thyristor and the transistor together [30]. It has fast turn-off capabilities and low switching losses, and greatly reduces the costs regarding gate drive and snubber circuits while still having the high power capability of a GTO.

The IGCT, developed by Mitsubishi and ABB, is an optimum combination between thyristor and GTO technology with low cost, low complexity and high efficiency characteristic [31]. It achieves fast turn-off and has low turn-off switching losses, and it is expected that it will soon replace the conventional GTO in high power FACTS applications. The IGCTs will be the key component for future medium to high-voltage applications from 0.5 MVA up to 100 MVA. The proof for that could be the first application of high power IGCT inverter in a 100 MVA intertie installation [32], in commercial operation since mid-1996 in Germany.

These high power semiconductor switches with turn-off capability are more expensive and have higher losses than thyristors without turn-off capability; however, they enable converter concepts that can have significant impact on overall system cost and many performance advantages. Therefore, it is important for the designers of FACTS controllers to be aware of the power semiconductor options, state of the device technology and future trends. The availability and performance characteriscs of power semiconductor switches will have a great influence over circuit and control design. For example, power semiconductor switches with low turn-on and turn-off losses and high switching frequency would be considered for an application in PWM converters. On the other hand, these switches have lower power ratings and, therefore, are limited to low and medium power applications. Power semiconductor switches with higher losses and lower switching frequency, but with higher power rating, would be considered for circuit concepts that need, for example, only one turn-on and turn-off per cycle.

2.3 Basic Operating Principles of Voltage-Sourced Converter

2.3.1 Basic Circuit Configuration

VSC transforms, through appropriate switching sequence, dc voltage at its dc terminals into an ac voltage of controllable frequency, magnitude and phase angle at its ac terminals. The output voltage could be fixed or variable, at a fixed or variable frequency. For FACTS application purposes, it is always assumed that the output voltage waveform has a fixed frequency equal to the fundamental frequency of a power system to which the converter is connected, as high voltage and power harmonics could create many problems.

Varying the input dc voltage and maintaining the gain of the converter constant, it is possible to obtain an output voltage of variable magnitude. In these converters, the input dc voltage is controlled in order to control the magnitude of the output ac voltage. The output ac voltage has a waveform similar to a square wave, and hence these converters

are called square-wave converters. Their drawback is that the output voltage waveform presents low order harmonics requiring some type of filtering, as discussed later in this Chapter, to get an output voltage of sufficiently high fundamental frequency component. Also, the output voltage magnitude can be controlled within some limited range that depends on the range of control of the dc voltage, i.e., it depends on the dc capacitor voltage and current ratings. The dc voltage should not exceed the maximum voltage rating of the dc capacitor and should be constantly above a certain level to avoid thyristor firing failure due to low voltage conditions.

On the other hand, keeping the input dc voltage fixed and varying the gain of the converter can control the converter output voltage. This kind of control of the output voltage magnitude is normally accomplished by Pulse-Width-Modulation (PWM) control; the converter gain in this case is defined as the ratio of the ac output voltage to the dc input voltage. There are various schemes to pulse-width-modulate the converter switches in order to shape the output ac voltage to be as close to a sine wave as possible. Currently, PWM control is still considered uneconomical in high power applications due to high switching losses and unavailability of fast switching turn-off capable switches, but with further improvements in high voltage power electronics this technique should become more competitive.

The converter dc terminals are connected to a dc capacitor whereas the ac side is connected to a power system through a transformer. The dc capacitor is assumed to be large enough to sustain changes in dc current without changes in the dc voltage and basically, at steady state operation, can be considered as a dc voltage source. The transformer plays two different roles: it connects the converter to the high voltage power system, while the transformer inductance ensures that dc capacitor is not short-circuited and discharged rapidly.

The three-phase VSC, shown in Fig. 2.1 in its simplest circuit configuration for FACTS application, is a two-level bridge composed of six valves. Each valve is made of semiconductor turn-off capable switches and an antiparallel diode. The switches should

be designed only for forward blocking voltage, as the diodes ensure that the voltage polarity of each switch is unidirectional. However, each converter arm, made of two valves, can conduct current in both directions, providing the converter with the capability to behave as an inverter or a rectifier.

The current is assumed positive if it flows from the ac to the dc side (a rectifier operation); the current is assumed to be negative when it flows from the dc to the ac side (an inverter operation). On the ac side, depending on the connection of the converter transformer, the output voltage of the converter can be connected in parallel or in series with the power system. If the converter is connected in parallel to the ac system, i.e. STATCOM operation, it is used to introduce capacitive or inductive current into the power system to regulate voltage. The converter in series with transmission line is used to introduce a phase-shifted voltage to regulate the total voltage drop/rise in the line, and to consequently regulate real/reactive power flow.

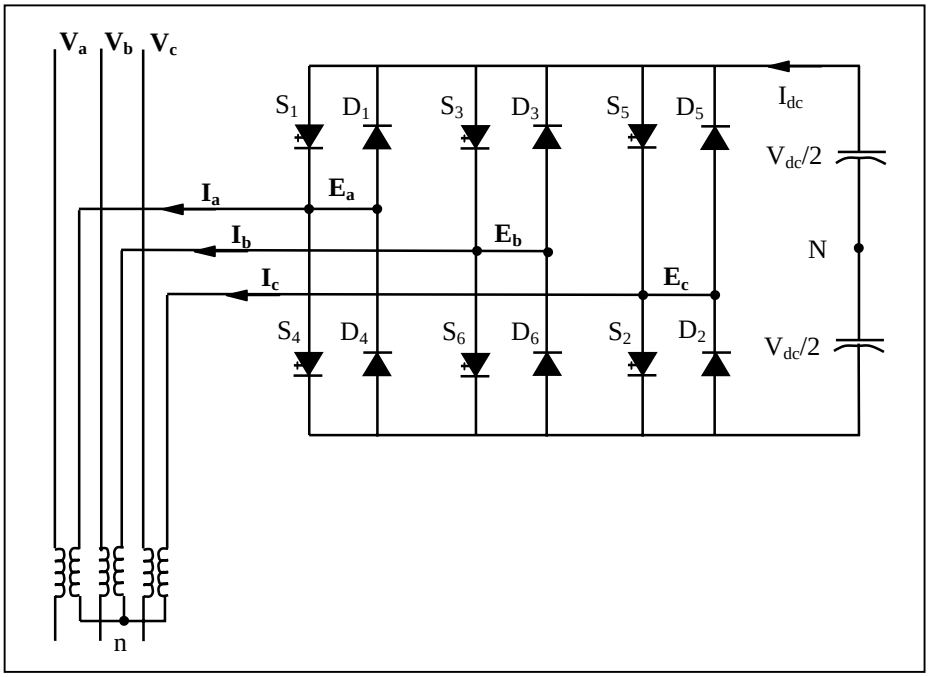


Figure 2.1 – Three-phase, two-level VSC circuit

2.3.2 Operating Principles and Basic Relationships

In the three-phase, two-level VSC of Figure 2.1 there are six controlled switches (for example GTO switches) to shape the converter output voltage from the input dc voltage. There are also six uncontrolled switches (diodes) to provide a path for inductive current whenever the controlled switch in the same leg is switched off. The ac current is the result of interaction of the converter output voltage with the ac system and can have any phase relationship with respect to the voltage. It is necessary for a VSC like this to never have two switches on at the same time, in any leg. Since there are three converter legs for three phase voltages, each 120^0 apart, there are always three switches on at the same time, one on each phase leg. To satisfy system requirements, there is always a complete conduction path between the dc capacitor and the ac system. It should be mentioned that there is never a sequence where three controlled switches, one on each phase, conduct at the same time. It is always a combination of two controlled switches and one uncontrolled switch conducting and vice versa. As a mater of fact, the switching pattern changes every 30^0 as indicated in Table 2.1.

Table 2.1 - Switching pattern for three-phase two-level VSC

PERIOD in degrees	**CONDUCT phase A**	**CONDUCT phase B**	**CONDUCT phase C**
0 – 30	D1	D6	**S5**
30 – 60	D1	**S6**	**S5**
60 – 90	D1	**S6**	D2
90 – 120	**S1**	**S6**	D2
120 – 150	**S1**	D3	D2
150 – 180	**S1**	D3	S2
180 – 210	D4	D3	S2
210 – 240	D4	**S3**	S2
240 – 270	D4	**S3**	D5
270 – 300	**S4**	**S3**	D5
300 – 330	**S4**	D6	D5
330 – 360	**S4**	D6	**S5**

Each valve is closed for 180^0, as described in Table 2.1 and shown later in the waveform v_a of Figure 2.3. The waveform shows a square-wave waveform representing voltage of ac bus phase *a* with respect to hypothetical dc capacitor midpoint N, with peak voltages of $+V_{dc}/2$ and $-V_{dc}/2$. In Table 2.1, from 0^0 to 180^0, the upper valve D1 and S1 conducts while the lower valve D4 and S4 conducts from 180^0 to 360^0. Three legs have their timing 120^0 apart; the upper valve D3 and S3 in the leg of phase *b* starts conducting 120^0 after the leg of phase *a*, while the upper valve D5 and S5 in the leg of phase *c* waits for 240^0 to start with its conduction. The Fourier analysis of phase voltage v_a, which is basically a periodical square wave with amplitude $V_{dc}/2$, shows a waveform composed of odd harmonics including third and its multiples harmonics.

$$v_a(t) = \frac{4}{\pi}\left(\frac{V_{dc}}{2}\right)\left[\cos \omega t - \frac{1}{3}\cos 3\omega t + \frac{1}{5}\cos 5\omega t - \frac{1}{7}\cos 7\omega t + \cdots\right] \qquad (2.1)$$

Figure 2.2 shows the phase *a*, *b*, and *c* connections to the dc capacitor for the interval 0^0 to 30^0, when switches D1, D6 and S5 are switched on (see Table 2.1). From this equivalent circuit, the currents and voltages associated with each phase can be determined. It is assumed that the transformer resistance is negligible; the load connected to the converter output terminals can also be assumed to be purely inductive. The arrangement of the two parallel inductances of phase *a* and *c*, as shown in Figure 2.2 (a), in series with the inductance of phase *b*, gives unequal voltage division.

The complete voltage pattern for each phase is given in Table 2.2. The waveform of phase to neutral converter output voltage for phase *a*, i.e. v_{an}, is shown in Figure 2.3. It deviates from the desired sinusoidal shape. This voltage is calculated by subtracting the voltage of the transformer floating neutral with respect to the ground v_n, shown in Figure 2.3, from the phase voltage with respect to dc neutral v_a.

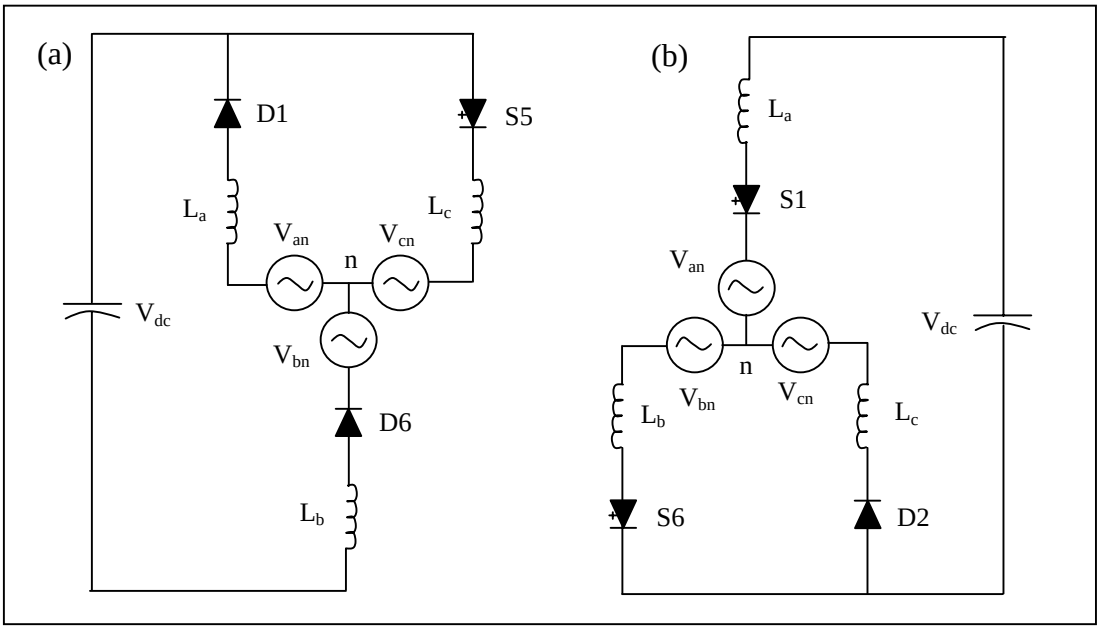


Figure 2.2 – Equivalent circuits

(a) Period 0^0 - 30^0 (b) Period 90^0 - 120^0

Table 2.2 - Switching pattern for phase-to-neutral voltages

PERIOD in degrees	**Voltage V_{an}**	**Voltage V_{bn}**	**Voltage V_{cn}**
0 – 30	$+V_{dc}/3$	$-2V_{dc}/3$	$+V_{dc}/3$
30 – 60	$+V_{dc}/3$	$-2V_{dc}/3$	$+V_{dc}/3$
60 – 90	$+2V_{dc}/3$	$-V_{dc}/3$	$-V_{dc}/3$
90 – 120	$+2V_{dc}/3$	$-V_{dc}/3$	$-V_{dc}/3$
120 – 150	$+V_{dc}/3$	$+V_{dc}/3$	$-2V_{dc}/3$
150 – 180	$+V_{dc}/3$	$+V_{dc}/3$	$-2V_{dc}/3$
180 – 210	$-V_{dc}/3$	$+2V_{dc}/3$	$-V_{dc}/3$
210 – 240	$-V_{dc}/3$	$+2V_{dc}/3$	$-V_{dc}/3$
240 – 270	$-2V_{dc}/3$	$+V_{dc}/3$	$+V_{dc}/3$
270 – 300	$-2V_{dc}/3$	$+V_{dc}/3$	$+V_{dc}/3$
300 – 330	$-V_{dc}/3$	$-V_{dc}/3$	$+2V_{dc}/3$
330 – 360	$-V_{dc}/3$	$-V_{dc}/3$	$+2V_{dc}/3$

As shown in Table 2.2, the phase to neutral output voltage consists of steps of $V_{dc}/3$ and it is free from triple harmonics, i.e.,

$$v_{an} = \frac{4}{\pi}\left(\frac{V_{dc}}{2}\right)\left[\cos\omega t + \frac{1}{5}\cos 5\omega t - \frac{1}{7}\cos 7\omega + \frac{1}{11}\cos 11\omega - \cdots\right] \qquad (2.2)$$

The phase-to-phase voltage v_{ab}, shown in Figure 2.3, is shifted by 30^0 with respect to v_{an}, and its amplitude is $\sqrt{3}$ times the amplitude of v_{an}. For example, for the interval 0^0 – 30^0, the phase-to-phase voltage v_{ab} can be constructed as:

$$v_{ab} = v_{an} - v_{bn} = \frac{V_{dc}}{3} - \left(-\frac{2V_{dc}}{3}\right) = V_{dc} \qquad (2.3)$$

The instantaneous phase-to-phase voltage v_{ab} can be expressed as a Fourier series which does not include even, third and multiples of third harmonics:

$$v_{ab} = \sqrt{3}\frac{4}{\pi}\left(\frac{V_{dc}}{2}\right)\left[\cos\omega t - \frac{1}{5}\cos 5\omega t + \frac{1}{7}\cos 7\omega t - \frac{1}{11}\cos 11\omega t + \cdots\right] \qquad (2.4)$$

The phase-to-phase rms voltage is given by:

$$V_{LL} = \sqrt{\frac{2}{2\pi}\int_0^{2\pi/3} V_{dc}^2 \, d(\omega t)} = \sqrt{\frac{2}{3}}V_{dc} = 0.8165V_{dc} \qquad (2.5)$$

The process of energy transfer from the ac to dc side and vice versa in a voltage-sourced converter is direct, i.e., the net instantaneous power at the ac terminals must always be equal to the net instantaneous power at the dc terminals, if the losses in the circuit are neglected. If a relatively small dc capacitor is connected across the input terminals of the converter, the converter keeps the dc capacitor charged to required levels. This is accomplished by making the converter output voltage lag the ac system

voltage, so that the converter absorbs a small amount of real power from the ac system to cover its internal losses and keep the capacitor voltage at desired levels. The same mechanism can be used to decrease the dc capacitor voltage by making the converter output voltage lead the ac system voltage. If the converter output voltage and the ac system voltage are made to be perfectly in phase, then the average dc voltage does not change. The dc capacitor voltage V_{dc} is shown in Figure 2.3.

In Figure 2.4, the current waveforms through the controlled and uncontrolled switches of phase *a* are shown, together with the phase current i_a and dc current I_{dc}. It was already stated before that the switches in the same phase leg cannot be turned on simultaneously. This can be observed in the current waveforms for valves 1 and 4 in the phase leg *a*. If both switches on a given leg are on, the dc capacitor would be short-circuited and a fast discharge of the dc capacitor would destroy the switches. Since the ac current is the result of the interaction between the converter generated ac voltage and the ac system voltage and impedance, the commutation from a controlled switch to a diode would occur naturally, so that the ac current is not interrupted. This can be seen clearly in Figure 2.4, as the current is transferred from the controlled switch GTO1 to diode D1 in the negative half cycle and from GTO4 to D4 in the positive half cycle. In this case, since the circuit is purely inductive, each controlled switch and diode within a valve carries alternately a 90^0 segment of the ac current in each cycle. This implies that the current ratings of the controlled switch and diode are the same.

It is also important to notice that the controlled switch has to be turned off at the peak of the current when the output is capacitive. This takes place when the converter output voltage exceeds the ac system voltage, and the current leads the converter output voltage by 90^0 (the circuit losses are neglected). In the case of inductive operation, the controlled switch commutates naturally, i.e. when the ac current drops to zero.

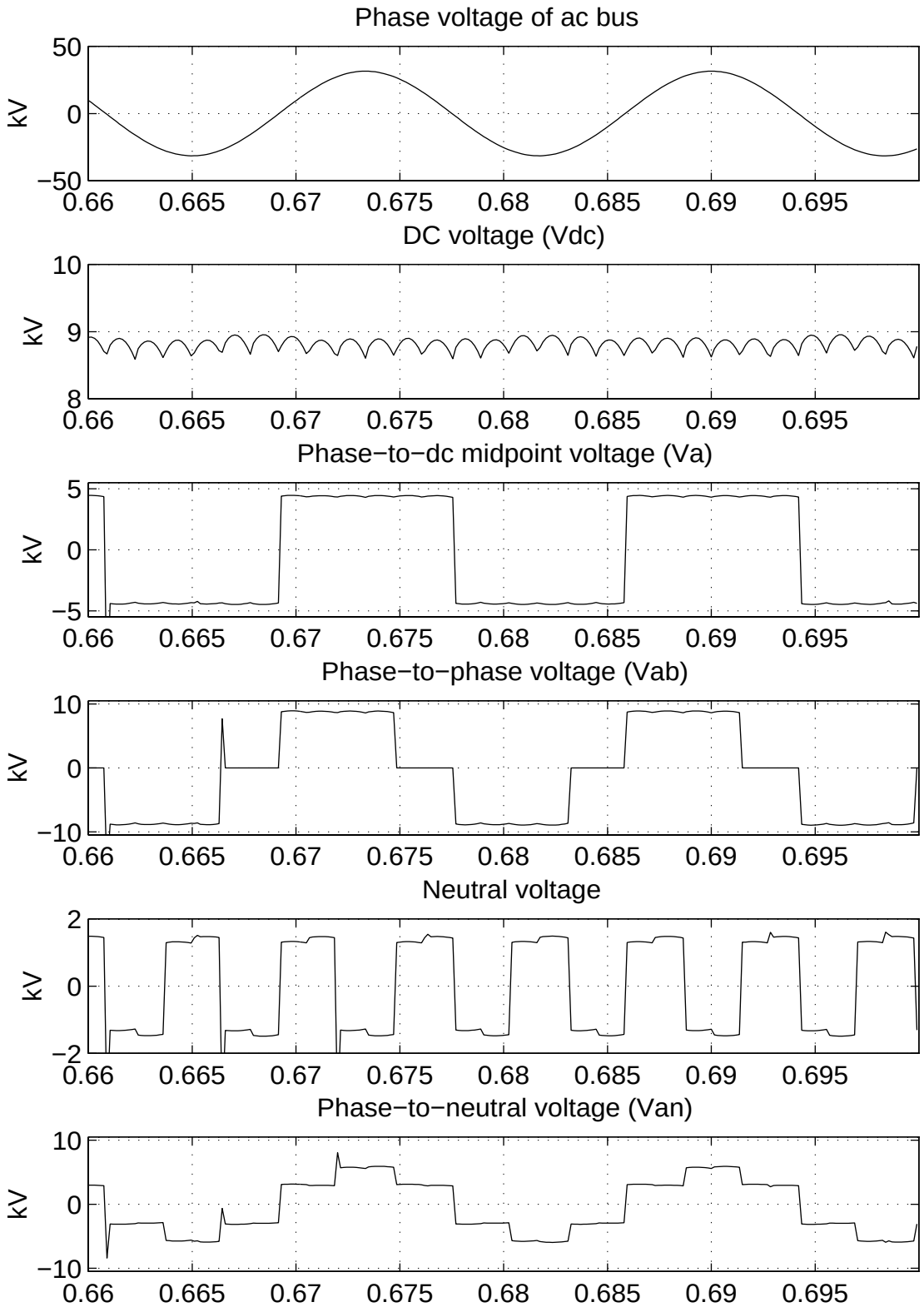


Figure 2.3 – EMTP results for a three-phase two-level VSC; voltage waveforms

It should be mentioned that since the voltage source is basically a reactive device, the ac current is always shifted $\pm 90^0$ (with a small deviation to account for circuit losses) with respect to the ac system voltage. If the converter were connected to a dc battery instead of a dc capacitor the ac current could take any phase angle with respect to the ac system voltage, extending the operation of the converter from two to four quadrant operation.

The dc current is rippled with an average value of zero in steady state operation, as shown in Figure 2.4. If the converter output voltage lags the ac system voltage by some small angle, the current flowing into the capacitor has a positive dc component, thereby raising the dc voltage by charging the dc capacitor. If the capacitor is overcharged and the converter output voltage is too high, the phase of the converter output voltage is advanced by some small angle with respect to the ac system voltage. In this case, the dc current has a negative dc value that reduces the dc voltage by discharging the capacitor.

2.3.3 Harmonic Reduction

One of the important requirements in high voltage power applications is that harmonics be kept at some satisfactory levels. For example, the number of six-pulse two-level bridges in the multi-bridge converter can be increased to cancel certain low frequency harmonics. It is also possible to increase the number of the bridges from two to three, for example, to reduce harmonic content. The advantage of the latter is that the fundamental component of the output voltage can be controlled even though the dc voltage is kept constant and the switching frequency is equal to the fundamental frequency [33]. The third method, the PWM method, based on the fast operation of switches in a six-pulse configuration, shifts low frequency harmonics to higher frequencies; the total harmonic current injection is reduced, but the total harmonic distortion in the ac output voltage is not changed. There are different categories of PWM techniques and a complete overview can be found in [34].

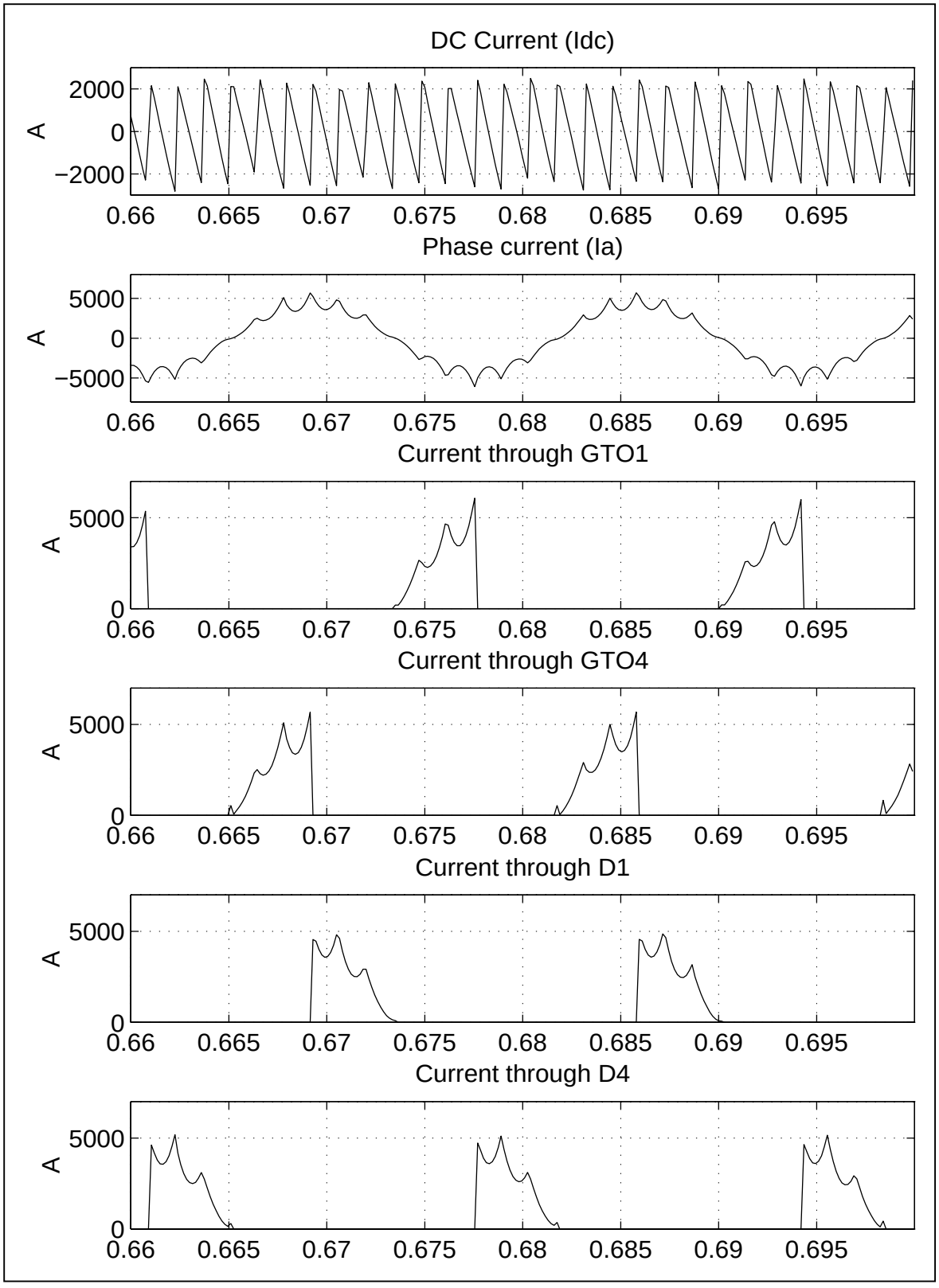


Figure 2.4 – EMTP results for a three-phase two-level VSC; current waveforms

2.3.3.1 Two-Level Multi-Bridge Converter

The waveforms of the voltage-sourced converter output voltage and current shown in Figure 2.3 and Figure 2.4 are far from sinusoidal. The output voltage waveform of the six-pulse converter contains harmonics of frequencies of $(6k \pm 1)f$, and its current is composed of frequencies of $6k \cdot f$, where f is fundamental frequency and $k = 1,2,3,\cdots$. Passive filters can filter some of the harmonics but this method is considered to be expensive, particularly at low frequencies, where L and C passive filter components have large values and sizes.

One way of reducing the level of harmonics present in the converter output waveforms is to increase the number of converters. This method involves multi-connected, out-of-phase six-pulse converters connected to a power system through an appropriate configuration of transformers. A $6n$-pulse converter can be obtained through series connection of n six-pulse converters operated from a common dc source with a successive $2\pi/6n$ phase displacement. The six-pulse converter output voltage waveforms are shifted by transformers with appropriate secondary winding configurations to cancel the phase displacement of the converter. The transformed outputs of all converters are in phase with each other and are summed by the series connection of all corresponding primary windings. It is necessary to have separate transformers for each converter, otherwise phase shifts in the non-characteristic harmonics, i.e. 6n – order harmonics, will result in a large circulating current due to a common core flux [33]. Transformer primary side windings should not be connected in parallel to the same three-phase ac buses for the same reason. Therefore, the harmonics present in the waveform of a general P-pulse converter are $(P \pm 1) \cdot f$ in the output voltage and $P \cdot f$ in the output current where P=6n and $n = 1,2,3,\cdots$. Since the order of the lowest harmonic present in the output current is the same as the pulse number, and the order of the lowest harmonic contained in the output voltage is the pulse number minus one, the harmonic spectrum improves rapidly by increasing the number of converters, and consequently by increasing the pulse

number. In the STATCOM application of [15], eight six-pulse converters are connected through appropriate transformer configuration to form a 48-pulse converter configuration.

To study the benefits of this method, a twelve-pulse converter is used here based on two six-pulse converters connected in series; their output waveforms are summed using two three-phase two-winding transformers. The transformer connection is shown in Figure 2.5, while the voltage and current waveforms for each winding are shown in Figure 2.6. As can be seen from Figure 2.5 and Figure 2.6, the phase-to-phase voltages of the second converter are connected to a delta winding, and hence the phase-to-phase voltage is shifted by 30^0 to be in phase with the phase-to-neutral voltage from the first converter. This arrangement puts the non-characteristic harmonics, i.e., harmonics of order different than $12n \pm 1$, in phase opposition.

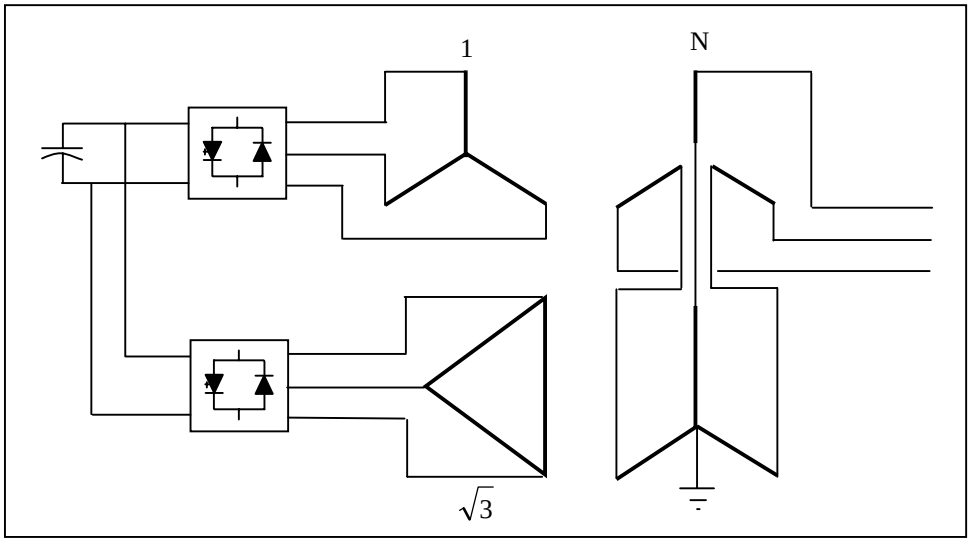


Figure 2.5 – Twelve-pulse VSC [33]

The magnitude of the converter output voltage is controlled by changing the input dc voltage, which is a disadvantage of this kind of arrangement as compared to PWM converters. On the other hand, the amount of harmonics generated by the converter can be controlled and reduced to acceptable levels by increasing the number of converters in the multi-converter arrangement.

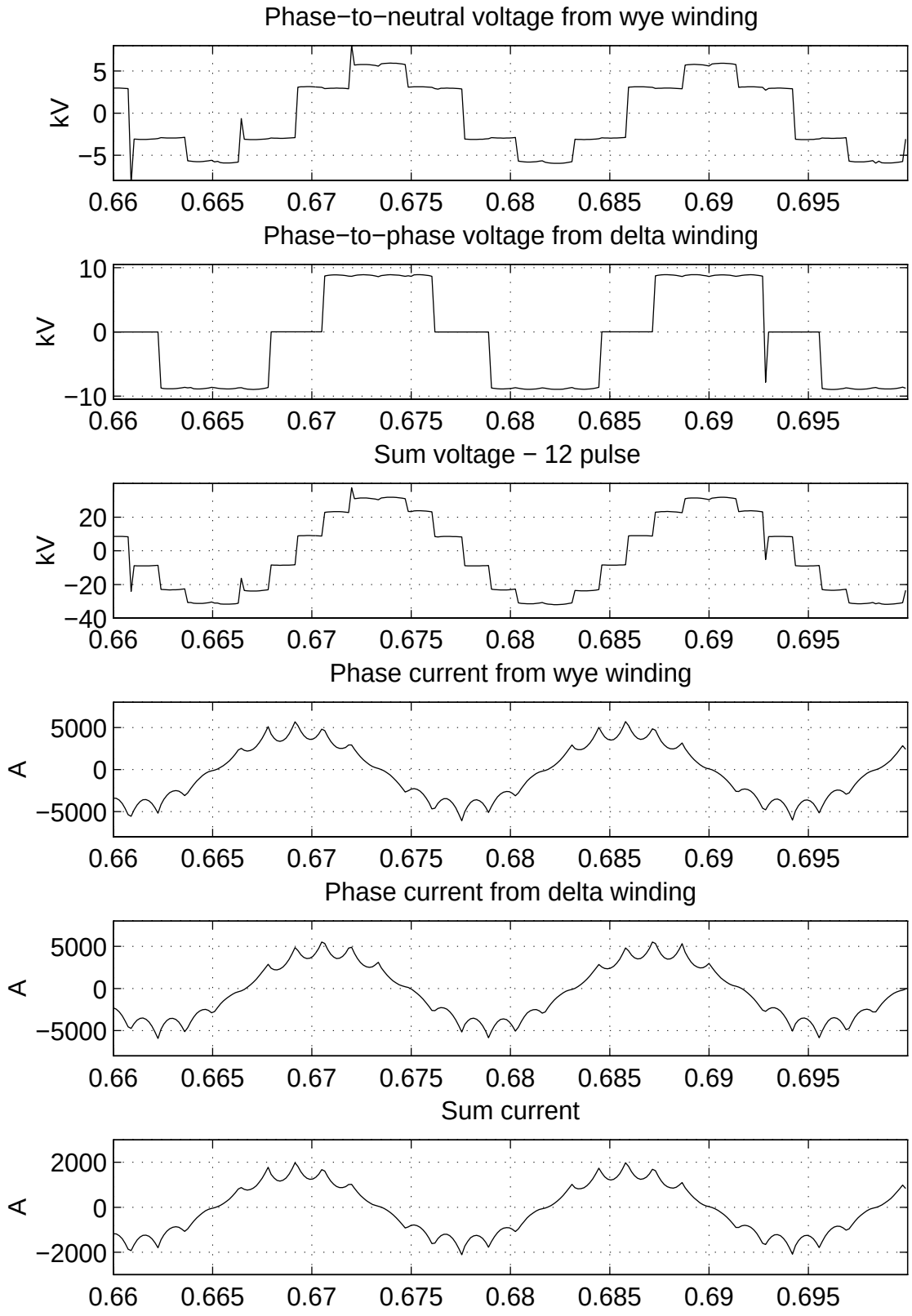


Figure 2.6 – EMTP results for 12-pulse operation of VSC

2.3.3.2 Pulse Width Modulation (PWM) Converter

The main advantage of PWM converters is the possibility of controlling the converter gain and consequently the converter output voltage. There are numerous PWM techniques used with different converter configurations [33, 34, 35]. In the most popular PWM method, the width of each pulse is varied in proportion to the amplitude of a sine wave or so-called control waveform [29, 36] as seen in Figure 2.7. The triangular or carrier waveform, which is shown in Figure 2.7 as a sinusoidal waveform due to the EMTP limitations to produce triangular waveform, has a certain switching frequency f_s, which establishes the frequency at which the converter switches. In the EMTP results shown in Figure 2.7, the frequency was kept at 540 Hz or 9 times the fundamental frequency.

In the two-level three-phase voltage-sourced converter shown in Figure 2.1, the switches are controlled in a way that the turn-on and turn-off pulses correspond to the crossing points of the control waveform with the carrier waveform of corresponding phase. The frequency of the carrier waveform determines the fundamental frequency of the output voltage (50 HZ or 60 HZ). The frequency modulation ratio is the ratio between frequencies of the carrier and control waveforms, i.e.,

$$m_f = \frac{f_{carrier}}{f_{control}} \tag{2.6}$$

By varying the amplitude of the control waveform $A_{control}$ from zero to the amplitude of the carrier waveform $A_{carrier}$, the pulse width can be varied from 0 to 180^0. The modulation ratio m_a defines the ratio between the control and carrier waveforms:

$$m_a = \frac{A_{control}}{A_{carrier}} \tag{2.7}$$

The waveform v_{aN} in Figure 2.7 shows the phase *a* to the dc midpoint voltage, which fluctuates between $-V_{dc}/2$ and $+V_{dc}/2$. The amplitude of the fundamental frequency component of the phase-to-dc midpoint voltage is m_a times $V_{dc}/2$:

$$V_{aN,max} = m_a \frac{V_{dc}}{2} \tag{2.8}$$

The waveform v_{bN} in Figure 2.7 is the output voltage of phase *b* to the dc midpoint, which lags v_{aN} by $120^{0.}$ The phase-to-neutral voltage v_{an} is calculated as the difference between the voltage of the floating neutral *n* of the wye-connected secondary of the step-down transformer, i.e. v_{nN}, and the dc midpoint voltage where:

$$v_n = \frac{v_{aN} + v_{bN} + v_{cN}}{3} \tag{2.9}$$

Since m_f is chosen to be an odd integer (9 for the waveforms shown in Figure 2.7), the phase-to-neutral and the phase-to-phase voltages result in an odd symmetry as well as a half-symmetry. Therefore, Fourier analysis of the converter output voltages shows that only the coefficients of the sine series are finite, while those for the cosine series are zero. This fact indicates that only odd harmonics are present, while the even harmonics disappear from the waveforms of v_{an} and v_{ab}.

The frequency modulation ratio m_f has an influence over the order of harmonics that appear as sidebands centered around the switching frequency and its multiples, i.e. around harmonics m_f, $2m_f$, $3m_f$, etc. The frequencies at which harmonics occur are:

$$\begin{aligned} &m_f, m_f \pm 2, \\ &2m_f, 2m_f \pm 1 \\ &3m_f, 3m_f \pm 2 \\ &4m_f, 4m_f \pm 1, \cdots \end{aligned} \tag{2.10}$$

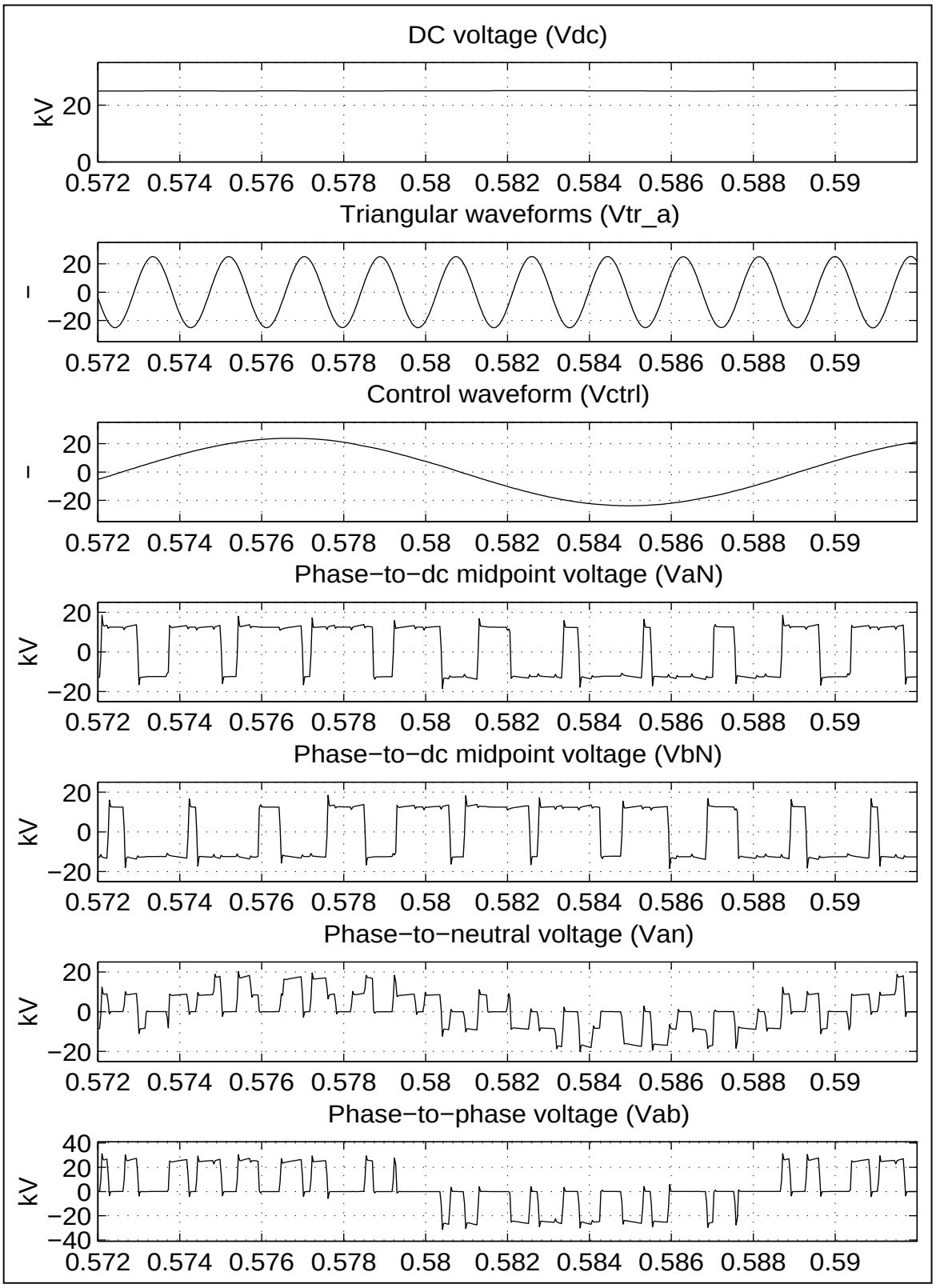


Figure 2.7 – EMTP results for PWM operation of VSC

It is important to mention that in a three-phase VSCs, triplen harmonics are eliminated. Also, if the frequency modulation ratio is chosen to be a multiple of 3, even the harmonics of the order of m_f are cancelled out in the converter output voltage waveforms.

2.4 Summary

This chapter has discussed the fundamentals of forced-commutated VSCs, with emphasis on high power applications. The basic relationships for VSCs are formulated to provide a basis for the discussions and results in the following chapters.

The operation principles of a VSC are explained briefly for two control methods: square-wave and PWM. The analogy and comparison of square-wave and PWM controlled methods is also given. Multi-level voltage-sourced converters are not within the scope of the thesis.

Chapter 3.

SHUNT SYNCHRONOUS STATIC COMPENSATOR
STATCOM

3.1 Introduction

The basic design and operating principles of a STATCOM are explained here together with the STATCOM control circuits. Twelve-pulse and PWM-controlled STATCOMs are implemented in the Electromagnetic Transients Program (EMTP). The three-phase studies shown in this chapter are based on a 230 kV test power system, adopted from [37] and modified to serve the purposes of these studies.

The presented STATCOM models are detailed models that include the GTO and diode valves together with their necessary snubber circuits, which makes these models a valuable tool in a power system design process. The designed control systems for the twelve-pulse and PWM-controlled STATCOM do not use typical d-q transformation to obtain dc signals for control purposes [41, 45, 47]. Instead, the control systems use simple input variable measurements, similar to a SVC control system, which is a different way to treat the STATCOM control circuit design. This approach also simplifies the control circuits. The STATCOM operating and control limits are included into the models, which makes these models suitable for quasi-steady state and transient stability studies.

The presented detailed models are not novel models since they realistically represent the practical device; however, their implementation into the EMTP proved to be a challenging task. The models produced the expected results only when certain snubber circuits were used, due to numerical oscillation problems of the trapezoidal integration method. Moreover, the STATCOM models were included into a realistic test system as opposed to the usual two- bus STATCOM tests systems found in the literature.

3.2 Basic Operating Principles

The STATCOM is given this name because in a steady state operating regime it replicates the operating characteristics of a rotating synchronous compensator. The basic electronic block of a STATCOM is a voltage-sourced converter that converts a dc voltage at its input terminals into a three-phase set of ac voltages at fundamental frequency with controllable magnitude and phase angle. The VSC can be built using one of the three previously described methods. Thus, it can be made up of three-phase two-level six-pulse converters connected by an appropriate magnetic circuit into a multi-pulse structure to meet practical harmonic, current and voltage rating requirements; or three-phase three-level twelve-pulse converters in a multi-pulse structure; or simply PWM controlled three-phase two-level converters. A STATCOM has no inertia and can basically act in a fraction of a second, which is an advantage over a synchronous compensator. Furthermore, STATCOM does not significantly alter the existing system impedance, which gives it an advantage over the SVC. In all STATCOM applications implemented in transmission systems so far, only two of these methods have been used; PWM are still considered uneconomical due to high switching losses of available semiconductor switches with intrinsic turn-off capabilities.

In 1980, Mitsubishi Electric Corporation and Kansai Electric Power developed a first prototype (77 kV, 20 MVA) of Static Var Generator (SVG) using forced-commutated circuits to provide a continuous and controllable var source [38]. In 1986, the first STATCOM, at the time called Advanced Static Var Generator, was built using GTOs, consisting of two six-pulse two-level bridges working in a twelve pulse operation in conjunction with passive filters [12, 39]. The rating of the controller was small, 1 Mvar. Nevertheless, it showed the potential of the controller for power system applications. The GTO switches used in this installation were rated at 2500 V and 2000 A. In 1991, continuous improvements in power electronics technology and the consequent increase in GTO ratings (4500 V and 3000 A), resulted in a 154 kV, 80 Mvar Static Var Generator in Japan [40]. With the support of the Electric Power Research Institute (EPRI) in sponsoring the development of high power GTOs and new converter topologies, a 161

kV, 100 Mvar STATCOM has been installed in 1995 at the Sullivan substation, Tennessee [15, 41]. The GTOs used in this installation are rated for 4500 V and 4000 A.

A STATCOM can be used for voltage regulation in a power system, having as an ultimate goal the increase in transmittable power, and improvements of steady-state transmission characteristics and of the overall stability of the system. Under light load conditions, the controller is used to minimize or completely diminish line overvoltage; on the other hand, it can be also used to maintain certain voltage levels under heavy loading conditions.

In its simplest form, the STATCOM is made up of a coupling transformer, a VSC, and a dc energy storage device. The energy storage device is a relatively small dc capacitor, and hence the STATCOM is capable of only reactive power exchange with the transmission system. If a dc storage battery or other dc voltage source were used to replace the dc capacitor, the controller can exchange real and reactive power with the transmission system, extending its region of operation from two to four quadrants. A functional model of a STATCOM is shown in Figure 3.1.

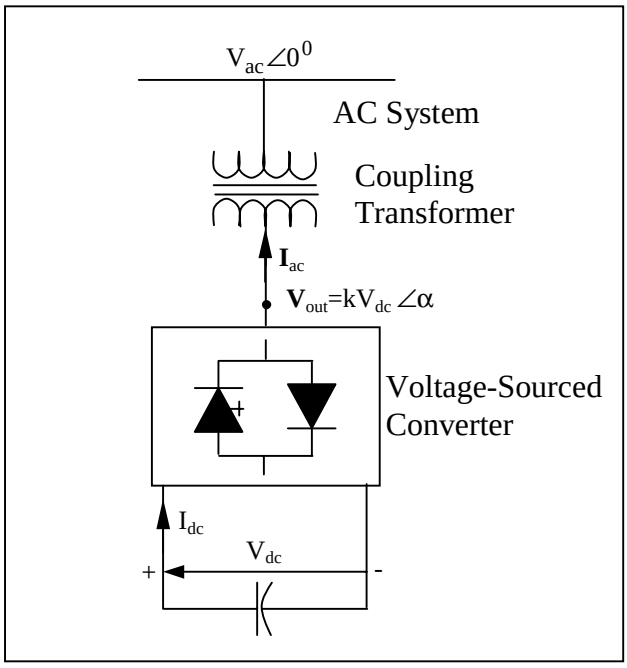


Figure 3.1 – Functional model of a STATCOM

The STATCOM's output voltage magnitude and phase angle can be varied. By changing the phase angle α of the operation of the converter switches relative to the phase of the ac system bus voltage, the voltage across the dc capacitor can be controlled, thus controlling the magnitude of the fundamental component of the converter ac output voltage, as $V_{out} = kV_{dc}$. Note that the coefficient k in this equation depends on the converter configuration, number of switching pulses and the converter controls. The difference between the converter output voltage and the ac system bus voltage basically determines the flow of reactive power through the coupling transformer to or from the system.

The real power flowing into the converter supplies the converter losses due to switching and charges the dc capacitor to a satisfactory dc voltage level. The capacitor is charged and discharged during the course of each switching cycle, but in steady state, the average capacitor voltage remains constant. If that were not the case, there would be real power flowing into or out of the converter, and the capacitor would gain or lose charge each cycle. In steady state, all of the power from the ac system is used to replenish the losses due to switching. The STATCOM's ability to absorb/supply real power depends on the size of dc capacitor and the real power losses due to switching. Since the dc capacitor and the losses are relatively small, the amount of real power transfer is also relatively small. This implies that the STATCOM's output ac current $\mathbf{I}_{ac}$ has to be approximately $\pm 90^0$ with respect to ac system voltage at its line terminals.

Figure 3.2 (a) shows the STATCOM ac current and voltage diagram where phasors $\mathbf{I}_Q$ and $\mathbf{I}_P$ represent the ac current $\mathbf{I}_{ac}$ components that are in quadrature and in phase with the ac system voltage $\mathbf{V}_{ac}$, respectively. The dc current I_{dc} and voltage V_{dc} are shown in Figure 3.2 (b). If the losses in the STATCOM circuit are neglected and it is assumed that real power exchange with the ac system is zero, then the active current component $\mathbf{I}_P$ and dc current I_{dc} are equal to zero; the ac current $\mathbf{I}_{ac}$ is equal to the reactive component $\mathbf{I}_Q$ in this case. In Figure 3.2 (a) for the real and reactive power flows positive means that power is going into the STATCOM while negative means that the power is going out of the STATCOM.

Varying the amplitude of the converter three-phase output voltage $\mathbf{V}_{out}$ controls the reactive power generation/absorption of the STATCOM. If the amplitude of the converter output voltage $\mathbf{V}_{out}$ is increased above the amplitude of the ac system bus voltage $\mathbf{V}_{ac}$, then the ac current $\mathbf{I}_{ac}$ flows through the transformer reactance from the converter to the ac system generating reactive power. In this case, the ac system draws capacitive current that leads by an angle of 90^0 the ac system voltage, assuming that the converter losses are equal to zero. The ac current flows from the ac system to the voltage-sourced converter if the amplitude of the converter output voltage is decreased below that of the ac system, and consequently the converter absorbs reactive power. For an inductive operation, the current lags the ac voltage by an angle of 90^0, assuming again that the converter losses are neglected. If the amplitudes of the ac system and converter output voltages are equal, there will be no ac current flow in/out of the converter and hence there will be no reactive power generation/absorption.

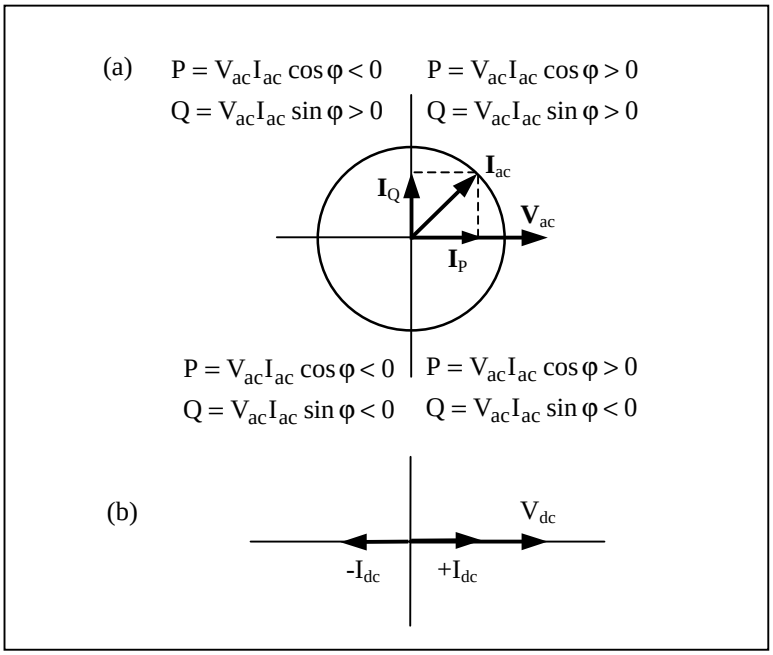


Figure 3.2 - STATCOM phasor diagrams (a) at ac terminals and (b) at dc terminals [11]

The ac current magnitude can be calculated using the following equation:

$$I_{ac} = \frac{V_{out} - V_{ac}}{X} \tag{3.1}$$

assuming that the ac current flows from the converter to the ac system. V_{out} and V_{ac} are the magnitudes of the converter output voltage and ac system voltage respectively, while X represents the coupling transformer leakage reactance. The corresponding reactive power exchanged can be expressed as follows:

$$Q = \frac{V_{out}^2 - V_{out} V_{ac} \cos\alpha}{X} \tag{3.2}$$

where the angle α is the angle between the ac system bus voltage $\mathbf{V}_{ac}$ and the converter output voltage $\mathbf{V}_{out}$.

Figure 3.3 (a) shows the case when the angle α is equal to zero and there is no real power transfer between the converter and ac system. Thus, the real power exchange between the converter and the ac system can be controlled by phase shifting the converter output voltage $\mathbf{V}_{out}$ with respect to the ac system bus voltage $\mathbf{V}_{ac}$. The converter supplies real power from its dc capacitor to the ac system if the converter output voltage leads the corresponding ac system voltage as is shown in Figure 3.3 (b), whereas the converter absorbs real power from the ac system if the converter output voltage is made to lag the ac system voltage, see Figure 3.3 (c). The amount of exchanged real power is typically small in steady state; hence, the angle α is also small (couple of degrees in steady state). The real power exchange between the voltage-sourced converter and the ac system can be calculated using:

$$P = \frac{V_{ac} V_{out} \sin\alpha}{X} \tag{3.3}$$

The real and reactive power generated or absorbed by the voltage-sourced converter can be controlled independently of each other, provided that the voltage-sourced converter is connected to a dc storage battery, dc voltage source or another voltage-sourced converter instead of a dc capacitor. The real power that is being exchanged by the transmission system must be supplied or absorbed at its dc terminals by the dc energy storage or any other previously mentioned device. In contrast, the reactive power exchange is internally generated or absorbed by the voltage-sourced converter, without the dc energy storage device playing any part in it. The converter simply interconnects the three-ac terminals in such a way so that the "reactive" current can flow freely between them [42]. In theory, an infinitely small capacitor could be used on the dc side if the connected ac system is symmetrical. However, since the ac systems are exposed to different unbalanced disturbances and the converter's valves cannot switch fast, together with a limited response speed of the control system, a sufficiently large capacitor should be used in practice to diminish variation on the dc side voltage.

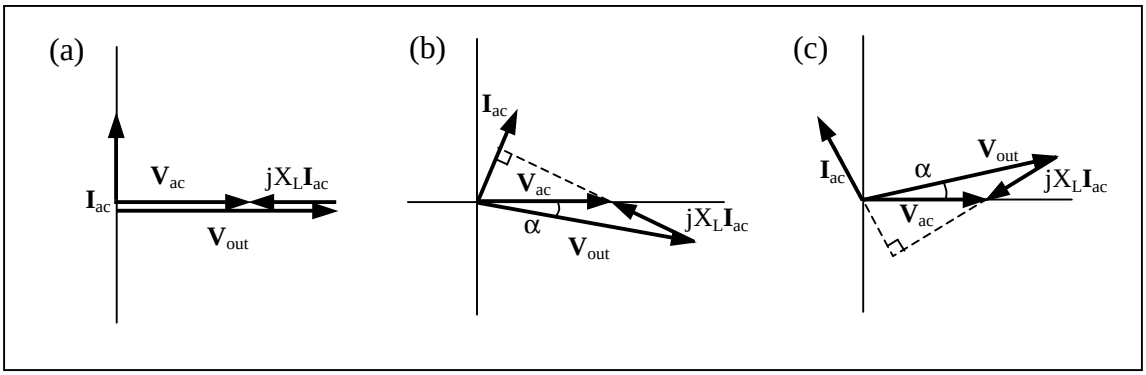


Figure 3.3 – STATCOM phasor diagrams for (a) steady-state operation, (b) charging of dc capacitor, and (c) discharging of dc capacitor

The energy going into the converter at its ac terminals has to be equal to the energy lost due to switching plus the energy stored in dc capacitor and vice versa, i.e.,

$$P_{ac} = P_{losses} + P_{dc} \tag{3.4}$$

Closer inspection of the dc current shows that the converter draws a rippled current from the dc capacitor. The reason for this is that the converter output voltage waveform is not perfectly sinusoidal; the amount of ripple (harmonics) depends on the method used to obtain the output waveforms (multi-converter configuration of two or three-levels or PWM methods). Since the voltage waveform is not perfectly sinusoidal, the instantaneous power going in/out of converter will follow these changes (ripples), resulting in a rippled dc current. While the average value of the dc current is zero in steady state, during transients this current follows the changes in the output waveforms to maintain the desired mean dc voltage.

3.3 STATCOM Control Systems

An advantage of the PWM based control technique is the possibility of independent active and reactive component control of the converter output current, but due to low switching frequency of the currently available semiconductor switches, this technique has not yet been used in high voltage applications. Furthermore, the phase control technique does not need filters to "clean" up the converter output waveforms, as it allows the connection of a number of converters to switch together in a high pulse mode. The STATCOM built for the Tennessee Valley Authority in 1995 generates a 48-pulse output voltage waveform by electro-magnetically combining 8 square wave outputs per phase [41].

The control scheme proposed in [44] controls reactive current of the VSC by controlling the phase shift (α) of the converter output voltage, which in turn controls the real power flow between the ac and dc sides and thus the dc voltage. The dc component of the converter current is obtained by performing α–β and d-q transformations on the measured instantaneous three phase currents. This transformation is important since it allows easy and independent control of the active and reactive components of the current. This transformation is explained in more detail in Appendix A.

Reference [45] provides details of the mathematical derivation of control equations and the control algorithms used in two possible cases, depending on the dc voltage control. The dc voltage is kept constant (PWM control) in the first algorithm, while the second allows the dc voltage to vary in response to changes in ac system bus voltage (phase control). In this case, d-q decomposition of the converter ac current was used to control the converter response to an unbalanced fault.

The authors in [46] present an approach for the dynamic control of voltage-sourced converter based FACTS controllers, which uses a linear multi-variable approach based on state space theory. Modeling and control of the system were carried out in a synchronous dq-frame. In [47], the authors use the work presented in [44] to discuss the use of a PWM based control system to control over-currents caused by an unbalanced single-phase fault placed at the ac bus where the STATCOM is connected. The same objective, the STATCOM control is discussed in [48]. In both papers, the STATCOM operates during the ac faults, showing that blocking the VSC during temporary ac faults is inadequate.

In this thesis, the STATCOM control system is treated similarly to the control system designed for a SVC, as presented in [37]. A phase control technique is implemented knowing that the error caused by a difference in measured ac system bus voltage magnitude and a set value is directly proportional to the phase angle difference α between the ac system bus voltage and the STATCOM output voltage. A PWM based control technique is also investigated since that real power flow in and out of the STATCOM can be controlled by controlling the dc bus voltage, while the reactive power generation/absorption is directly proportional to the magnitude of the STATCOM output voltage. New and more advanced control strategies, such as H_∞ or adaptive nonlinear controls have been proposed for STATCOM control [44, 49]; however, these are beyond the scope of this thesis leaving them for future research.

3.3.1 Test System Description

In order to study in detail the STATCOM under phase and PWM controls, a test system, introduced in [50] and modified to serve the purpose of this thesis, has been implemented in the EMTP. The 10-bus test system operates at 230 kV and is shown in Figure 3.4. The system consists of a 245.5 MW, 13.8 kV generator with Automatic Voltage Regulator (AVR) and a Δ - Y step-up transformer; an infinite bus with its corresponding Thevenin impedance is modeled as an ideal voltage source and a coupled Z-matrix, respectively, to represent a system equivalent. The test system is made of several transmission lines of various lengths, where long lines are modeled with distributed parameters, while short length lines are modeled as 3-phase Π equivalents. There are two loads modeled as impedance loads, while the corresponding step-down transformers are simply modeled using their leakage reactances.

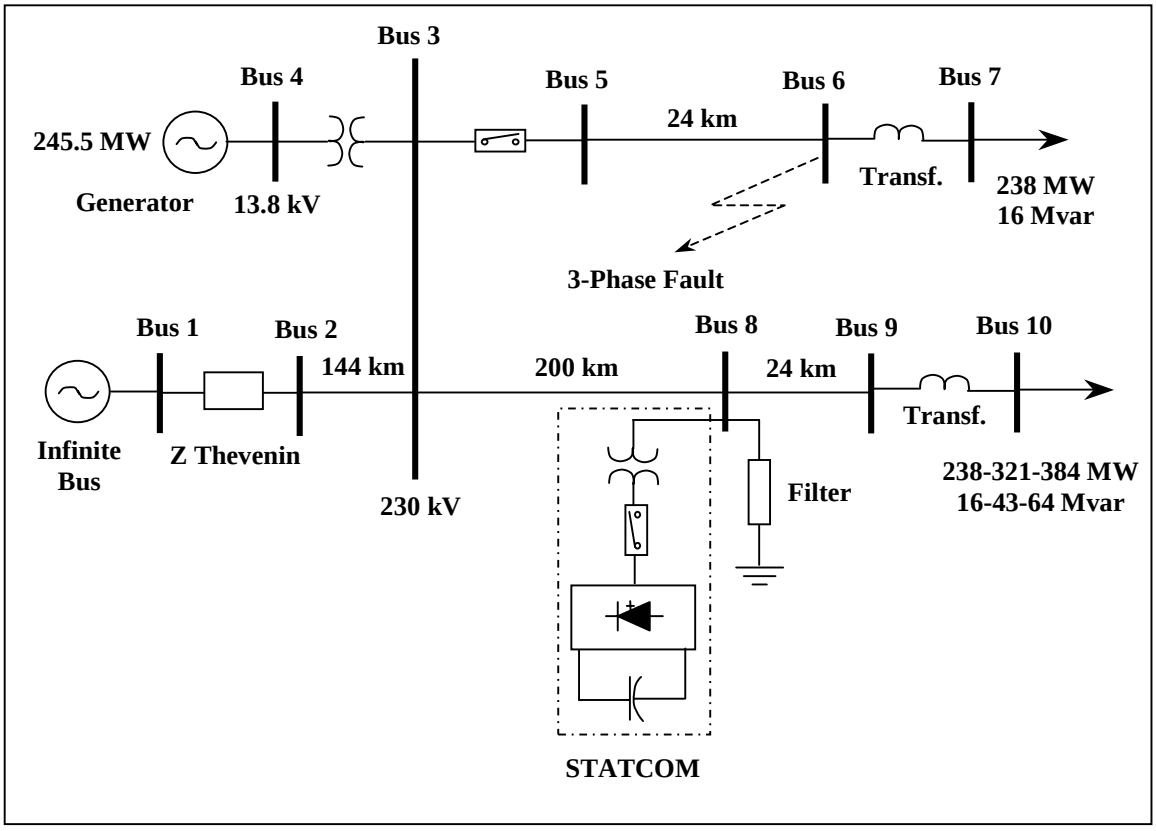


Figure 3.4 – 10-Bus test system

3.3.2 Phase Control Technique

A STATCOM, used to regulate the voltage level at Bus 8 in the test system, is modeled as a three-phase, twelve-pulse voltage-sourced converter that is connected to the ac system through an appropriate transformer. The basic building block of the 150 Mvar, 230 kV STATCOM circuit is the six-pulse converter shown in Figure 2.1 and explained in detail in Section 2.3.1. It is important to emphasize that the STATCOM model, includes all GTO valves and diodes, with the required snubber circuits to reduce dv/dt and di/dt due to valve switching. The STATCOM control circuit is also modeled in great detail.

The control of the STATCOM is achieved by variations in the switching angle of the controlled semiconductor switches, so that the fundamental component of the STATCOM output voltage lags or leads the ac system bus voltage by a few degrees. This causes real power to transiently flow in or out of the converter, thus changing the dc capacitor voltage and consequently the magnitude of the STATCOM output voltage. The modeled twelve-pulse STATCOM circuit is shown in Figure 3.5. The circuit consists of two six-pulse converters connected in series on the ac side of the circuit with a 150 Mvar, 230 kV / 6 kV summing and intermediate transformer.

The dc sides of the two converters are connected in parallel and share the same dc capacitor. They can also be connected in series on the dc side in twelve-pulse operation, with twice the dc voltage and, consequently, twice the converter output ac voltage. However, this kind of connection is avoided due to the fact that the two dc buses (capacitors) must have equal voltages. From the ac side, the converters are connected in series through the series connection of the line-side windings of the intermediate transformer to provide appropriate cancellation of the characteristic harmonics. It is possible to connect the converters in parallel on the ac side, but that would require transformers with special windings and would increase the total cost of the STATCOM.

A passive filter is connected to Bus 8 to prevent the 11^{th}, 13^{th} and 23^{rd} and higher harmonics from penetrating into the ac system. At fundamental frequency, the filter is capacitive with 65 Mvar of reactive power.

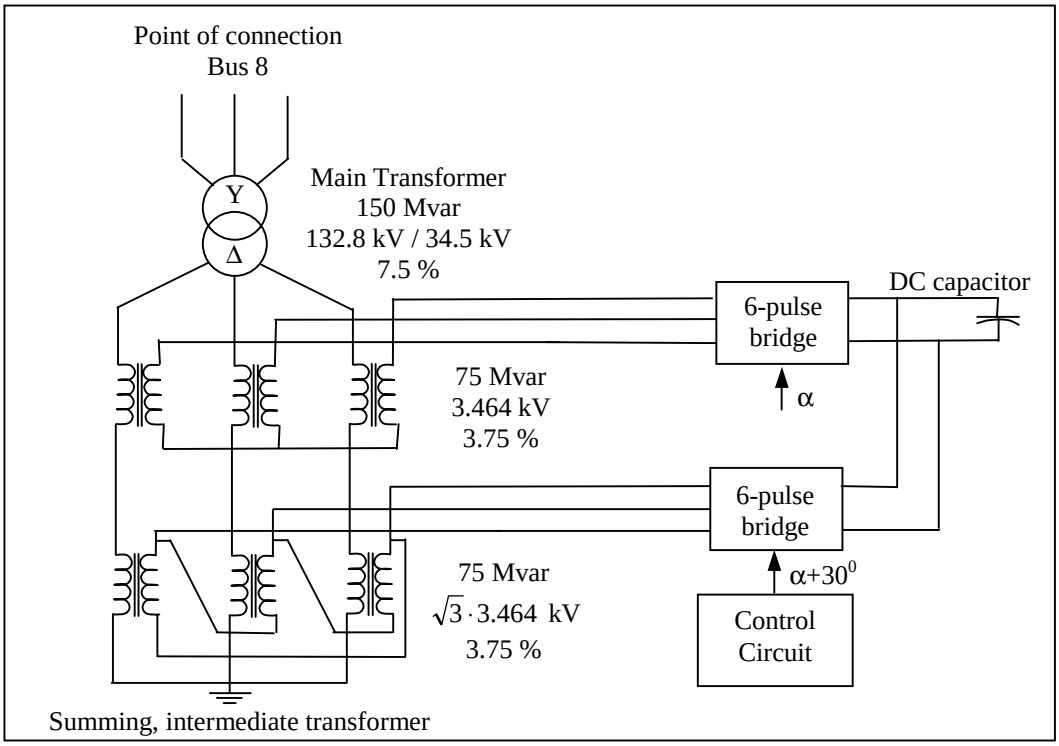


Figure 3.5 –Twelve-pulse series connected STATCOM circuit

Figure 3.6 shows the control block modeled in the EMTP and used for voltage regulation in a power system. The actual voltages from "NETWORK", i.e., voltages at the Bus 8, are measured and their signals are transferred to EMTP-TACS using type-90 voltage sources. TACS is an acronym for Transient Analysis of Control Systems and is used to digitally simulate analog control functions while "NETWORK" depicts the ac system part of the test system modeled in the EMTP which is then used as inputs to a voltage synchronization block to generate a set of balanced phase voltages. The generated set of voltages is then used as an input to the gate pulse generator responsible for proper turn-on and turn-off of the GTO valves. The signal from the type-90 sources is also used as an input to the p.u. voltage regulator after being properly scaled to per unit

values. The output of the p.u. voltage regulator, i.e., the firing angle α in seconds is measured after the reference voltage $v_8(t)$ zero crossings and is used as one of the inputs to the gate pulse generator.

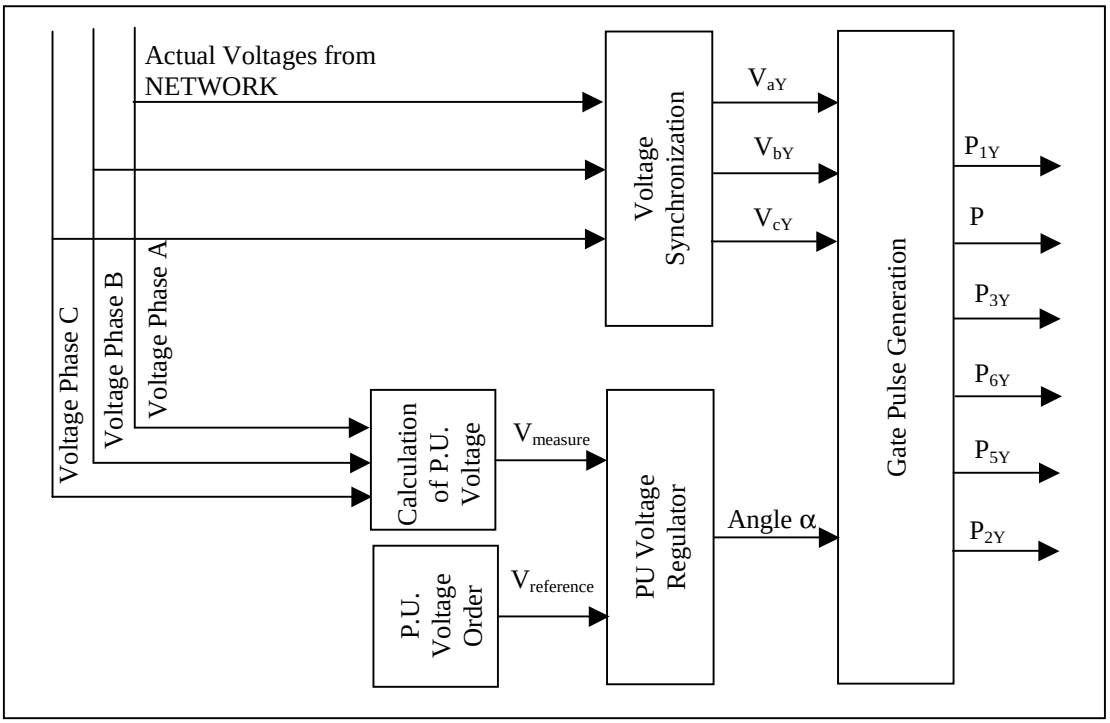


Figure 3.6 –TACS block for voltage regulation [50]

The p.u. voltage regulator for the twelve-pulse STATCOM is shown in more detail in Figure 3.7. It has the following functions:

- Measure the actual voltage at Bus 8 using type-90 voltage sources. The signal, representing the instantaneous voltage at a given time, is then sent to a RMS calculator device (TACS code number is 66). The RMS value is multiplied by $\sqrt{3}$ and then divided by the base voltage of 230 kV to obtain the p.u. value, which is the signal V8puA.
- If the signal V8puA is greater than the ordered voltage signal V8signal, then the error signal V8err is positive. The integrator output V8I increases, which, in turn,

increases the firing angle α and the voltage on the dc capacitor. As a final outcome, the ac voltage at the bus where the STATCOM is connected increases.

- The regulator path V8G gives a gain proportional to the error signal, while the regulator path V8H gives a gain related to the rate of voltage error change. This improves the response of the regulator, so that it can change voltage rapidly if there is a sudden disturbance or load change.

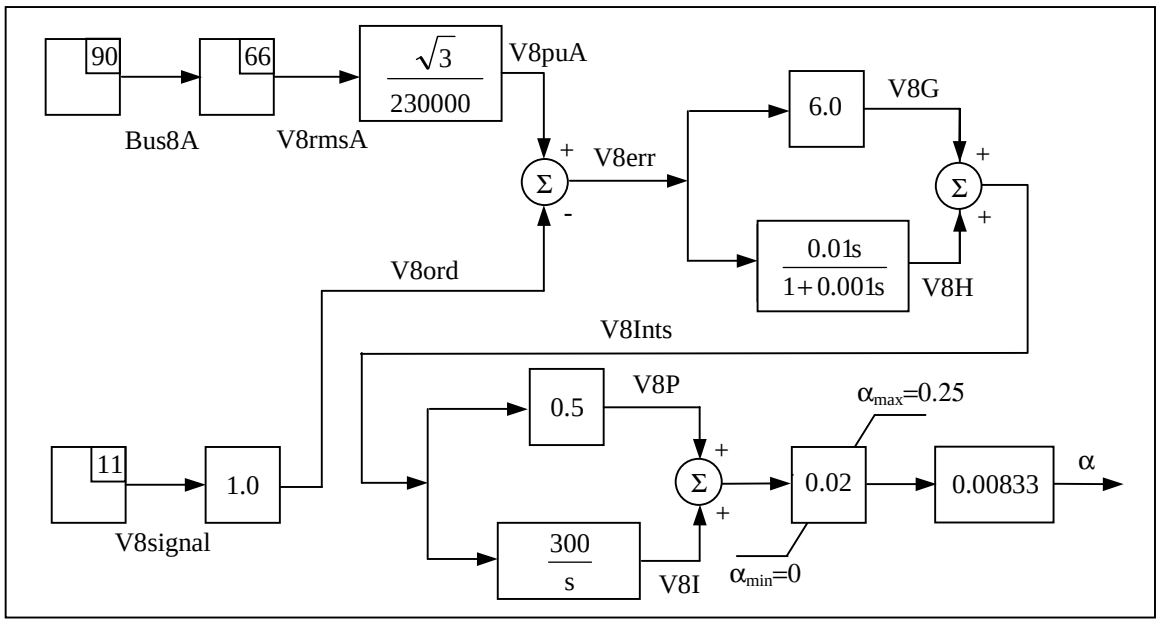


Figure 3.7 –EMTP - TACS block for p.u. voltage regulation

- The integrator output V8I is designed so that 1 p.u. corresponds to 180^0 of firing angle α. The initial value is set to 0. To avoid extreme swings of α under transient conditions, the integrator output is limited between 0 ($\alpha_{min}=0^0$) and 0.1 ($\alpha_{max}=18^0$). This also limits the maximum dc voltage and STATCOM output current. The firing delay angle α is multiplied by 0.00833 to convert the angle from radians to seconds.

The gate pulse generator uses the value of the firing angle α given in seconds to generate a GTO valve firing pulse exactly (90^0 + α) degrees after the natural zero

crossing of the particular ac voltage. The gate pulse generator concept is adopted from [50] and shown in Figure 3.8. The actual three-phase voltage at Bus 8 is tracked for its zero crossings, and the voltage synchronizing voltage block is used to generate a set of balanced phase to neutral voltages V_{aY}, V_{bY}, and V_{cY}.

The scheme shown in Figure 3.8 generates the pulses for the six-pulse converter connected to the Y transformer converter winding. For the six-pulse converter connected to the Δ transformer converter winding, the pulses P1Δ, P4Δ, etc. are shifted by 1.39 ms, i.e., 30^0, from the corresponding pulses of the Y transformer secondary winding. This technique used to produce the firing pulses is known as Equidistant Firing Pulse Control and is used in balanced power systems.

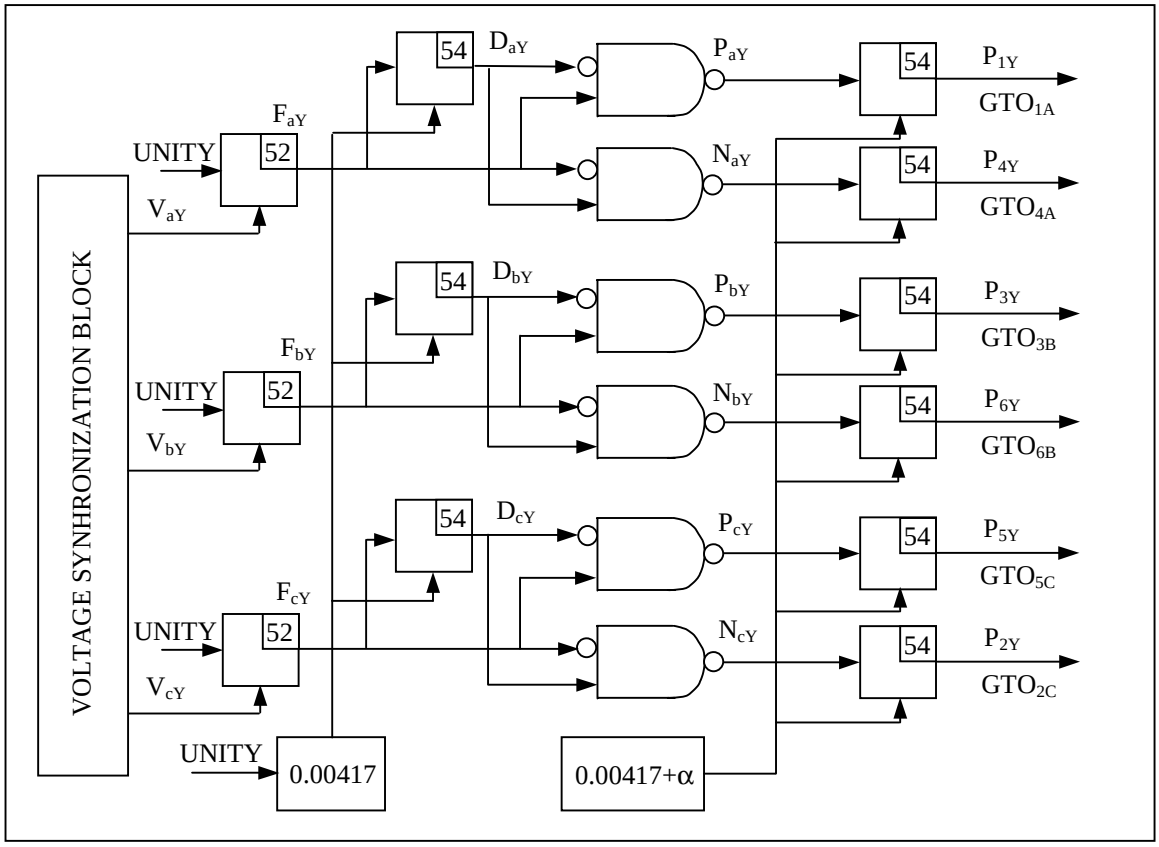


Figure 3.8 –TACS block for gate pulse generator

A voltage synchronizing block, similar to the one explained in [50], is designed to track the actual phase voltages at Bus 8 and to generate a set of balanced voltages that truly follow the phase voltages at Bus 8, in its voltage magnitude and phase angle. This set follows the reference voltage zero crossings and is used as the input to the gate pulse generator.

Thus, the ac voltage in phase *a*, in general and including harmonics, can be represented as:

$$v_a(t) = \sum_{h=1}^{\infty} V_{am_h} \cos(h\omega t + \Theta_a) \tag{3.5}$$

The fundamental component is given by:

$$v_{a1}(t) = C_a \cos \omega t + S_a \sin \omega t \tag{3.6}$$

where the coefficients C_a and S_a represent the Fourier coefficients. On the other hand, the positive sequence components of the tracked phase voltages, in the time domain, can be expressed as:

$$\begin{aligned} v_{a1}(t) = \frac{1}{3}[&(V_{am}\cos(\omega t + \Theta_a) + V_{bm}\cos(\omega t + \Theta_b + 120^0) \\ &+ V_{cm}\cos(\omega t + \Theta_c - 120^0)] \end{aligned} \tag{3.7}$$

which results in:

$$\begin{aligned} v_{a1}(t) = {} & V_{am} \cos \omega t \cdot \cos \Theta_a + V_{bm} \cos(\omega t + 120^0) \cdot \cos \Theta_b + V_{cm} \cos(\omega t - 120^0) \cdot \cos \Theta_c \\ & - V_{am} \sin \omega t \cdot \sin \Theta_a - V_{bm} \sin(\omega t + 120^0) \cdot \sin \Theta_b - V_{cm} \sin(\omega t - 120^0) \cdot \sin \Theta_c \end{aligned}$$

$$\begin{aligned} = {} & C_a \cos \omega t + C_b \cos(\omega t + 120^0) + C_c \cos(\omega t - 120^0) \\ & - S_a \sin \omega t - S_b \sin(\omega t + 120^0) - S_c \sin(\omega t - 120^0) \end{aligned} \tag{3.8}$$

Similarly, equations for $v_{b1}(t)$ and $v_{c1}(t)$ can be derived and included in the voltage-synchronizing block.

3.3.3 PWM Control Technique

The conventional method for harmonic reduction in schemes employing GTO-based STATCOMs is the combination of two- or three-level VSCs through phase-shifting transformers. This cancels characteristic harmonic orders produced by the 6-pulse operation of the converter. In applications involving the transmission system, however, phase-shifting transformers can increase dramatically the complexity and size of the STATCOM. The PWM control of voltage-sourced converter is based on multiple pulses with adjustable width to vary the ac output voltage. Increased number of pulses reduces the presence of the low order harmonics but increases the switching losses. Also, the impact of increased higher harmonics, audible noise, etc., has to be justified by appropriate gains in other areas, such as the elimination of the need for a specialized transformer as required in two or higher level converter applications.

A 150 Mvar, 230 kV STATCOM is modeled as a three-phase, PWM-controlled VSC connected at Bus 8 in the test system shown in Figure 3.4. The basic building block is made up of a three-phase ideal Y - Δ transformer and a two-level PWM-controlled converter. The controlled semiconductor switches are switched at a frequency of 900 Hz (15 times the fundamental frequency), according to the control law explained in section 2.3.3.2. They are modeled as ideal switches having a small resistance connected between two switches to model on-state voltage drop and, at the same time, fulfill the EMTP requirement that two nodes, as well as two switches, need to be separated by a passive element. RC parallel snubber circuits are connected across the switches to reduce dv/dt spikes due to switching, while an inductance is connected between the switches to smooth the converter output current. The modeled PWM-controlled basic STATCOM circuit is shown in Figure 3.9.

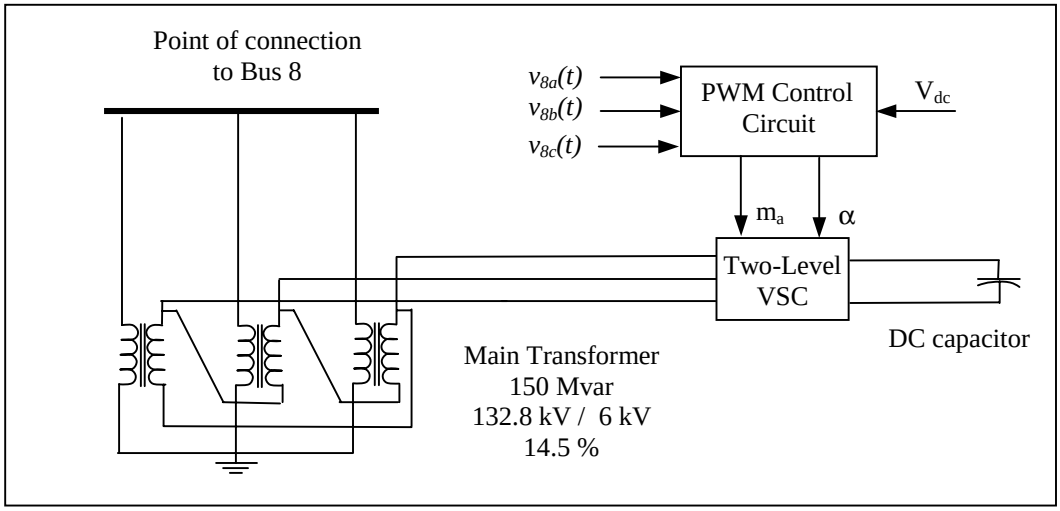


Figure 3.9 –PWM controlled STATCOM circuit

The control of the STATCOM is achieved using the Sinusoidal Pulse Width Modulation method, where a sinusoidal control waveform of fundamental frequency is compared with a triangular waveform of a desired switching frequency. Thus,

$$v_{cta} = m_a V_{dc} \cos(\omega t + \Theta - \alpha) \tag{3.9}$$

$$v_{ctb} = m_a V_{dc} \cos(\omega t + \Theta + 120^0 - \alpha) \tag{3.10}$$

$$v_{ctc} = m_a V_{dc} \cos(\omega t + \Theta - 120^0 - \alpha) \tag{3.11}$$

$$v_{tr} = V_{dc} \cos(15\omega t + \Theta - \alpha) \tag{3.12}$$

where v_{cta}, v_{ctb}, v_{ctc} denote the control waveforms, while v_{tr} is the carrier waveform which defines number of pulses per cycle. The control waveforms are synchronized to the reference voltage, i.e. the Bus 8 phase voltage, and have the amplitude of $m_a V_{dc}$. The variable m_a is the modulation ratio and represents the output of the ac system voltage control loop while V_{dc} is the filtered dc voltage. The triangular waveform v_{tr} is also synchronized to the Bus 8 phase voltage, with amplitude V_{dc} and angular frequency 15 times the fundamental. The angle α is the output of the dc voltage control loop.

A hierarchically structured control system, shown in Figure 3.10, that utilizes the capabilities of the PWM-controlled STATCOM, regulates the voltage of the transmission system. The STATCOM controller consists of three major loops that provide synchronization with the ac system voltage, maintain the dc capacitor voltage at constant level and regulate the ac system voltage. The instantaneous voltages at Bus 8 are measured and their signals are used as inputs to the Voltage Synchronization block, which is used to calculate using Fourier analysis the ideal harmonic free voltage waveforms and the angle θ.

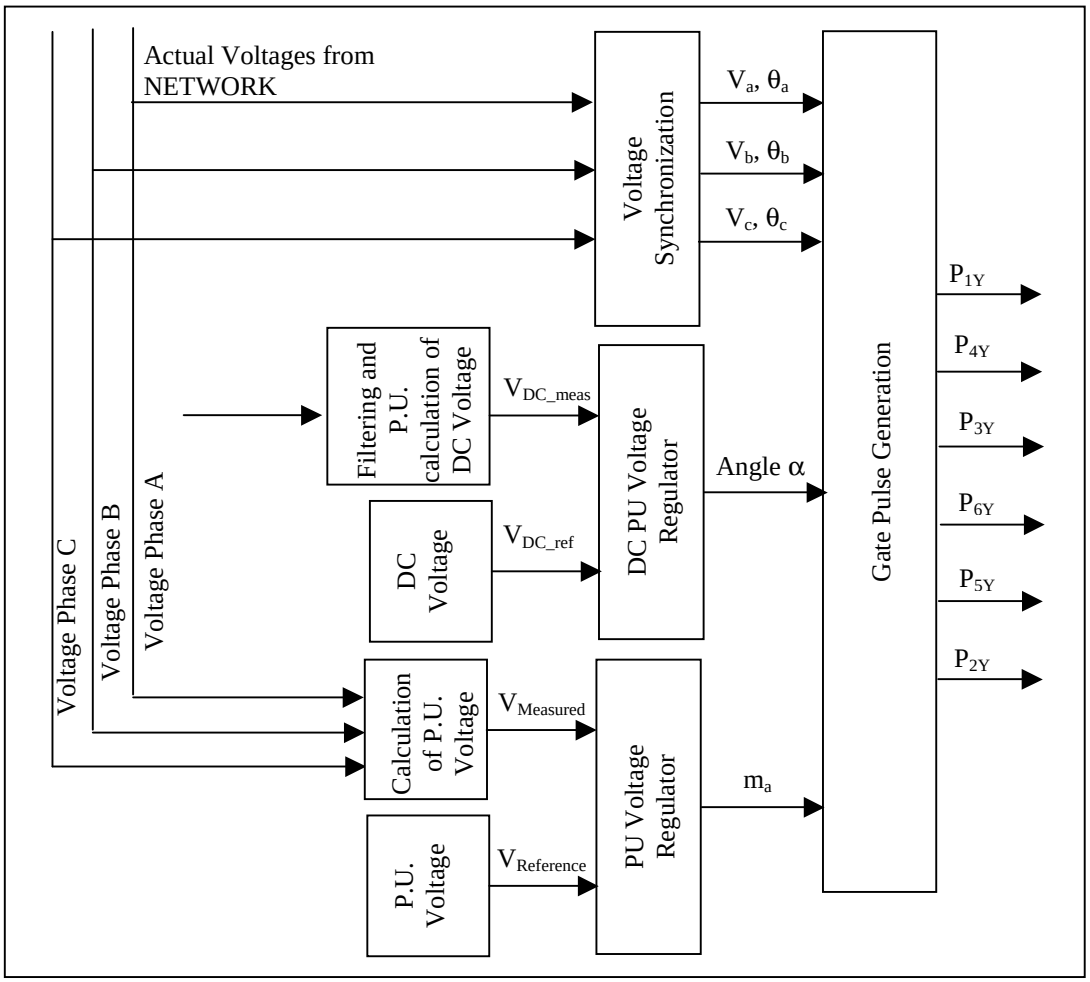


Figure 3.10 – TACS block for voltage regulation of the PWM-controlled STATCOM

The design procedure for dc and ac system voltage loops is based on the respective time response requirements. The transient response of the PWM-controlled STATCOM is determined by the ac system voltage control loop, which has to be fast enough to force the ac system voltage to track the voltage reference waveform closely. On the other hand, the time response of the dc capacitor voltage control loop does not need to be fast, so it is selected to be at most one third of the speed of the ac system voltage loop response, in order not to interfere with the operation of the latter. Thus, these loops can be designed as two independent systems of similar control block structure as the one shown in Figure 3.11.

The objective of the dc voltage control loop is to maintain the dc capacitor charged at a set reference voltage. The error of the DC voltage regulation loop is used to change the phase difference between the fundamental components of the ac system voltage and the STATCOM output voltage. Consequently, the converter exchanges incremental amounts of real power with the ac system charge or discharge the dc capacitor to maintain the required value.

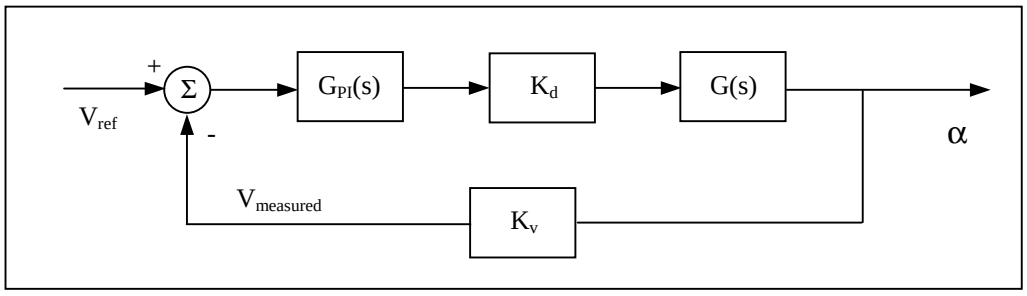


Figure 3.11 – The general block diagram of the voltage control systems

The detail block diagram of the closed loop dc voltage control system is shown in Figure 3.12. At low frequencies, the dc voltage loop has characteristics of a first order system and its transfer function can be approximated by:

$$G(s) = \frac{\Delta V}{\Delta \alpha} = \frac{A_0}{\frac{s}{\omega_b} + 1} \tag{3.13}$$

where $\Delta\alpha$ is the variation of the phase-shift angle between the converter output voltage and the corresponding ac system voltage, A_0 is the compensator open loop gain and ω_b is the open loop break frequency [57]. Applying a standard design approach, a PI controller is used, with the following functions:

(1) The integral term I, with a transfer function k_i/s is required for steady-state accuracy, since the loop has a finite dc gain resulting from the losses.

(2) The proportional term P, of gain k_p, allows for a required bandwidth to be achieved.

The transfer function of the PI controller is given by:

$$G_{PI}(s) = k_p + \frac{k_i}{s} = \frac{s/\omega_{PI} + 1}{s/k_i} \tag{3.14}$$

where $\omega_{PI} = k_i/k_p$. The break frequency ω_{PI} is made equal to the open loop break frequency ω_b. The closed loop transfer function of the dc voltage control system is:

$$H(s) = \frac{K_d G_{PI}(s) G(s)}{1 + K_v K_d G_{PI}(s) G(s)} \tag{3.15}$$

where K_d is the gain of the volts to angle conversion and K_v is the gain of the voltage feedback transducer. The closed loop break frequency ω_{bc} is equal to:

$$\omega_{bc} = K_v K_d k_i A_0 \tag{3.16}$$

From the equation (3.16):

$$k_i = \frac{\omega_{bc}}{K_v K_d A_0} \tag{3.17}$$

$$k_p = \frac{k_i}{\omega_{PI}} \tag{3.18}$$

Some additional blocks are added into the dc voltage controller after analyzing some EMTP simulations, such as the blocks with V_{DCG} and V_{DCH} outputs, shown in Figure 3.12. The regulator path V_{DCG} gives a gain proportional to the error signal, while the regulator path V_{DCH} gives a gain related to the rate of dc voltage error change; this improves the response of the regulator. Also, the PI gains are adjusted with respect to the theoretically derived ones after some EMTP simulations.

Under steady-state operating conditions, the dc voltage control loop keeps the dc voltage constant. However, transient changes in the ac system voltage command signal, which result in changes in the converter output current amplitude, generate voltage fluctuations across the dc capacitor. Their amplitude can be controlled effectively with an appropriate choice of dc capacitor. An overvoltage is created when the converter output currents are forced to reduce their amplitude, and conversely, an undervoltage is generated when the output currents are forced to increase their amplitude.

The amplitude of the resulting capacitor fluctuation depends on the size and duration of transient changes in the converter output current. The maximum overvoltage value is given by:

$$V_{cmac} = \frac{1}{C} \int i_c(t)\, dt + V_{dc} \tag{3.19}$$

where

V_{cmax} is the maximum voltage across the dc capacitor,

V_{dc} is the steady-state dc voltage,

i_c is the instantaneous capacitor current,

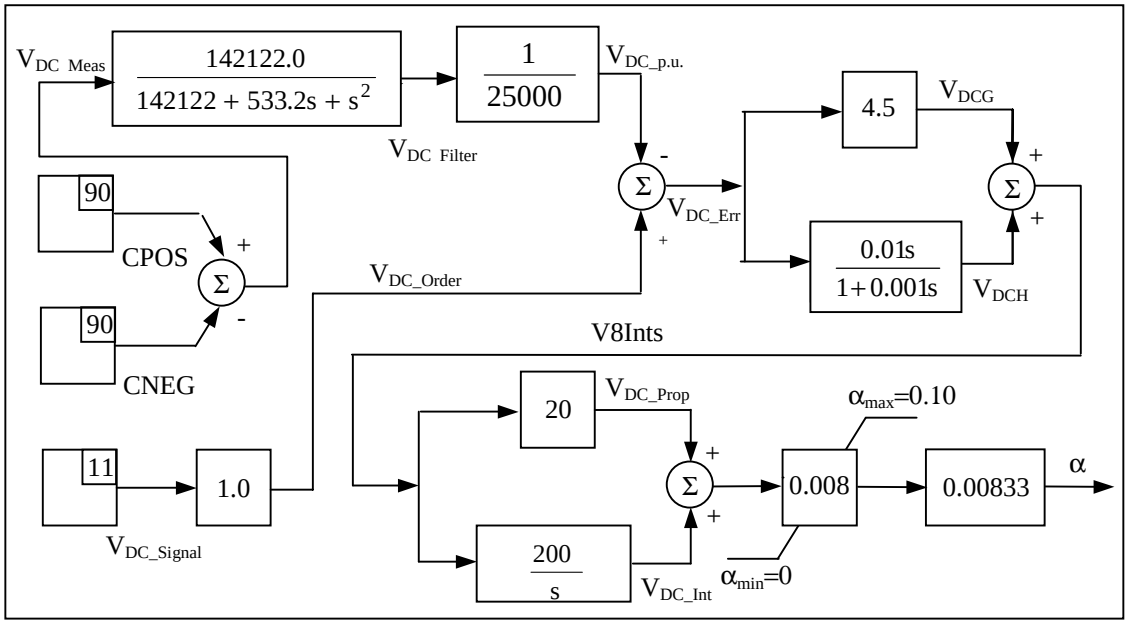


Figure 3.12 – TACS block for dc voltage regulation

From equation (3.19), the value of the dc capacitor can be calculated as:

$$C = \frac{1}{\Delta V}\int_{t} i_c(t)dt \qquad (3.20)$$

where

$\Delta V = V_{cmax} - V_{dc}$ is the allowed voltage fluctuation.

The ac system voltage regulation control loop is shown in Figure 3.13. The ac system voltage at the Bus 8 is controlled by changes in the reactive current of the converter. This current is capacitive (leading), if the fundamental voltage generated by the converter is higher than the fundamental voltage of the line; otherwise, it is inductive (lagging). The rms of the fundamental voltage of the STATCOM varies by varying the amplitude modulation ratio. Consequently, the reactive power is exchanged with the line, keeping the ac system voltage at the desired value. A PI controller is selected for the ac system voltage control loop, since it can achieve zero steady-state error in tracking the reference ac system voltage signal. The proportional and integral gain are kept close to those of the dc voltage control loop, but gain K_d is chosen to be 3.75 bigger making this control loop much faster.

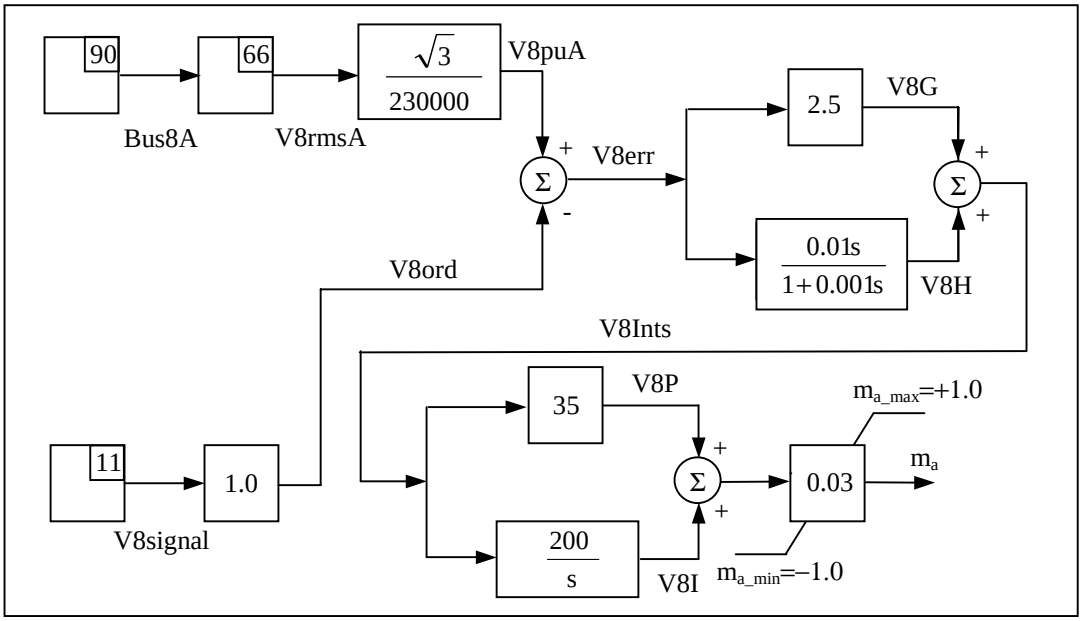


Figure 3.13 – TACS block for p.u. voltage regulation

The gate pulse generator block is shown in detail in Figure 3.14. This is the most basic and fastest loop of the controller and synchronizes the firing pulses of the converter with the ac system voltage. A constant switching frequency is achieved by comparing a sinusoidal waveform with a carrier waveform. The purpose of introducing the carrier

waveform is to stabilize the converter switching frequency, forcing it to be constant and equal to the frequency of the triangular waveform.

Since EMTP does not provide already built a triangular waveform, the sinusoidal waveform of 15 times of the fundamental frequency has been used. The error produced by this replacement is assumed to be small, and therefore, it is neglected.

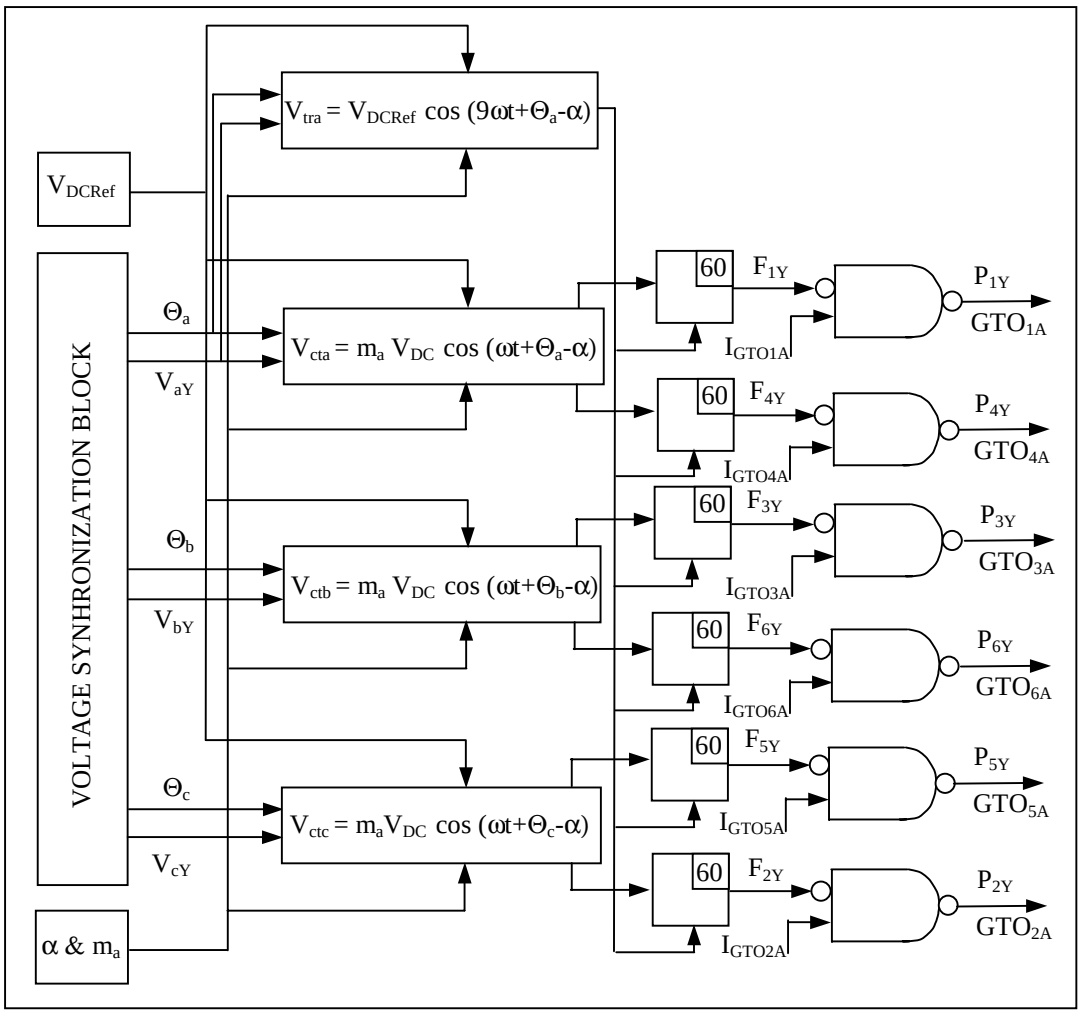


Figure 3.14 – SPWM -TACS block for gate pulse generator

3.4 EMTP Time-Domain Simulations

3.4.1 Capacitor Banks

Figure 3.15 shows the EMTP results for the test system shown in Figure 3.4 with capacitor banks connected at Bus 8, such that the voltage is 1.0 p.u. at nominal load conditions. Increases in load power demand at Bus 10 reduces voltage to an unacceptable low value of 0.84 p.u. at a maximum load of 225 MW. It is interesting to note that the measured load power demand essentially stays the same, even though that load was increased in two steps at 5 s and 6 s because the load is modeled as an impedance, which is sensitive to the voltage magnitude. Decreases in load voltage yield a reduction in load power demand that have a stabilizing effect on the overall power system behavior.

The capacitor banks are passive compensators lacking fast control. Increases in load power demand lead to depressed voltages, which in turn decrease the reactive power generated by the capacitor banks, as the reactive power generated by a fixed capacitor is proportional to the square of the voltage. Therefore, the least reactive power is produced when it is needed the most. Electronically controlled capacitor switching is a possible alternative but would be generally inferior to the dynamic and continuos reactive power capability of a STATCOM. Thus, a STATCOM can be used to minimize the magnitude and duration of system disturbance by regulating the voltage at Bus 8. A compromise the significant costs associated with high capacity STATCOMs, is the combination of capacitor banks and smaller rating STATCOMs. Capacitor banks could be used as basic voltage control, while the STATCOM would be responsible for the dynamic regulation of the voltage.

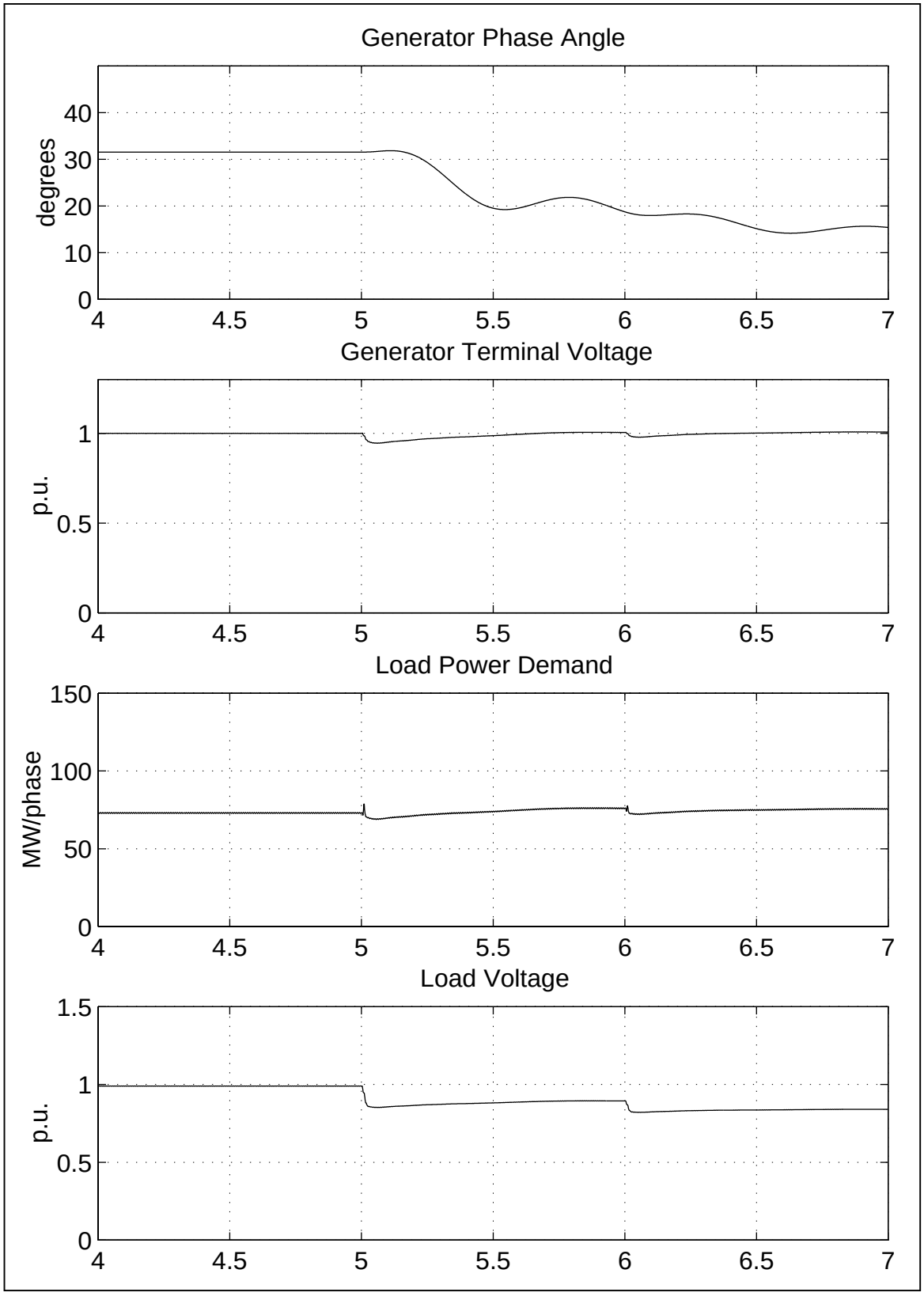


Figure 3.15 –Test system response to load changes with capacitor banks at Bus 8

3.4.2 STATCOM with Phase Control

A voltage profile in the test system shows dynamic amplitude and frequency variations due to the load changes at 5 s and 6 s. Hence, to keep the voltage in the system at an acceptable level, a ± 150 Mvar STATCOM is connected at Bus 8. There is 65 Mvar of reactive power from the passive filters connected on the line side of the STATCOM transformer at the fundamental frequency.

The results obtained with the STATCOM added to the system are depicted in Figure 3.16 and Figure 3.17. Figure 3.16 shows the internal generator phase angle and the AVR controlled generator terminal voltage; the instantaneous ac voltage at Bus 8, the STATCOM ac output current, and the dc voltage and current at the dc capacitor are also shown. The ac voltage at Bus 8 has a sinusoidal shape and does not contain harmonics due to the presence of passive filters. The STATCOM ac output current is measured at the primary side of the transformer and clearly shows its reaction to an increase in load power demand.

Observe that the dc voltage increases from 7.8 kV at 4 s to 8.5 kV at 5 s, and finally to 8.6 kV at 6 s, consequently increasing the STATCOM ac output voltage according to the equation $V_{statcom} = 0.9V_{dc}$, where 0.9 is the constant that relates the dc voltage to the fundamental STATCOM ac output voltage for the twelve-pulse converter. The STATCOM control circuit allows 15 percent increase in V_{dc} from its rated voltage of 7.5 kV; beyond that value the dc capacitor should be protected by keeping the control output angle α at its maximum value α_{max}.

The average dc current is equal to zero at steady state conditions. There are positive deviations at the two transient periods at 5 s and 6 s, due increments in the angle α. The load demand increase is matched by an increase in the instantaneous STATCOM output current, which in turn increases the instantaneous dc current, as the real power on the ac and dc sides of the converter must be the same if the losses are neglected.

In Figure 3.17, the load power demand changes are shown. Notice that the STATCOM control adjusts the angle α so that at 4 s the STATCOM draws capacitive current of 0.12 p.u., at 5 s it becomes 1 p.u., and at 6 s it changes to 1.5 p.u. The ac system voltage is maintained at 1.0 p.u., as required by the control, except at 6 s when it drops to 0.985 p.u. due to the limit in angle α; the dc voltage stays at 8.6 kV which is close to the dc capacitor voltage limit, while the reactive power output of the STATCOM is 150 Mvar, which corresponds to the maximum capacitive current limit.

It is possible to temporarily increase the STATCOM output current by approximately 25% to 35% to respond to transient conditions in the system. It has to be noted that the magnitude and duration of the allowed overcurrent is different for inductive and capacitive regions of operation. The STATCOM can sustain this transient limit for about 2 s after which it has to be returned to its steady-state limit using the control circuit to reduce the angle α. The STATCOM responds to any changes in the ac system voltage within 2 cycles, due to the relatively small transformer reactance, which allows almost instantaneous changes in the STATCOM ac output current to compensate for system voltage variations.

After evaluating the STATCOM response to changes in system load demand, studies were undertaken to determine the STATCOM response and appropriate protections in the case of severe three-phase and line-to-neutral faults placed at Bus 6. The fault is cleared after 6 cycles by disconnecting the faulted transmission line. The resulting protection scheme permits the STATCOM to remain operative during the duration of the fault as shown in Figure 3.18 and Figure 3.19. The protection scheme temporarily reduces the var capacity by keeping the angle α at the value when the STATCOM output ac current reaches its maximum pre-set value. As soon as the current resumes the allowed value, the angle α is free to change in response to system voltage changes. During the fault, the voltage at Bus 8 falls almost to 50 percent of its pre-set value of 1 p.u., while maximum capacitive current is provided by the STATCOM. The fundamental current component, in all three phases, is approximately 2.0 p.u. during the fault. Therefore, the STATCOM is capable of transiently providing capacitive current in excess to the nominal 1.0 p.u.

Figures 3.20 and 3.21 illustrate the response of the STATCOM to the most common power system fault, single-phase line-to-ground fault. The fault is applied for 6 cycles at Bus 6, phase A. The figures illustrate the capacity of the STATCOM to provide maximum capacitive current during low voltage conditions. The fundamental component of the STATCOM output current jumps from 1.0 p.u. in the steady state to approximately 1.9 p.u. during the fault. As it can be seen here, the STATCOM output is the same for all three phases even though the applied system disturbance is clearly unbalanced. This could be remedied by changing the existing control circuit to one where each phase of the STATCOM output voltages and currents are monitored and controlled independently.

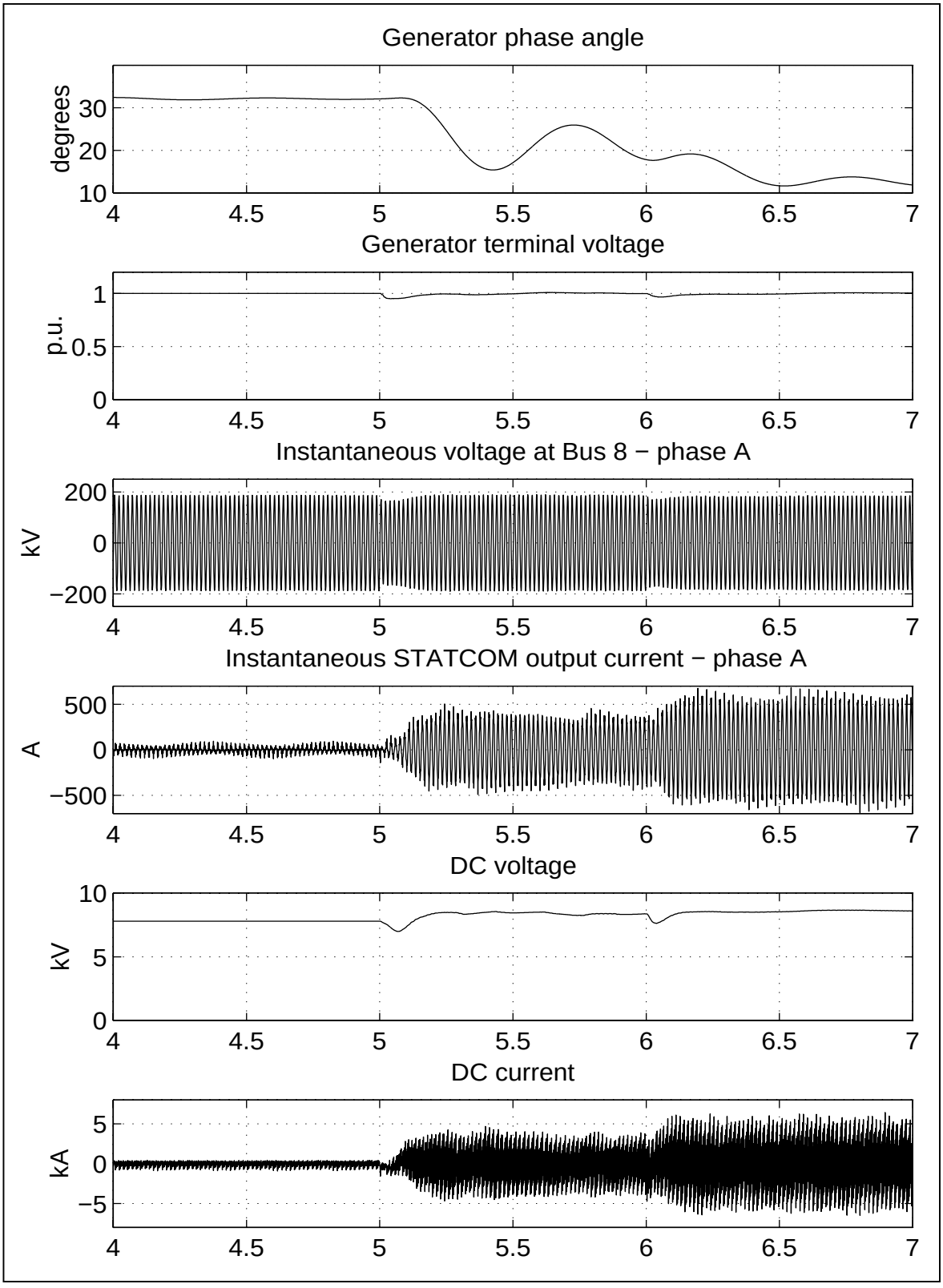


Figure 3.16 – Phase controlled STATCOM response to changes in load conditions

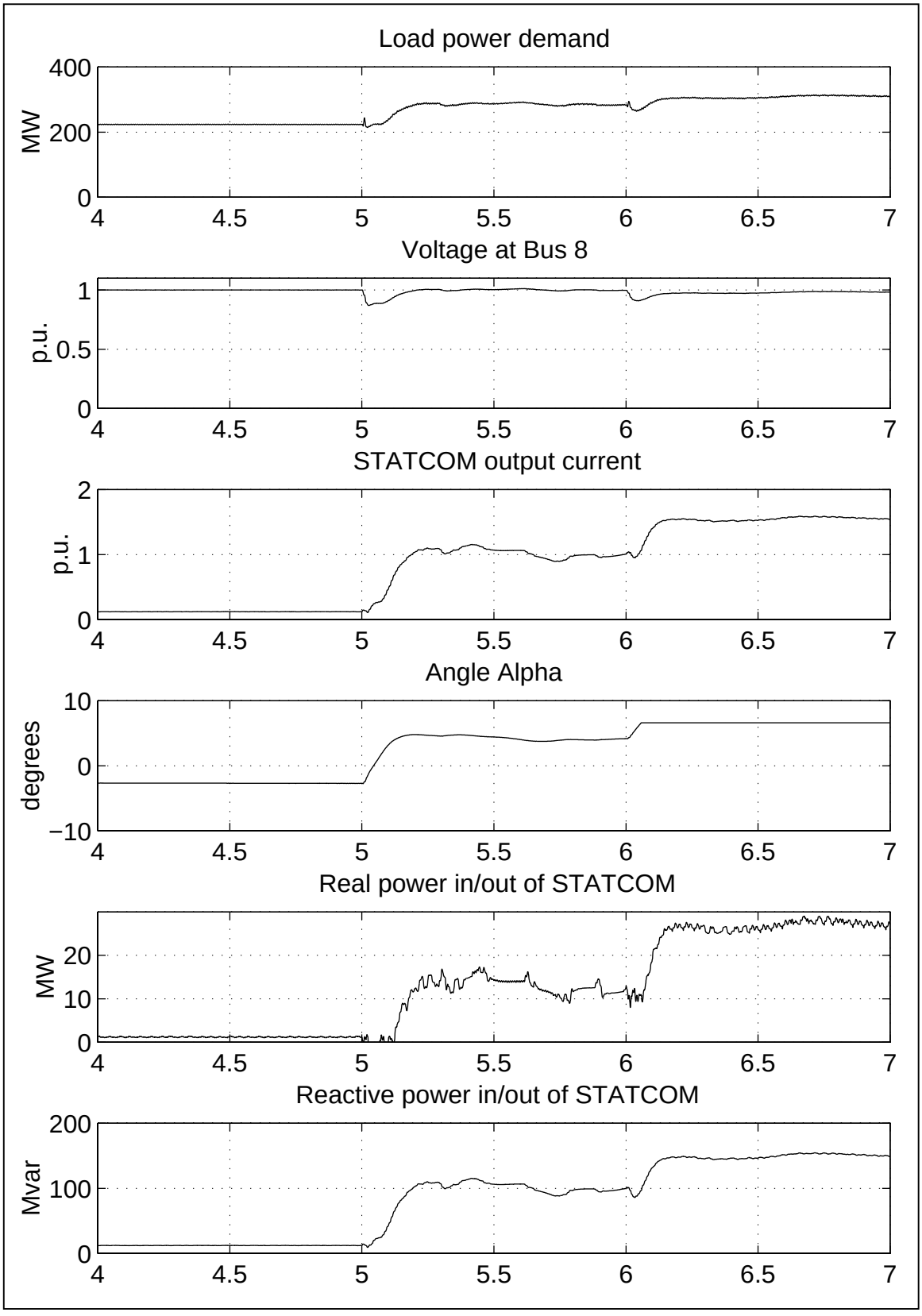


Figure 3.17 – Phase controlled STATCOM response to changes in load conditions

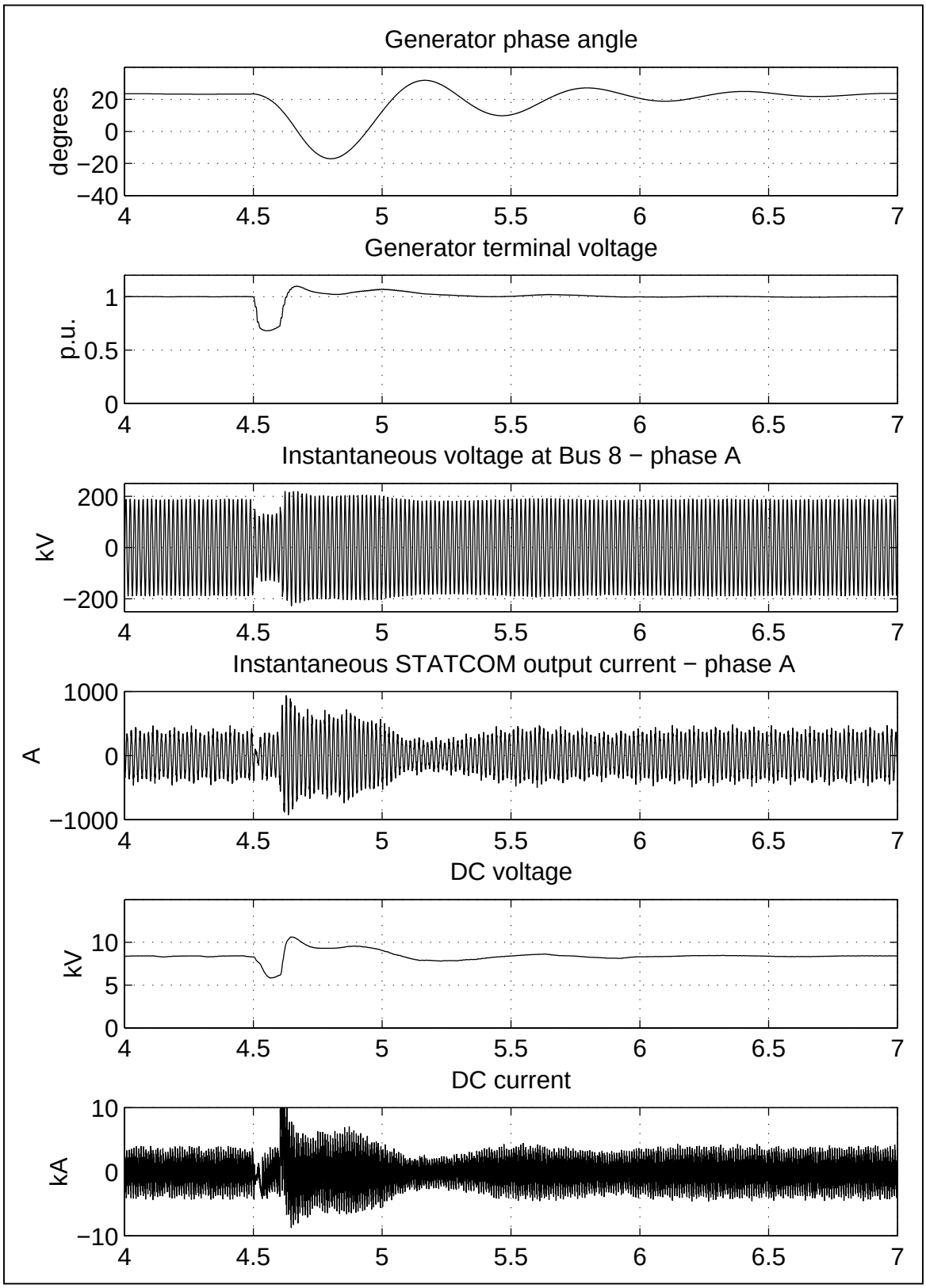


Figure 3.18 – Phase controlled STATCOM response to a three-phase fault at Bus 6

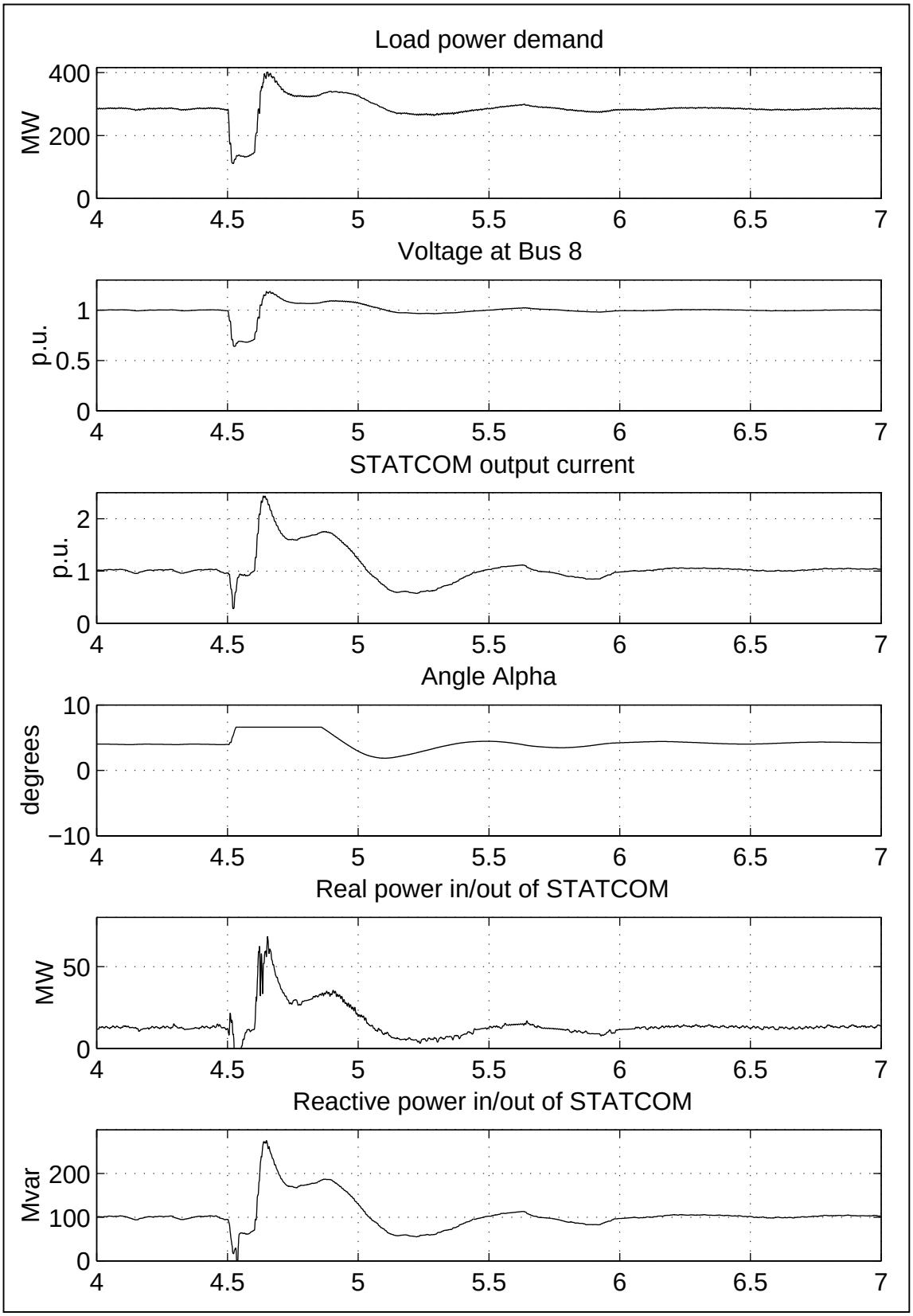


Figure 3.19 – Phase controlled STATCOM response to a three-phase fault at Bus 6

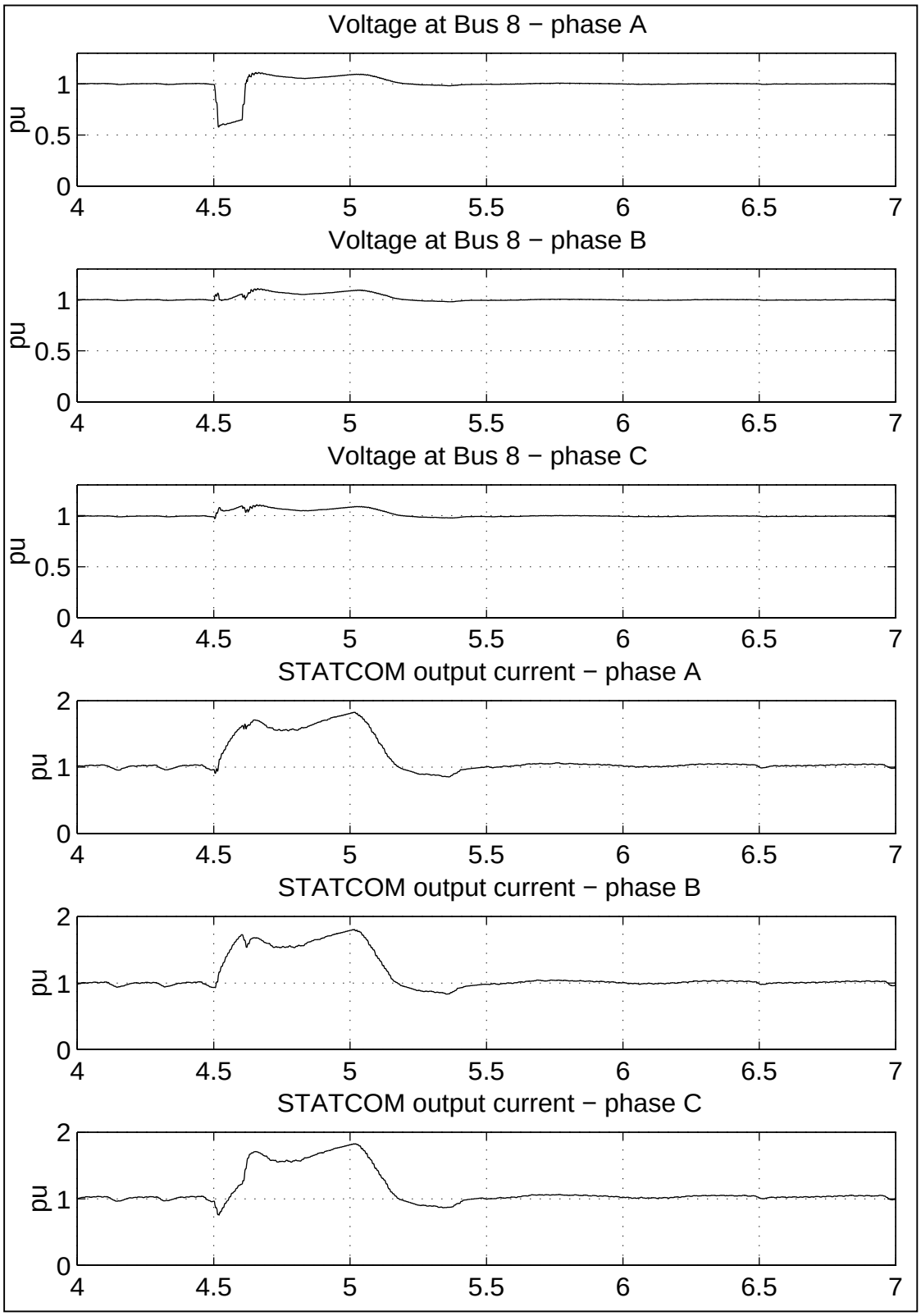


Figure 3.20 – Phase controlled STATCOM response to a single-phase fault at Bus 6

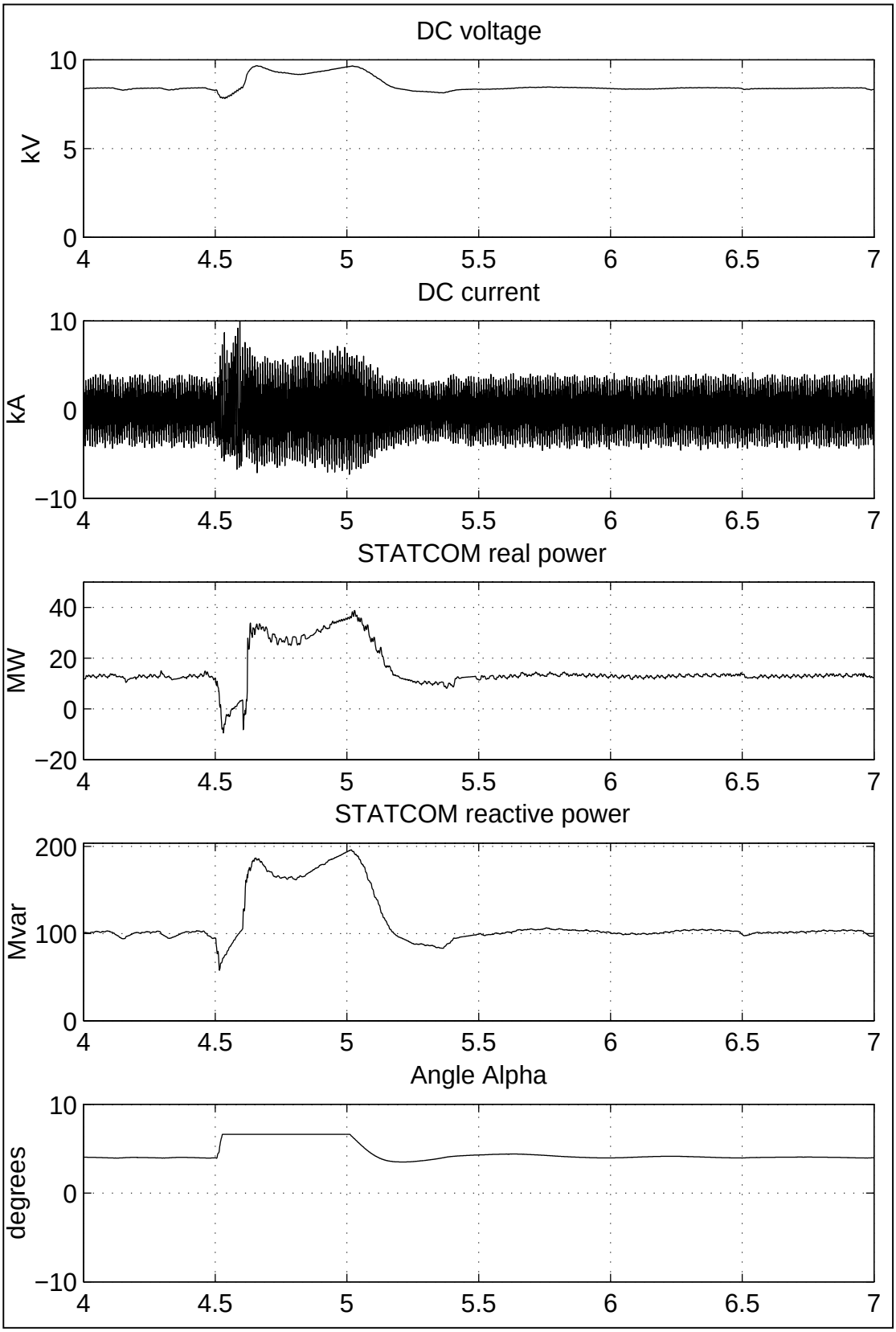


Figure 3.21 – Phase controlled STATCOM response to a single-phase fault at Bus 6

3.4.3 STATCOM with SPWM Control

The dynamic response to changes in load conditions for a Sinusoidal PWM (SPWM) –controlled STATCOM connected at Bus 8 are depicted in Figure 3.22 and Figure 3.23. The load power demand is changed in two steps; at 5 s and 6 s, the three-phase load power demand at Bus 10 is increased, as shown in Figure 3.23. An increase in the load power demand reduces the voltage profiles of the line, which is then corrected by the actions of the STATCOM. The p.u. voltage at Bus 8 is shown in Figure 3.23.

Notice in Figure 3.22 that the dc voltage in the PWM controller is kept constant at 25 kV. The dc voltage at the PWM-controlled STATCOM has to be kept sufficiently high to provide enough margin for the changes in the modulation ratio m_a. Figure 3.22 also shows the instantaneous STATCOM output current waveform. A closer inspection of the waveform shows a small dc component, which could be assigned to the presence of the filter inductance in the STATCOM circuit used to "smooth" the STATCOM output current.

The STATCOM response to a severe three-phase fault is shown in Figure 3.24 and Figure 3.25. The fault is applied at 0.455 s at Bus 6 and is cleared by opening the breaker between Bus 3 and Bus 5 after 6 cycles. During the fault, the voltage at Bus 8 falls to an unacceptable low value of 0.35 p.u., which leads to an instant STATCOM response in an attempt to support the voltage magnitude. During this period, angle α has reached its maximum allowed value of 25^0, helping in the recovery of the dc voltage during the fault. After the fault, the dc voltage, as well as the Bus 8 voltage, experience an overvoltage, which is then reduced by a reduction in the angle α.

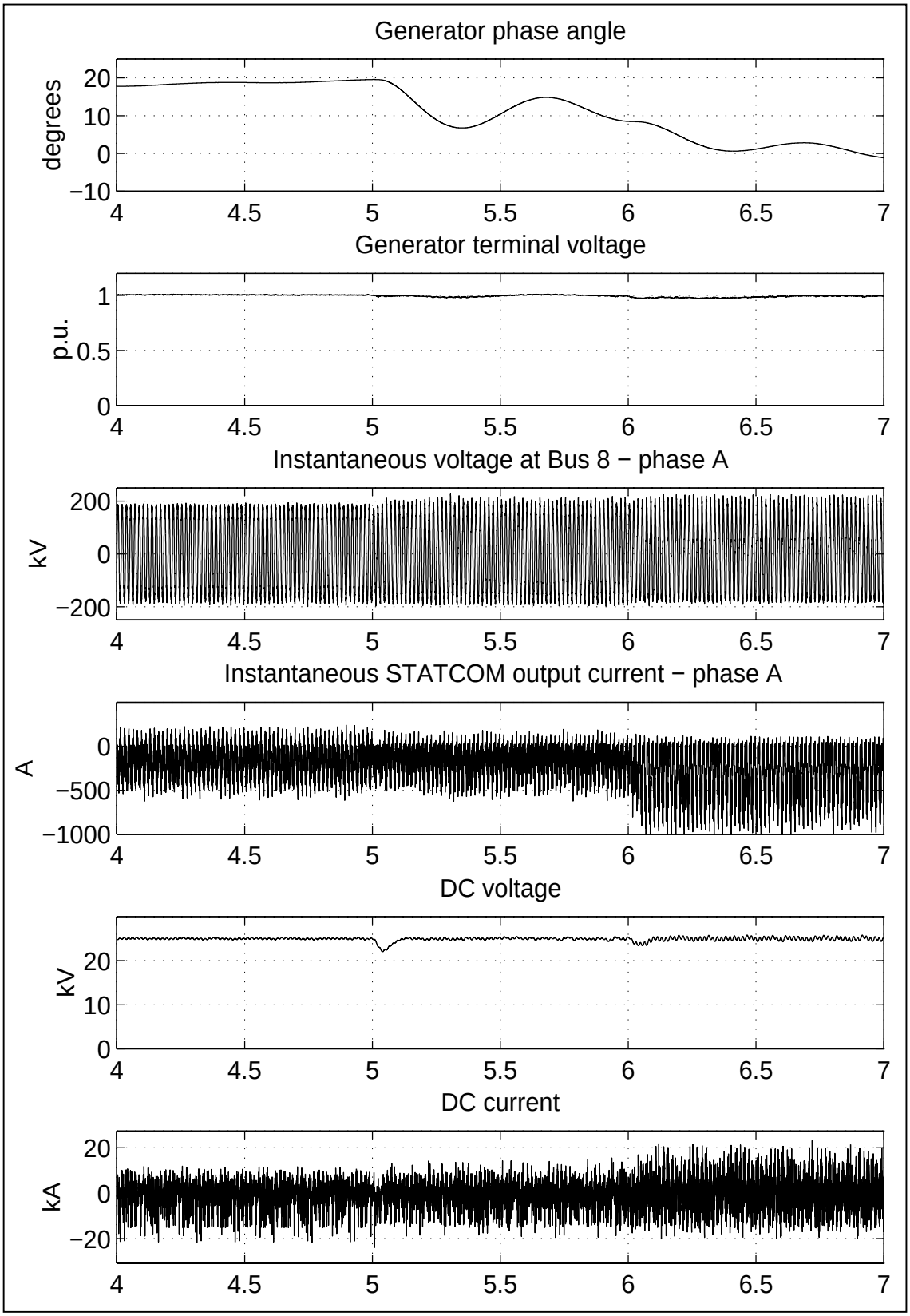


Figure 3.22 – SPWM controlled STATCOM response to changes in load conditions

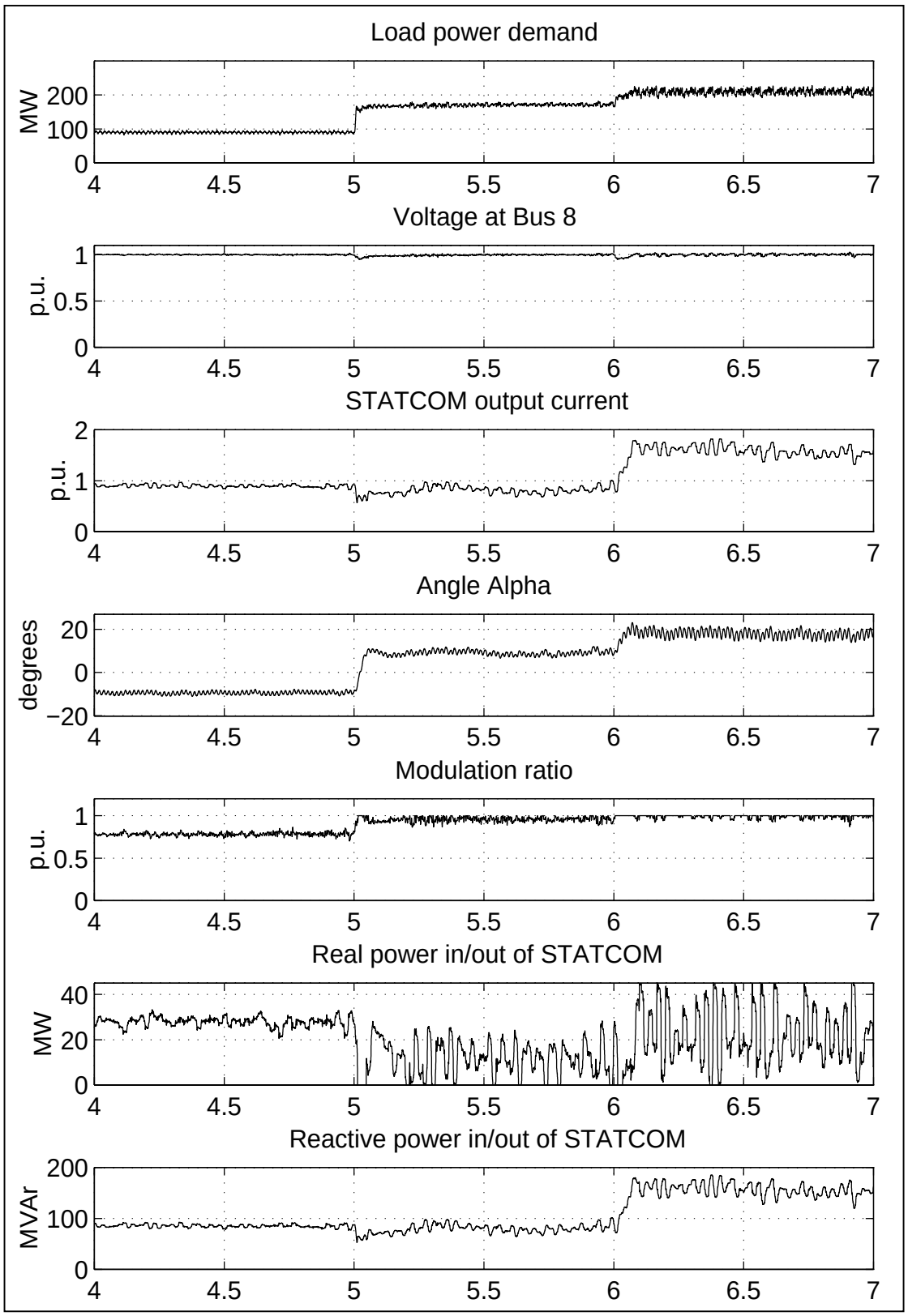


Figure 3.23 – SPWM controlled STATCOM response to changes in load conditions

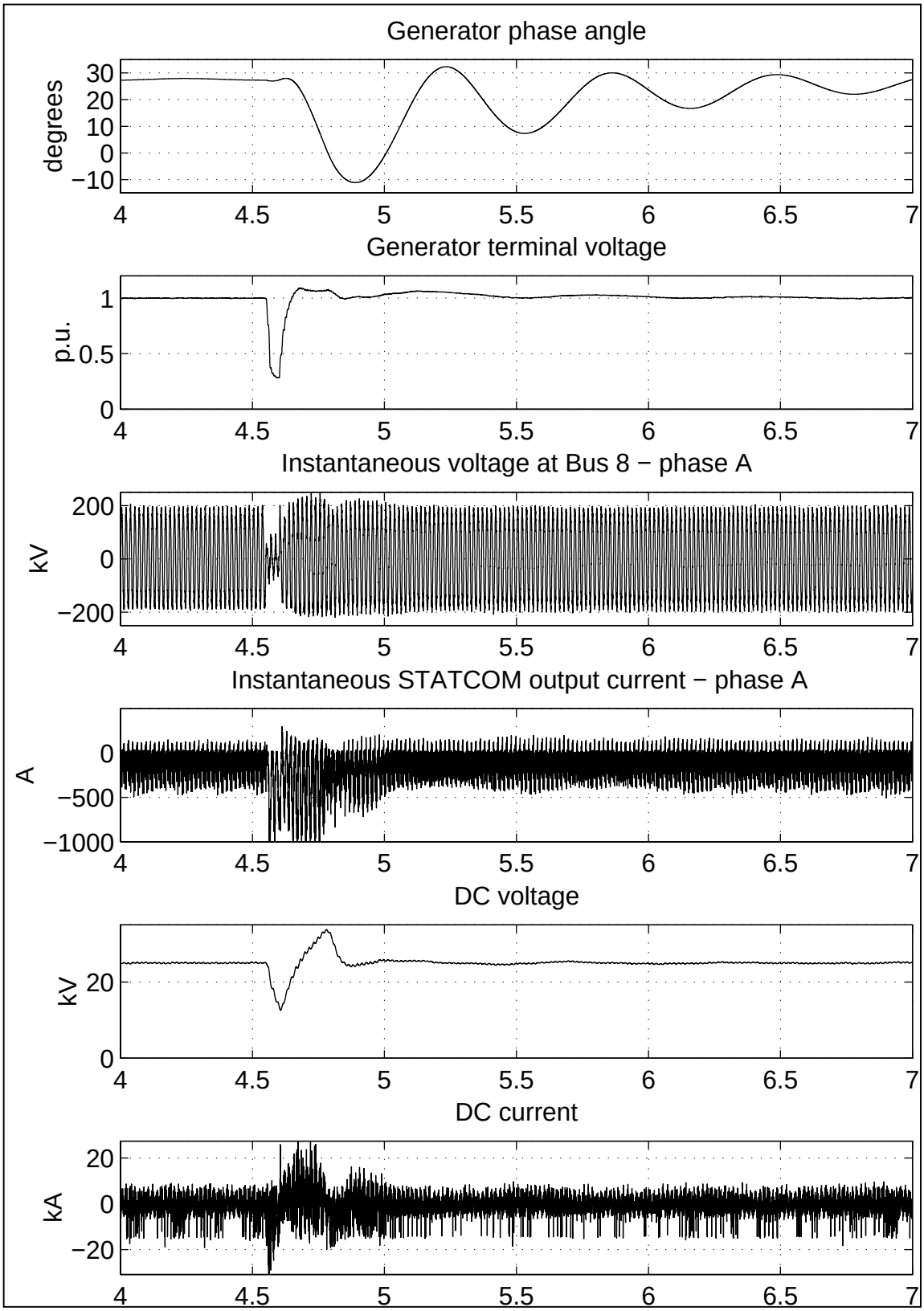


Figure 3.24 – SPWM controlled STATCOM response to a three-phase fault at Bus 6

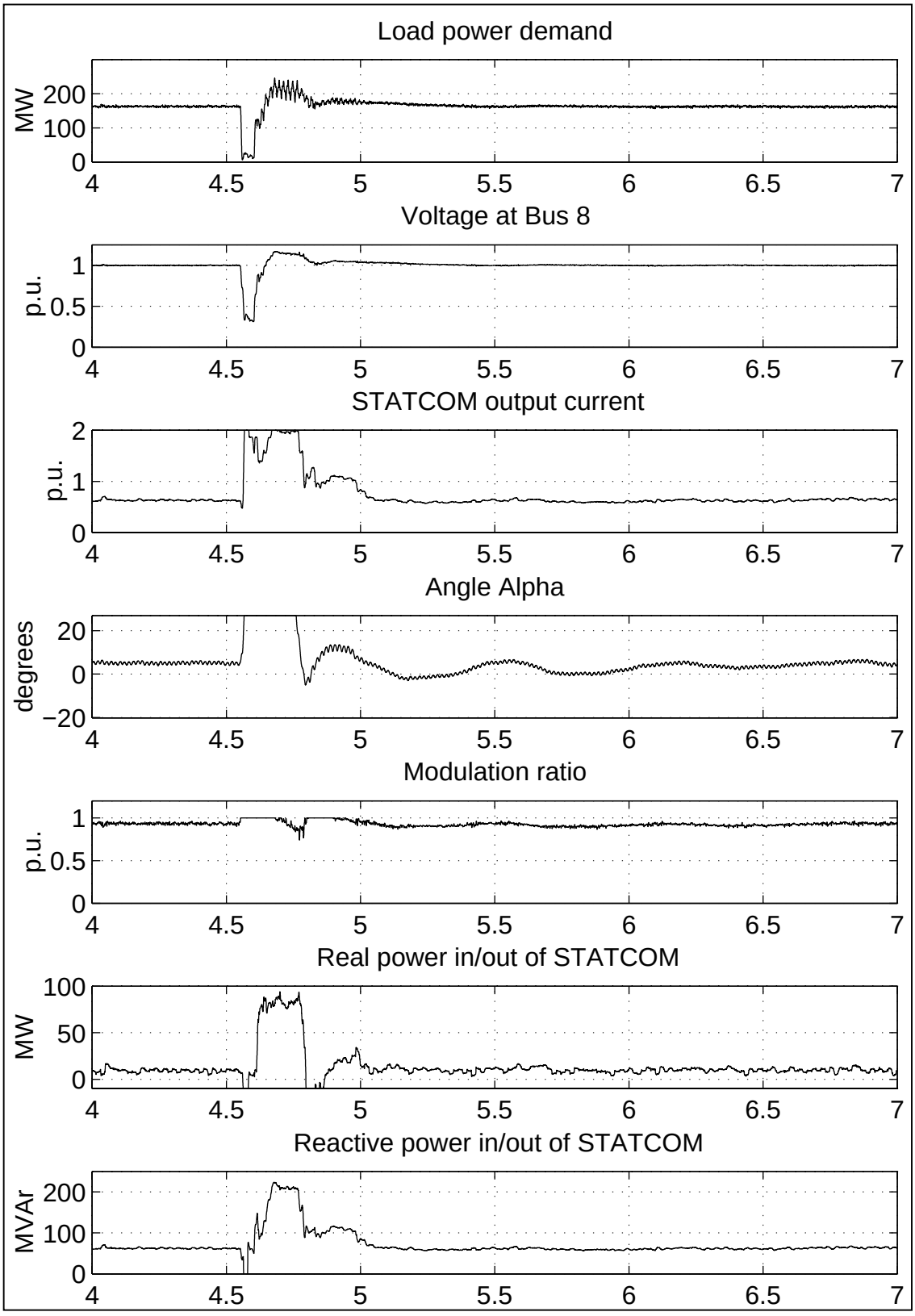


Figure 3.25 – SPWM controlled STATCOM response to a three-phase fault at Bus 6

3.5 Summary

The general concepts of power system stability under shunt compensation are described along with the theory and basic equations of a STATCOM. Historical development of the high power electronic converters was reviewed.

The performance of the STATCOM is discussed and compared with respect to a conventional SVC, from the point of view of the mitigation of stability problems in power systems. It is shown that the STATCOM provides better performance than the SVC in the enhancement of dynamic and transient stability. The total cost associated with the STATCOM is generally higher than the cost of the SVC; however, it is concluded that with further developments in the power electronics industry, the cost of the STATCOM will be more competitive.

A twelve-pulse STATCOM, using two two-level voltage-sourced converters, is successfully modeled in the EMTP, including a detailed representation of the valves and the accompanying snubber circuits. Also, the PWM based STATCOM is modeled in the EMTP using a one two-level voltage-sourced converter. The presented time-domain simulations in EMTP verify the adequate operation of the designed controller, demonstrating successful applications of two kinds controllers, i.e., PWM and phase controllers. The implementation and the design for the PWM controller are simpler than for phase control, due to the easy separation of the active and reactive components of the STATCOM output current without a need for a d-q decomposition. This will be particularly important in designing a controller for the UPFC, which has the inherent capability to control active as well as reactive power flow. Also, independent control of each phase voltage is only achievable in the PWM control. It is shown that classical and simple PI controllers are suitable for STATCOM control.

The PI-based controllers have shown satisfactory response in the symmetrical three-phase ac system conditions. As ac systems are exposed to different disturbances, for instance a single-phase fault is the most common fault in the ac system which give non-

symmetrical operating conditions, it is necessary to improve the STATCOM response when three-phases are non-symmetrical. For a STATCOM with PWM-based controller, the fundamental component of converter output voltage can be easily controlled from the maximum value to zero independently in each phase. Therefore, it is possible for the PWM converter to control each phase current independently. This is not possible for phase-control based STATCOM due to fact that all three phases are directly proportional to the dc voltage, without possibility to adjust them independently.

Chapter 4.

SERIES SYNCHRONOUS STATIC COMPENSATOR
SSSC

4.1 Introduction

This chapter addresses the problem of controlling and modulating power flow in a transmission line using a Synchronous Static Series Compensator (SSSC). The EMTP simulation studies, which include detailed representations of twelve-pulse and PWM-controlled SSSC, are conducted and the control circuits are designed. The developed control strategies for both twelve-pulse and PWM-controlled SSSC use direct manipulations of control variables instead of typical d-q transformations, which further simplifies the control circuits, as shown in sections 4.5.2 and 4.5.3.

The STATCOM and UPFC operating principles and control circuit design are documented more extensively in the literature than the SSSC operating characteristics, particularly with regards to control circuits design. This thesis explains in detail the SSSC operation and control circuit design process, which should be beneficial for future research work. For example, the PWM-controlled SSSC presented in this thesis is not properly documented in the literature, even though the idea itself is not new.

Again, the developed SSSC models, as in the case of the STATCOM models, are unique, since the EMTP implementation is not an easy task. Furthermore, the models developed are included into a realistic test system, which cannot be found in the current literature. The presented detailed models of the SSSC are particularly useful in control and protection circuits design, as these realistically reproduce the controller response in a power system.

4.2 Basic Operating Principles

The SSSC controller consists of a solid-state VSC with several GTO thyristor switches, or any other semiconductor switches with intrinsic turn-off capability valves, a dc capacitor, a transformer, and a controller. The basic converter circuit is already explained in Chapter 2; it is important to note that several of the VSCs can be connected together through a transformer of sometimes a complex and custom made design configuration. The number of valves, and the various configurations of the transformer depend on the desired quality of ac waveforms generated by the SSSC. Another approach involves PWM-controlled VSCs where the quality of the ac output waveforms depends on the switching frequency.

The line side transformer winding is connected in series, placing the VSC also effectively in series with a transmission line, and thus allowing series compensation of the line. The SSSC is used to generate or absorb reactive power from the line, and hence can be utilized as a transmission line power flow controller. Basically, it generates on its output terminals a quasi-sinusoidal voltage of variable magnitude in quadrature with the transmission line current, if the SSSC losses are neglected. Thus, the line injected voltage emulates a capacitive or an inductive reactance in series with a transmission line, which increases or decreases the total transmission line reactance, resulting in a decrease or increase of the power flow in the transmission line.

In general, the SSSC can be viewed as analogous to an ideal synchronous voltage source as it can produce a set of three-phase ac voltages at the desired fundamental frequency of variable and controllable amplitude and phase angle. It also resembles a synchronous compensator, as it can generate or absorb reactive power from a power system and can, independently from the reactive power, generate or absorb real power if an energy storage device instead of the dc capacitor is used in the SSSC.

The SSSC is typically restricted to only reactive power exchange with the nearby ac system, neglecting the small amount of real power used to cover the circuit and switching

losses, because of the relatively small SSSC capacitor. If the dc capacitor were replaced with an energy storage system, the controller would be able to exchange real power with the ac system and compensate for the transmission line resistance. Alternatively, a STATCOM could send real power to the SSSC through a common dc capacitor. The combined controller formed by this connection is called a Unified Power Flow Controller (UPFC), as explained in more detail in Chapter 5.

Figure 4.1 shows a functional model of the SSSC where the dc capacitor has been replaced by an energy storage device such as a high energy battery installation to allow active as well as reactive power exchanges with the ac system. The SSSC's output voltage magnitude and phase angle can be varied in a controlled manner to influence power flows in a transmission line. The phase displacement of the inserted voltage $\mathbf{V}_{pq}$, with respect to the transmission line current $\mathbf{I}_{line}$, determines the exchange of real and reactive power with the ac system.

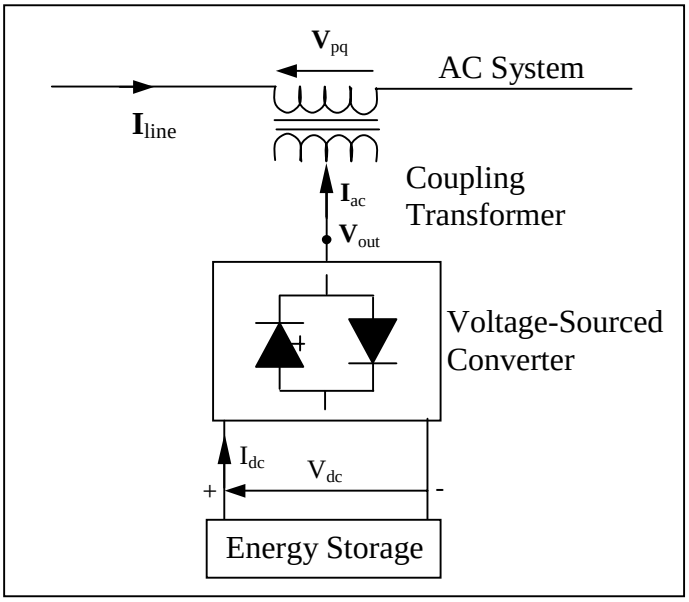


Figure 4.1 – Functional model of SSSC

Figure 4.2 shows the SSSC operation in four quadrants, again assuming an energy storage device connected at the SSSC's input terminals. The line current phasor $\mathbf{I}_{line}$ is used as a reference phasor while the injected SSSC voltage phasor is allowed to rotate

around the centre of the circle defined by the maximum inserted voltage $\mathbf{V}_{pq}^{max}$. Theoretically, SSSC operation in each of the four quadrants is possible, but there are some limitations to the injected SSSC voltage due to operating constraints of practical power system.

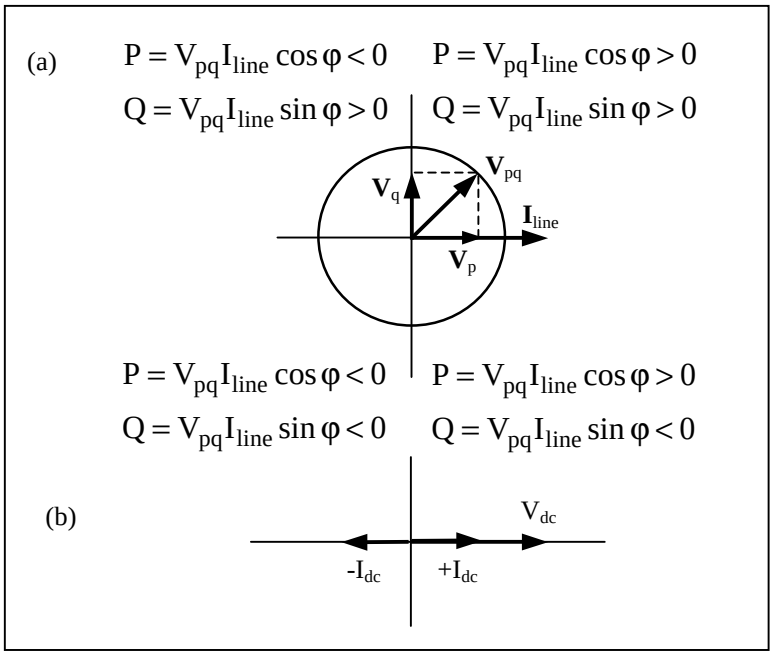


Figure 4.2 – SSSC phasor diagram

In capacitive mode, the injected SSSC voltage is made to lag the transmission line current by 90^0; in this case, the SSSC operation is similar to the operation of a series capacitor with variable capacitance kX_c, i.e., $\mathbf{V}_{pq} = -jkX_c\mathbf{I}_{line}$, where k is a variable. By this action, the total transmission line reactance is reduced while the voltage across the impedance is increased, leading to increase in the line currents and transmitted power. This action is illustrated in Figure 4.3.

It is also possible to reverse the injected SSSC voltage by 180^0, i.e., $-\mathbf{V}_{pq} = jkX_c\mathbf{I}_{line}$, causing an increase in the transmission line reactance, which results in a decrease of the line current and transmitted power. While this equation for $\mathbf{V}_{pq}$ shows

changes in the phasor magnitude and phase angle, it can be somewhat misleading, since it shows that the series injected voltage magnitude is directly proportional to the line current magnitude. In reality, this is not true; the inserted voltage magnitude is set by the SSSC control and is independent of the network impedance and, consequently, line current changes. In Figure 4.3, it is assumed that the SSSC losses are zero and, therefore, the series injected voltage is in perfect quadrature with the line current, leading or lagging.

The operating conditions that limit the SSSC operation from the power system point of view are also depicted in Figure 4.3. The SSSC can increase as well as decrease the power flow in the transmission line by simply reversing the operation from capacitive to inductive mode. In the inductive mode, the series injected voltage is in phase with the voltage drop developed across the line reactance; thus, the series compensation has the same effect as increasing the line reactance. If the series inserted voltage magnitude is larger than voltage drop across the uncompensated line, i.e., $V_{pq} \geq V_{Line}$, the power flow will reverse. This fact can limit the SSSC operation to values of $V_{pq} \leq V_{Line}$, as in practice, it would be unlikely to use the SSSC for power reversal. Also, if the rating of the SSSC controller is high, it is possible to increase or decrease the receiving end voltage above or below the typical operating voltage range of 0.95 p.u. – 1.05 p.u., but with possible negative consequences for other system devices.

The SSSC output current corresponds to the transmission line current, which is affected by power system impedance, loading and voltage profile, as well as by the actions of the SSSC. Thus, the relationship between the SSSC and the line current is complex. The fundamental component of the SSSC output voltage magnitude is, on the other hand, directly related to the dc voltage that is either constant or kept within certain limits, depending on the chosen design and control of the SSSC.

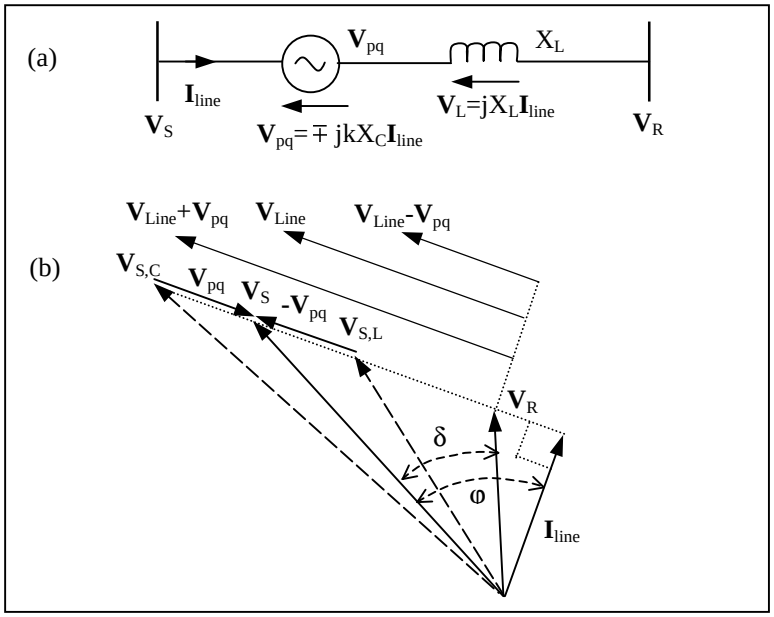


Figure 4.3 – Series compensation by a SSSC

The SSSC output voltage phase angle is correlated to the line current phase angle by plus or minus few degrees for example, to account for changes in the dc voltage. It has to be noted that the injected SSSC voltage V_{pq} is different from the SSSC output voltage V_{SSSC}, due to the voltage drop or rise across the series transformer reactance, i.e.,

$$V_{pq} = V_{SSSC} \mp X_{tr} I_{line} \tag{4.1}$$

where the minus sign corresponds to capacitive operation, while the positive sign corresponds to inductive operation of the SSSC and X_{tr} stands for the series transformer reactance. This voltage difference between the injected and output SSSC voltage can be small in the case of small transmission line currents, but it can be significant in high loading conditions.

The active and reactive power exchanged between the SSSC and the transmission line can be calculated as follows:

$$P_{pq} = V_{pq} \cdot I_{line} \cos \varphi \quad (4.2)$$

$$Q_{pq} = V_{pq} \cdot I_{line} \sin \varphi \quad (4.3)$$

where φ represents the angle between the injected SSSC voltage and transmission line current.

Inspection of the equations (4.2) and (4.3), considering that the angle between the SSSC output voltage and line current is approximately 90^0, shows that the SSSC real power should be small compared to the reactive power. This is expected, since the real power going into the SSSC is used only to cover for the losses and charging of the dc capacitor, i.e.,

$$P_{pq} = P_{dc} + P_{losses} \quad (4.4)$$

The losses in the SSSC circuit are due to the transformer windings and especially due to the switching of the GTO valves.

4.3 Rating of the SSSC equipment

The SSSC ratings and, therefore, the amount of the real and reactive power that can be exchanged with the power system, are determined by ratings of its components, namely, the dc capacitor (energy storage device), VSC, and the series connected coupling transformer. The dc capacitor or energy storage device limits are characterized by its voltage and current ratings; the dc bus voltage V_{dc} should not exceed the voltage rating of the dc capacitor or energy storage device. To prevent overvoltages, in most cases, arresters are used in parallel with the dc capacitor. Also, to prevent the misfiring of the GTO thyristors, the dc voltage must always be above certain level. The current rating determines how fast the dc capacitor can be charged or discharged, and it must be $I_{dc,min} \le I_{dc} \le I_{dc,max}$.

Special care has to be taken in choosing the right size of the dc capacitor, considering both technical and economical factors. A large dc capacitor would need longer periods for charging and discharging, but large voltage variations on the dc side during a transient on the ac side would be avoided in this case. Reducing dc voltage variations, especially dc voltage increases, would avoid the need for special dimensioning of the semiconductor components, having a positive effect on the overall costs. Some authors suggest that the dc capacitor should be sized to a maximum ripple of 10 % in the dc voltage [12]. The work presented in [60] shows that a reference value of 2.65 ms for the capacitor time constant corresponds to a 10 % ripple in the dc voltage.

The converter GTO thyristor valves are also characterized by their current and voltage ratings. As was the case with STATCOM, the GTO thyristor valves for the SSSC are composed of several GTO thyristors connected in series to achieve the desired voltage level. The voltage rating of the valve is the sum of the rated voltages of the individual thyristors minus a derating factor; the usual practice is to place one additional GTO thyristor as a reserve in a case of failure of one GTO's in the string, assuming that the failed GTO goes immediately into short-circuit state. The valve current rating include both, instantaneous and RMS currents. The RMS current ratings translate into restrictions on the converter output currents at the ac side: $I_{line} \leq I_{rating}$ for continuous operation, and $I_{line} \leq I_{transient}$ for a 1s transient overload [51]. The time of the continuous and transient overload is a function of the GTO heating characteristics and the cooling system, and is different for different applications.

The SSSC volt-ampere rating is also the rating of the series coupling transformer; its rating is determined by a product of the maximum injected SSSC voltage and the maximum transmission line current, i.e., $MVA = I_{line,max} \cdot V_{SSSC,max}$. Note that in practical applications I_{max} may represent the rated maximum steady state line current or a specified short duration overcurrent. Based on this, there are two recognizable SSSC ratings: steady state and short duration MVA rating.

The V-I characteristic of the SSSC is shown in Figure 4.4. As it can be seen from this figure, the SSSC can provide capacitive and inductive voltage up to its specified maximum current rating. In this Figure, it is assumed that the SSSC can maintain its rated maximum capacitive and inductive voltage even in the situations when the line current is equal to zero. In practice, this is not the case. The practical minimum line current is the one at which the SSSC's dc capacitor voltage can be kept at the desired level while supplying for the controller losses. Also, it has to be noted that if the voltage drop/rise across the transformer leakage reactance is included into Figure 4.4, the V-I characteristic changes to that depicted with dashed lines. This difference between the V-I characteristics is greater at high transmission line currents, and in some applications it can be as high as 40 % of the series voltage nominal rating.

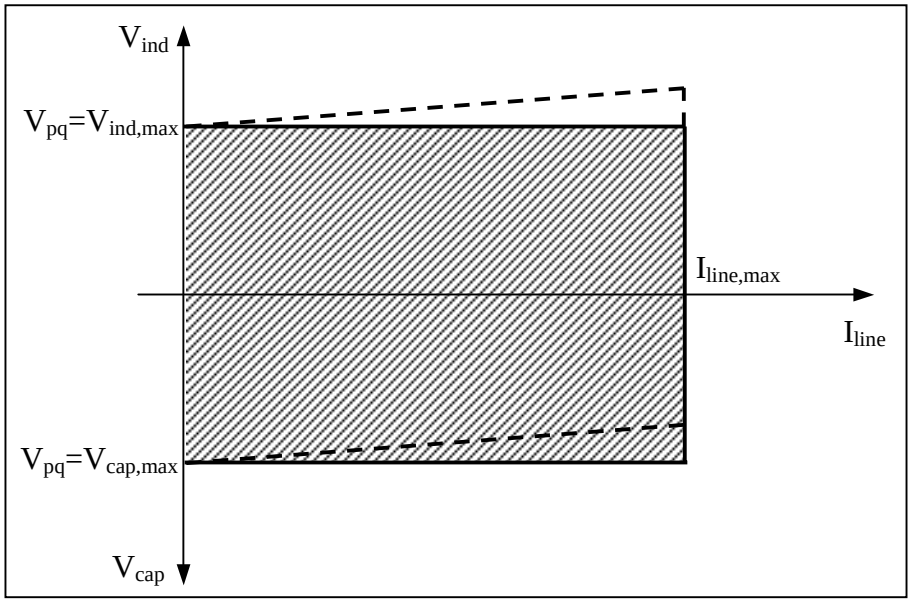


Figure 4.4 – V-I characteristics of the SSSC

4.4 SSSC Control Systems

In this thesis, two different control techniques, one based on multi-pulse phase control and another based on PWM control, are discussed, implemented and tested. These two control techniques are sometimes characterized as "indirect" and "direct"

controls [42]. An indirectly or phase controlled VSC allows control of the output voltage angular position only; the magnitude remains proportional to the dc terminal voltage directly controlled by appropriate valve gating. For directly or PWM controlled converters both the angular position and the magnitude of the output voltage are controllable. The control objective in both techniques is to achieve a desired current in the compensated line based on a set reference level. The proposed control schemes instead of using d-q decomposition use direct control variables, i.e. transmission line current, to achieve desired line power flow.

The SSSC control scheme has two major functions. One function is to establish the desired capacitive or inductive compensation by an externally fixed reference, where the reference could be an impedance Z_R, the series injected voltage V_{SSSC}, or simply the current in the compensated line I_{line}. The second function is to modulate the series reactive compensation so as to improve transient stability and provide power oscillation damping [58].

In [53], the switching frequency of the GTOs for the proposed SPWM scheme was three turn-on and turn-off operations per fundamental cycle. This proposed control scheme resulted in lower switching losses of the VSC, but pronounced low order harmonics of the SSSC's ac output voltage. The choice of the amplitude modulation ratio of $m_a = 0.8$ eliminated the 5^{th} harmonic; this fact, combined with the proposed low rating of the SSSC, did not significantly affect the harmonic profile of the line current. However, in high power transmission applications, this control scheme would certainly affect the harmonic profile, and higher switching frequencies should be used. This would increase the VSC switching losses using today's GTOs; hence, PWM schemes are ruled out for now in high power applications.

In [54], the NETOMAC program was used to verify a detailed SSSC model, including a basic control system that enables the SSSC to follow the changes in the reference value of the active power supplied by an outer system controller. A d-q decoupled control structure with a predictive control loop based on the transformation of the three-phase system to the rotating reference frame was used. The presented SSSC

model has a generic structure that allows the use of PWM as well as phase angle control schemes.

Reference [55] proposes a three-level VSC structure and 24-pulse operation for a modeled SSSC. According to the chosen VSC structure, the author uses a phase control technique to dynamically regulate the dc link capacitor voltage in relationship with the insertion voltage amplitude demand, since the VSC output voltage amplitude on the converter side of the series transformer and the dc link capacitor voltage demand are directly related by the converter dc-to-fundamental ac amplitude gain factor of $K_{conv}=2/\pi$.

4.5 SSSC Design

4.5.1 Test System Description

In order to validate the proposed control strategy, a test system, introduced in [50] and modified to serve the purpose of this thesis, has been implemented in the EMTP. The 11-bus test system is shown in Figure 4.5, and is based on the system used in Chapter 3.

In this case, the transmission system has been changed so that the lower transmission branch has two parallel ac lines with identical parameters but different length resulting in an unequally divided power flow. After some EMTP simulations and careful assessment of the SSSC role in the test system, it was determined that the SSSC could be used to equalize or reschedule the power flow between these two parallel ac lines.

Two transformers with their line side windings connected in series for a total of 70 MVA, 30 kV / 6 kV are used to couple the twelve-pulse SSSC into the ac system. The voltage ratio of the SSSC transformer was chosen so that the SSSC would have an acceptable control range for the given loading conditions. The total leakage reactance with respect to a 100 MVA system base is 14.5 %.

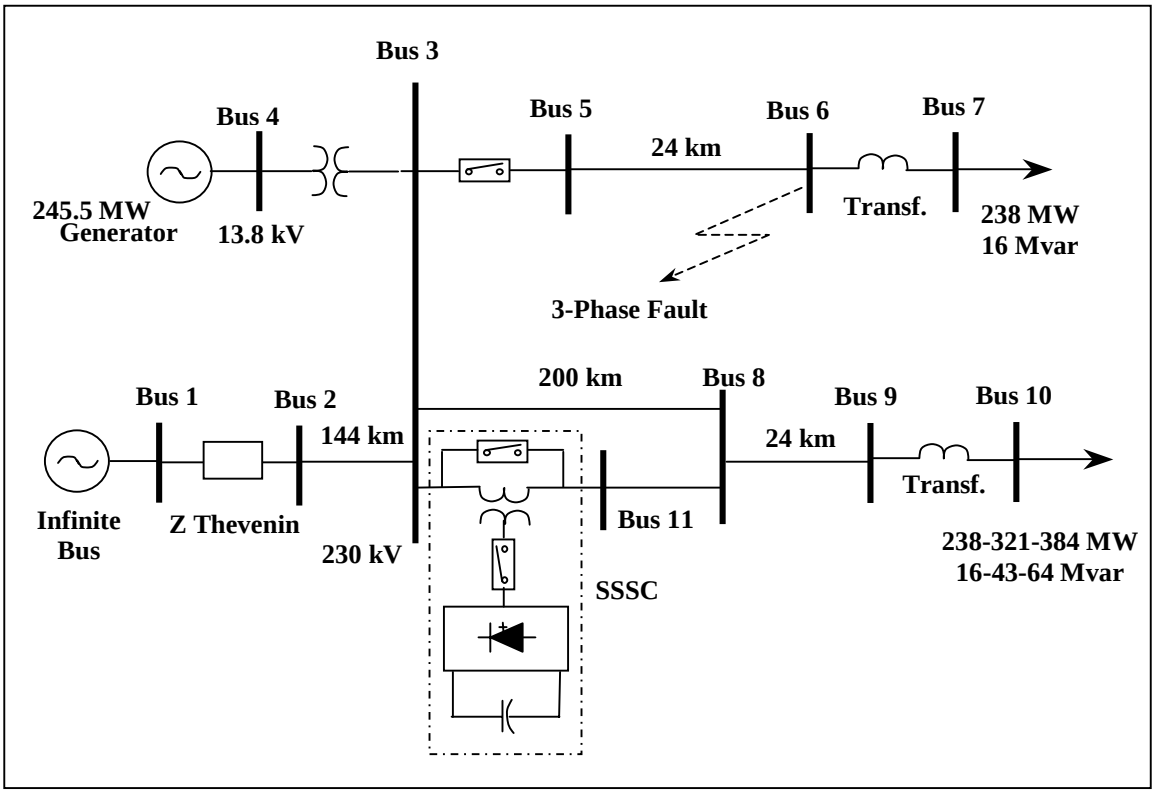


Figure 4.5 – 11-Bus test system

No external filters, or higher than twelve-pulse operation, is modeled since the SSSC steady-state output voltages are sufficiently sinusoidal to satisfy the basic objective of this thesis. The detailed model is used as a basis for comparisons with the reduced, fundamental frequency model, as will be discussed in Chapter 5. The SSSC rating is chosen according to the following equation:

$$\mathrm{MVA}_{3\mathrm{Phase}} = 3 \cdot \mathrm{I}_{\mathrm{line}}^{\mathrm{max}} \cdot \mathrm{V}_{\mathrm{SSSC}}^{\mathrm{max}} = 3 \cdot 753\mathrm{A} \cdot 30\mathrm{kV} = 68 \qquad (4.5)$$

where the 753 A current corresponds to 3 p.u., which is the thermal limit of the transmission line. The voltage of 30 kV is 23 % the transmission voltage rating, and is chosen so that it is possible to change the transmission line current from 1 p.u. to 2.0 p.u.

4.5.2 Phase Control Technique for SSSC

The controlled switches and diodes are respectively modeled by the equivalent functions in TACS and in the EMTP circuit models [50, 56]. The switches are considered ideal switches, but to somewhat account for the losses in the converter circuit and also to satisfy basic connection requirements in the EMTP, a resistor is added between every two switches. The required snubber circuits, in series and in parallel with a GTO switch, are also included in the model.

The modeled SSSC circuit with its two six-pulse VSCs and their series transformers is shown in Figure 4.6. The converters are connected in series to the transmission line through two banks of lossless three-phase single-phase two-winding transformers with no saturation. The dc sides of the converters are connected in parallel and share the same dc bus.

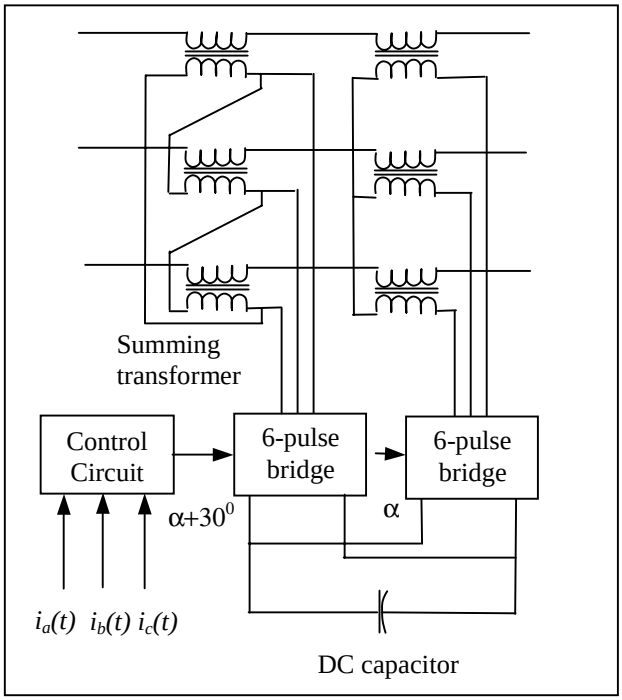


Figure 4.6 – Transformer configuration of 12-pulse SSSC

The GTO valves are switched at fundamental frequency, and the dc voltage varies according to the phase control technique used to control the output voltage. The SSSC switching is synchronized with respect to the transmission line current i_{line}, and its rms magnitude I_{line} is controlled by transiently changing the phase shift α between this current and the SSSC output voltage v_{pq}. The change in the phase shift between the SSSC output voltage and the line current results in the change of the dc capacitor voltage V_{dc}, which ultimately changes the magnitude of the SSSC output voltage V_{SSSC} and the magnitude of the transmission line current I_{line}. A block diagram of the SSSC controller, as implemented in the EMTP simulation, is depicted in Figure 4.7.

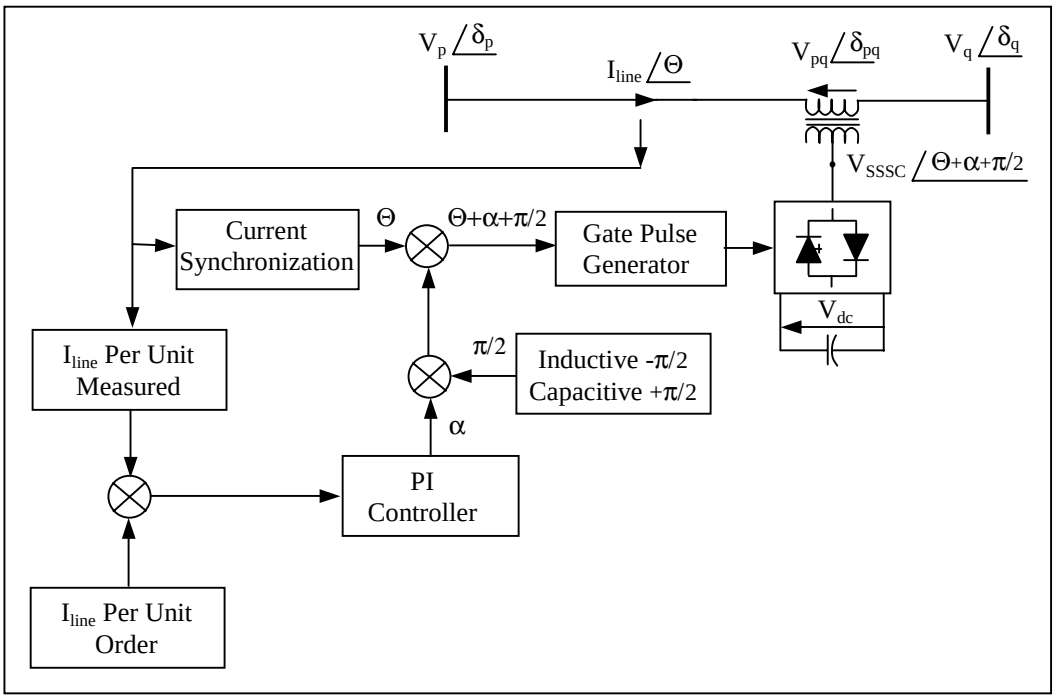


Figure 4.7 – Functional control diagram for the phase-controlled SSSC

The SSSC output voltage $\mathbf{V}_{SSSC}$ is controlled by a simple closed loop; the per unit value of the measured line current is compared with the line current per-unit order and the error of these two values is passed to the PI controller. The output of the PI controller is the angle α, which is added to the synchronizing signal Θ passed to the gate pulse generator by the current synchronization block. To this signal $\Theta+\alpha$, an angle of $-\pi/2$ or $+\pi/2$ has to be added since the SSSC output voltage is lagging or leading the line current

by 90^0 depending on the desired capacitive or inductive operation. The phase shift of the converter output voltage $\mathbf{V}_{SSSC}$ with the respect to the line current $\mathbf{I}_{line}$ will cause the flow of a small amount of real power from or into the converter, thereby causing a change in the dc capacitor voltage, and consequently causing a change in the converter output voltage magnitude.

A PI block controls the transmission line current I_{line}, and is shown in detail in Figure 4.8. The absolute value of reference $I_{lineORD}$ is compared to the measured p.u. value of the transmission line current I_{linePU}, and the amplified difference (error) is passed to a control block that improves the response of the regulator, by changing current rapidly if there is load change. The firing angle α is limited and then multiplied by 0.00833 to convert the angle from radians to seconds.

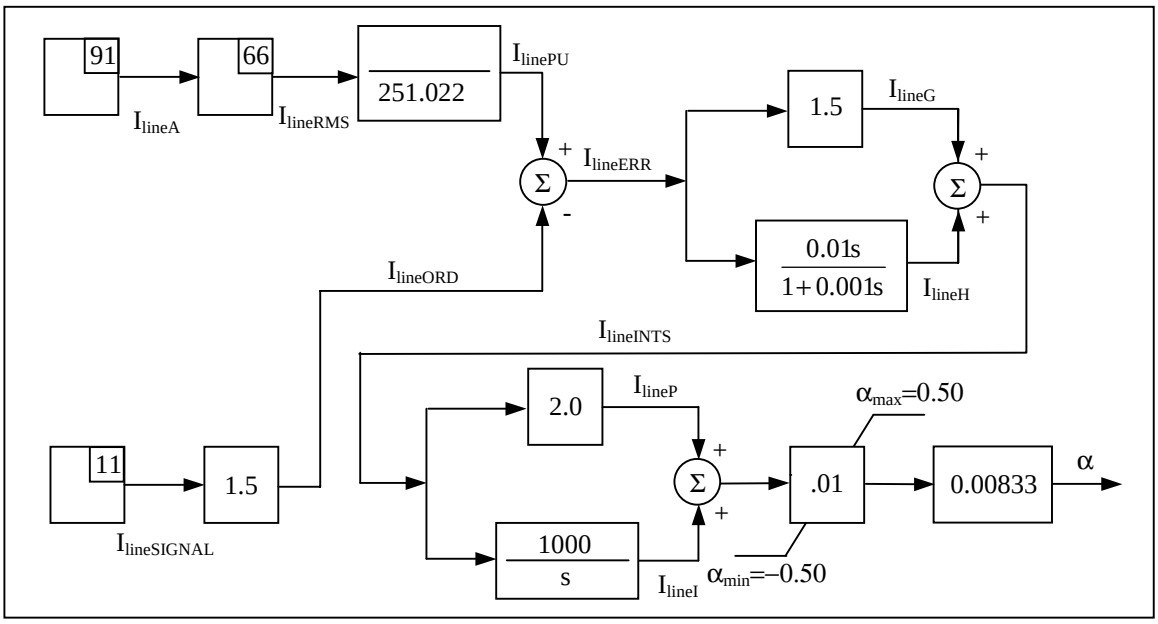


Figure 4.8 – Control block diagram of the SSSC

Additional loops can be added to the control block shown in Figure 4.8, such as for dc voltage and converter output current limitation. The dc voltage protection would monitor the dc terminal voltage so that it is kept between its minimum and maximum values by limiting the control angle α.

The design and operation of circuit breakers take into account the fact that power system equipment, such as power transformers, cables, etc., are usually designed to withstand short-circuit current during at least 30 cycles [59]. However, this is not the case for the SSSC, as the semiconductor devices can be destroyed when the current exceeds the maximum turn-off current value of the switching components. In order to protect the SSSC, the circuit breaker isolation, or diversion, must be correspondingly rapid.

The converter output current is basically the transmission line current and as such cannot be limited, since it is a function of ac system impedance and power flow. To protect the converter switching components, the transmission line is monitored and in a case of short-circuit current, a circuit breaker isolating the converter circuit and switching components from this current would bypass the series transformer. In practice, rapid diversion by, for example, a thyristor-based switch, would precede circuit breaker operation. This electronic switch should be placed on the secondary side of the series transformer to protect the circuit as soon as the overcurrent is sensed.

The proposed SSSC protection strategy can be expected to be costly. To prevent unnecessary operation of the SSSC protection, there are some possible solutions that may reduce the number of the SSSC protection equipment operations [60]. One possibility is to control the overcurrent by suitably controlling the SSSC output voltage, which implies that the SSSC control has to be fast; the disadvantage of this method is the fact that the SSSC output voltage is limited, so it might not be possible to fully control the overcurrent.

4.5.3 PWM Technique

The 70 Mvar, 30 kV SSSC is modeled as a three-phase, PWM-controlled two-level VSC. The SSSC is modeled in detail, based on an ideal representation of the converter valves and diodes. RC parallel snubber circuits are used to reduce EMTP numerical oscillations due to switching, while a series inductance is employed at the converter output to smooth the output current. The series transformer is modeled as an ideal, three-phase, two-winding, Y - Δ connected transformer. The transformer rating is 70 MVA, 30 kV / 6 kV, 14.5 % on the 100 MVA system base. The modeled PWM-controlled SSSC basic circuit is shown in Figure 4.9.

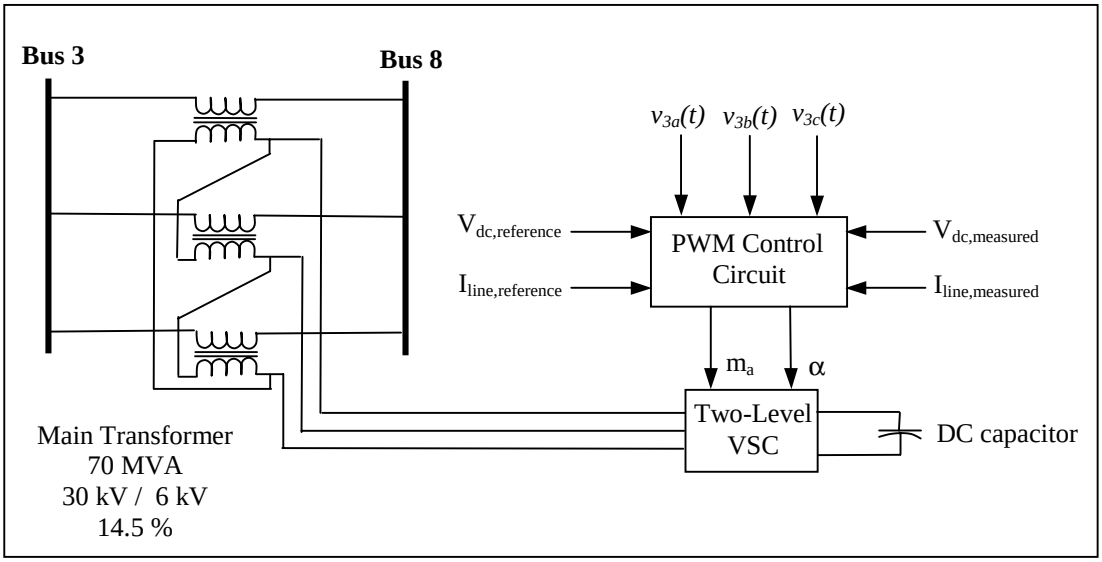


Figure 4.9 – PWM-controlled basic SSSC circuit

The control of the SSSC is achieved by applying SPWM control technique with a small modification. A third harmonic of appropriate amplitude is added to the sinusoidal control waveform to increase the fundamental component of the SSSC output voltage [29]. The frequency modulation ratio m_f =15 is chosen to eliminate the even harmonics and moreover, since 15 is a multiple of 3, to cancel out the most dominant harmonics from the line-to-line output voltages (in the three-phase converters, only the harmonics in the line-to-line voltages are of concern).

The control and triangular waveforms are synchronized with respect to the reference voltage at Bus 3, instead to the transmission line current, which was the case for the phase controlled SSSC. The synchronizing waveforms in this case can be any voltage or current waveform; this should have no influence the controller performance. The SSSC controller uses three reference signals and consequently consists of three major control loops. The reference signals to the controller are the instantaneous three-phase voltage waveforms at Bus 3, the instantaneous transmission line current, and the filtered voltage at the dc terminals. The SSSC control loops provide synchronization with the ac system voltage, maintain the dc capacitor voltage at a constant level and regulate the transmission line current. Figure 4.10 show the functional control diagram, including the three control loops, of the PWM-controlled SSSC.

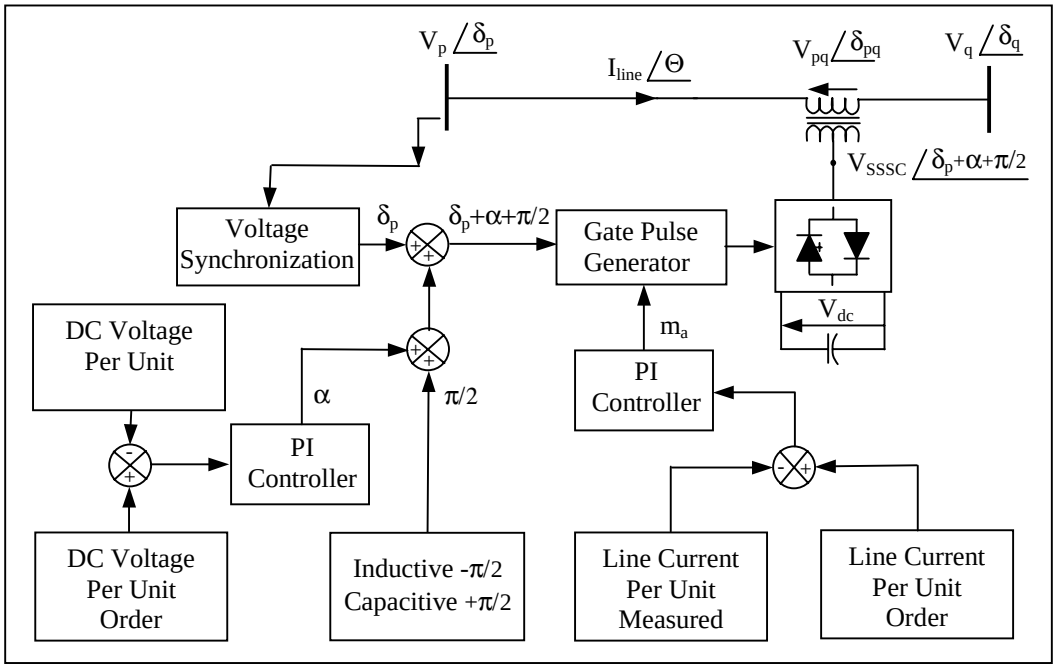


Figure 4.10 – Functional control diagram for the PWM-controlled SSSC

The voltage synchronization block is used to track voltage waveforms, and then, using Fourier analysis, recalculate ideal harmonic-free voltage waveforms. The control is synchronized to the voltage at Bus 3, to which a $+\pi/2$ or $-\pi/2$ phase shift and the output of

the dc voltage regulator are added. The sum of these three phase shifts provides the basic synchronizing signal δ_p.

It is assumed that the current loop is fast enough to force the line current to closely follow changes in the reference current. The dc voltage control loop is not as fast as the line current loop, to prevent possible interactions between these two loops. These two control loops are designed as two independent systems; the real and reactive powers between the SSSC and the ac system are independent and hence can be controlled independently. The objective of the dc voltage control loop shown in Figure 4.11, is to control the real power flow in/out of the SSSC and keep the dc voltage at a reference value. The error of the dc voltage regulation loop varies the phase angle between the fundamental components of the transmission line current and SSSC output voltage, i.e., $P_{SSSC} = V_{SSSC} I_{line} \cos(\delta_p + \alpha \pm \pi/2 - \Theta)$, where the angle $\delta_p - \Theta$ represents the relative phase angle between the system voltage at Bus 3 and the line current. The angle α is the output of dc voltage control loop.

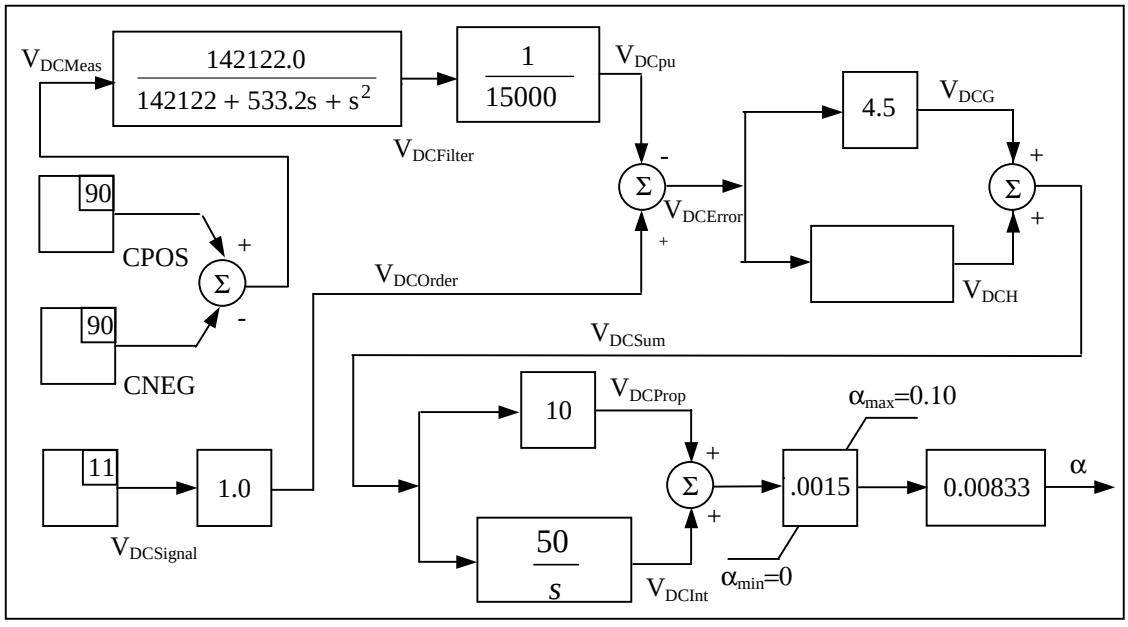


Figure 4.11 – TACS block for dc voltage regulation

The transmission line current control block is shown in detail in Figure 4.12. The absolute value of reference $I_{lineORD}$ is compared to the measured p.u. value of the transmission line current I_{linePU}, and the amplified difference (error) is passed to the sudden response regulator and PI control block. The output of the line current control block is the amplitude modulation signal, which is limited to values between –1.0 and 1.0 to keep the SSSC in the linear control range.

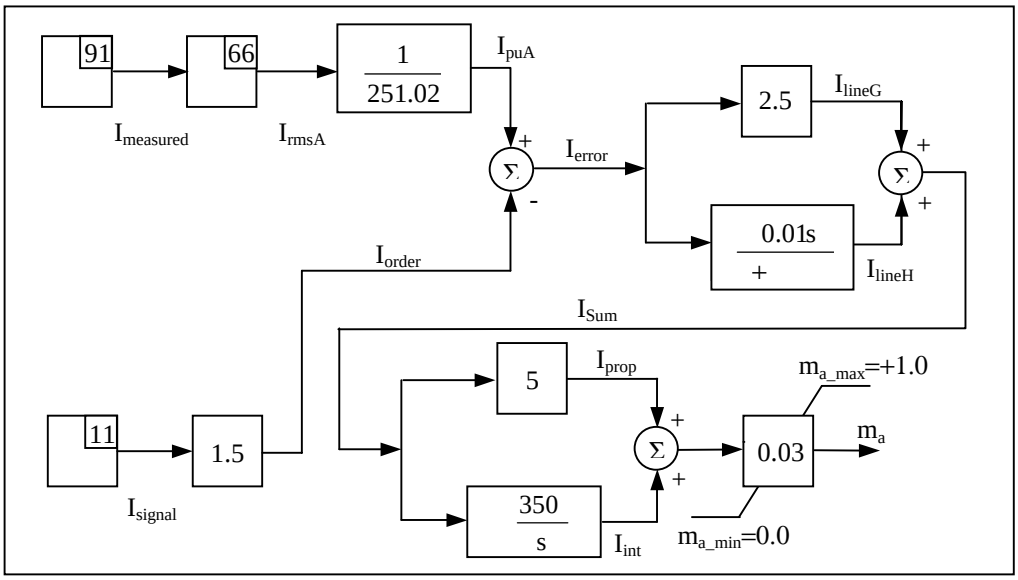


Figure 4.12 – TACS block for p.u. transmission current regulation

4.6 EMTP Time-Domain Simulations

The EMTP results are divided into three sections. Thus, Section 4.6.1 discusses results for the tests system without the SSSC. The results obtained for the test system with phase-controlled SSSC are presented in Section 4.6.2, while Section 4.6.3 discusses the results obtained with the PWM-controlled SSSC. Two kinds of tests were simulated: dynamic changes in load conditions, and a three-phase solid fault applied at Bus 6.

4.6.1 Test System without SSSC (Base Case)

The two current profiles depicted in Figure 4.13 for the test system show the dynamic amplitude variations due to the load changes at times 5 s and 6 s. Due to different total impedance, the total load current is unequally divided between transmission lines Bus 3 - Bus 8 and Bus 3 – Bus 11. The load at Bus 10 is increased in two steps, from 220 MW to 250 MW and finally to 280 MW. Since the passive loads are voltage dependent, the load power demand does not change significantly.

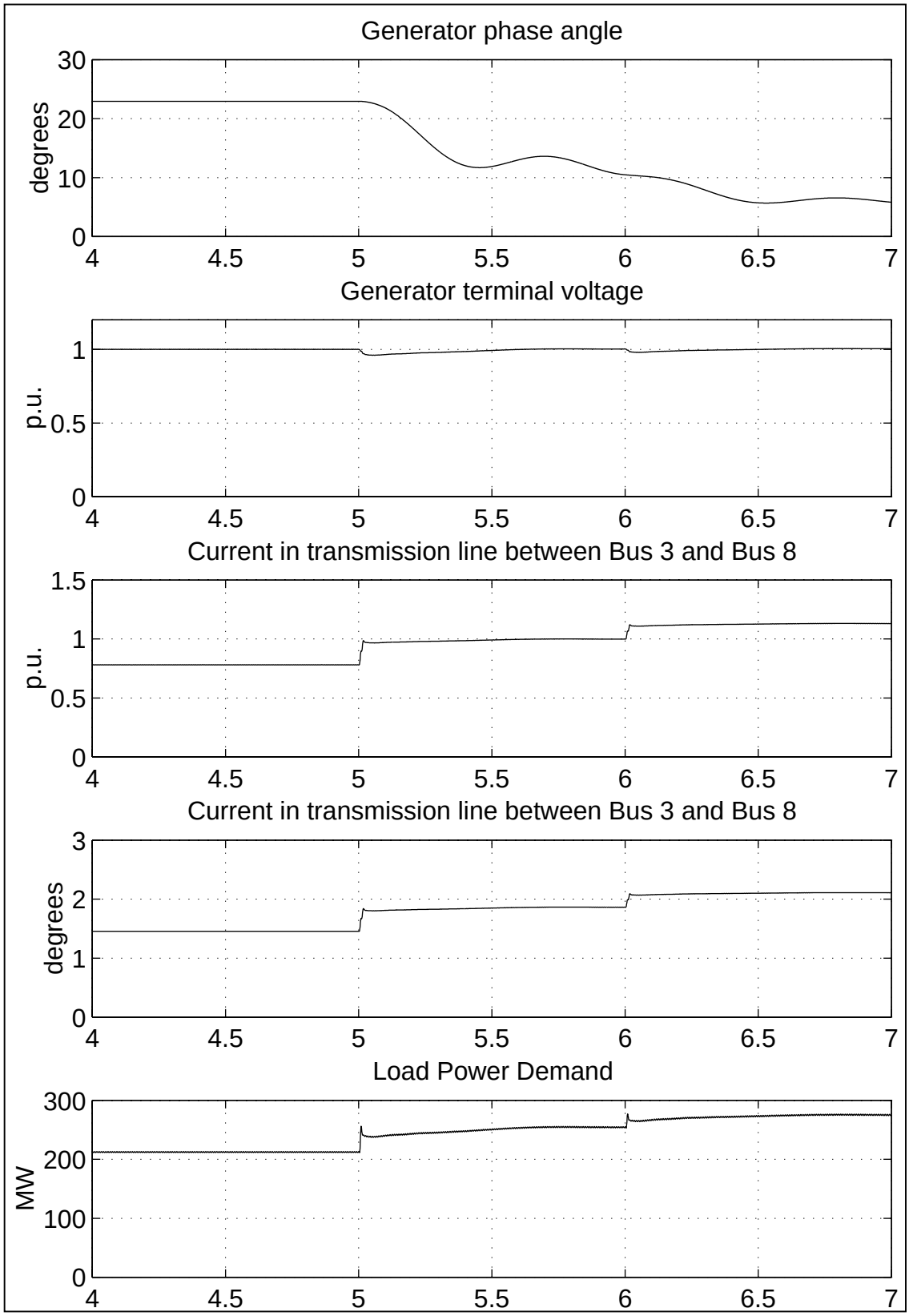


Figure 4.13 – EMTP results for the test system without SSSC

4.6.2 Test System with Phase-controlled SSSC

A 70 Mvar 30 kV SSSC is inserted in the test system between Bus 3 and Bus 11, in series with the transmission line with higher impedance. The objective of the SSSC controller is to regulate the line current to 1.5 p.u. After some EMTP simulations, the SSSC rating is adjusted to 70 Mvar and 30 kV so its rating is sufficient to regulate the transmission line current between 1 p.u. and pre-defined value of 1.5 p.u.

Figure 4.14 and Figure 4.15 show the SSSC response under phase-control to changes in the system load conditions. The figures show an increase in dc voltage and, therefore, an increase in the SSSC output voltage to keep the line current at a reference value of 1.5 p.u. as the load increases. In this case, the load increase affects primarily the current in the uncontrolled parallel transmission line.

These EMTP time-domain simulations verify the successful operation of the designed controller. The SSSC output current reaches its set reference current within 50 ms, as it can be seen from Figure 4.15 where the SSSC output current is shown.

To further test the proposed SSSC controller, a three-phase fault is applied at Bus 6. Figures 4.16 and 4.17 show the SSSC response in this case. The fault is applied at 5.5 s and then isolated from the rest of the system by opening the transmission line Bus 3 – Bus 5 after 150 ms. The fault conditions in the power system reduce the voltage profile at Bus 3 down to 70 % of nominal values; this sudden reduction leads to a decrease in dc voltage, followed by a subsequent decrease in the line current. The fact that the load is simplistically supplied only from one side of the system and that this side was the faulted one, explains why the SSSC was not bypassed by its protection; instead, the SSSC was allowed to ride through the fault and restore the line current to its reference value approximately 50 ms after the fault. In the period immediately after the fault, there is an overcurrent and dc overvoltage due to the delay introduced by the dc voltage filter. The overcurrent was below the pre-set value needed to activate the SSSC protection.

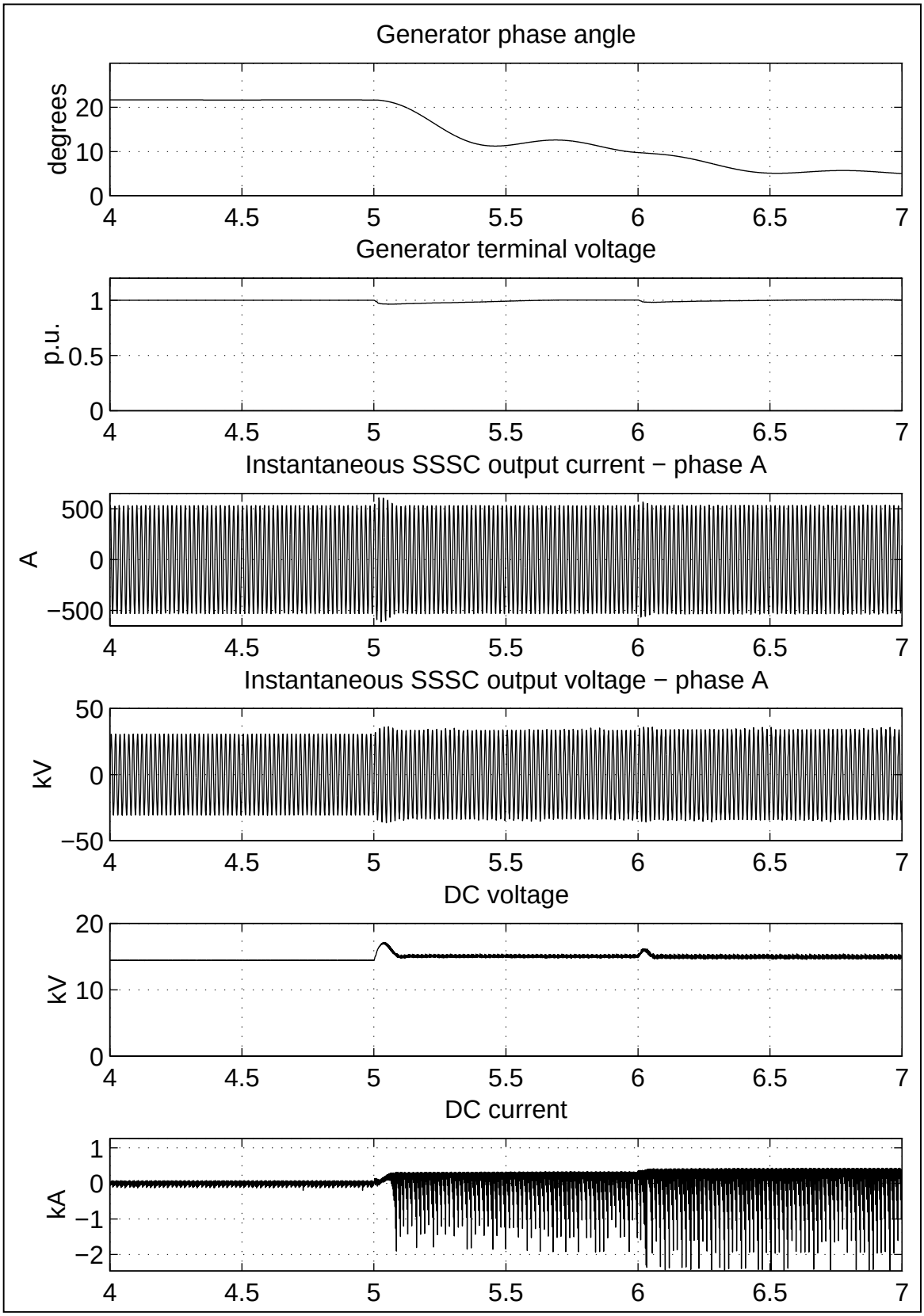


Figure 4.14 – Phase-controlled SSSC response to changes in load conditions

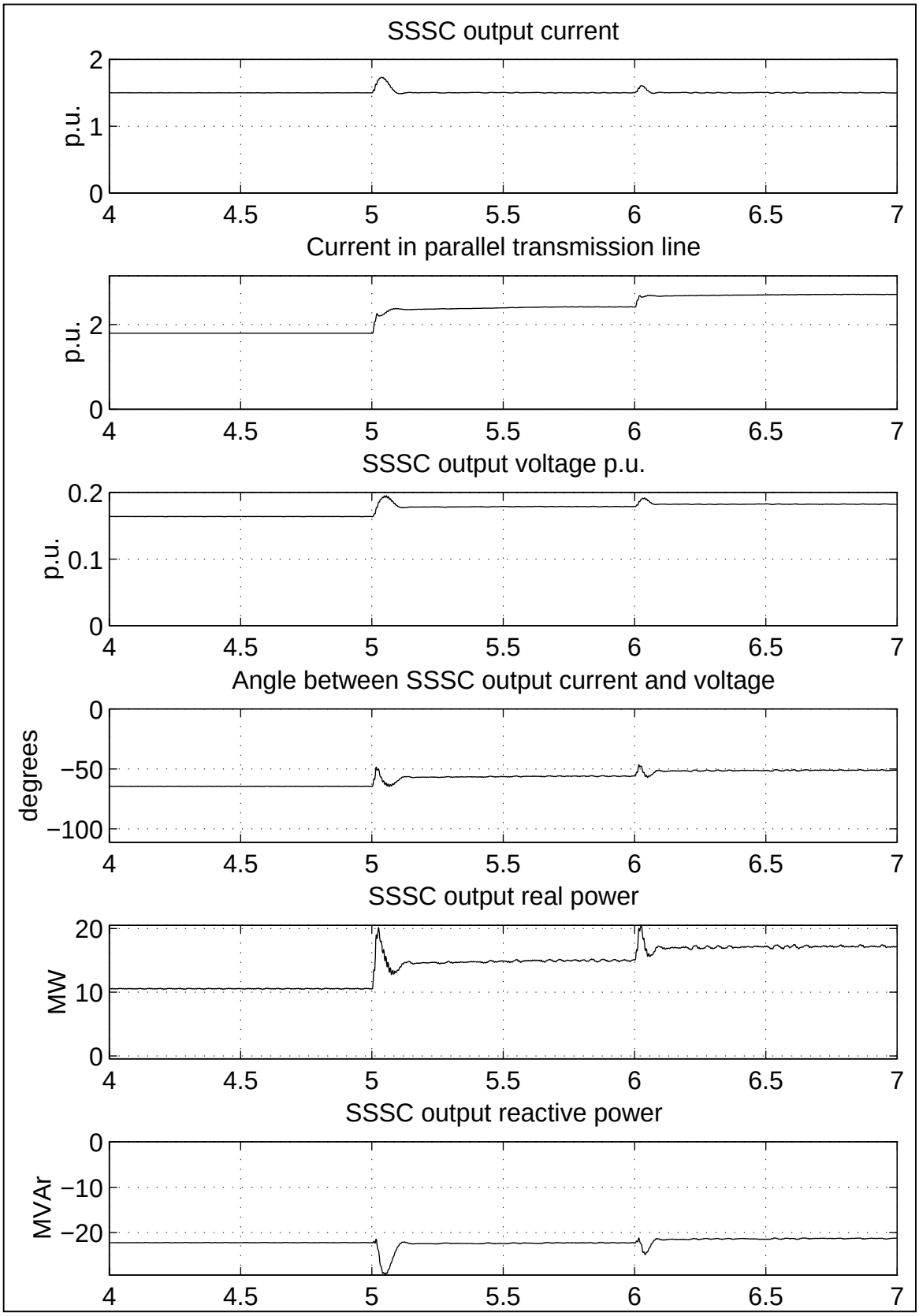


Figure 4.15 – Phase-controlled SSSC response to changes in load conditions

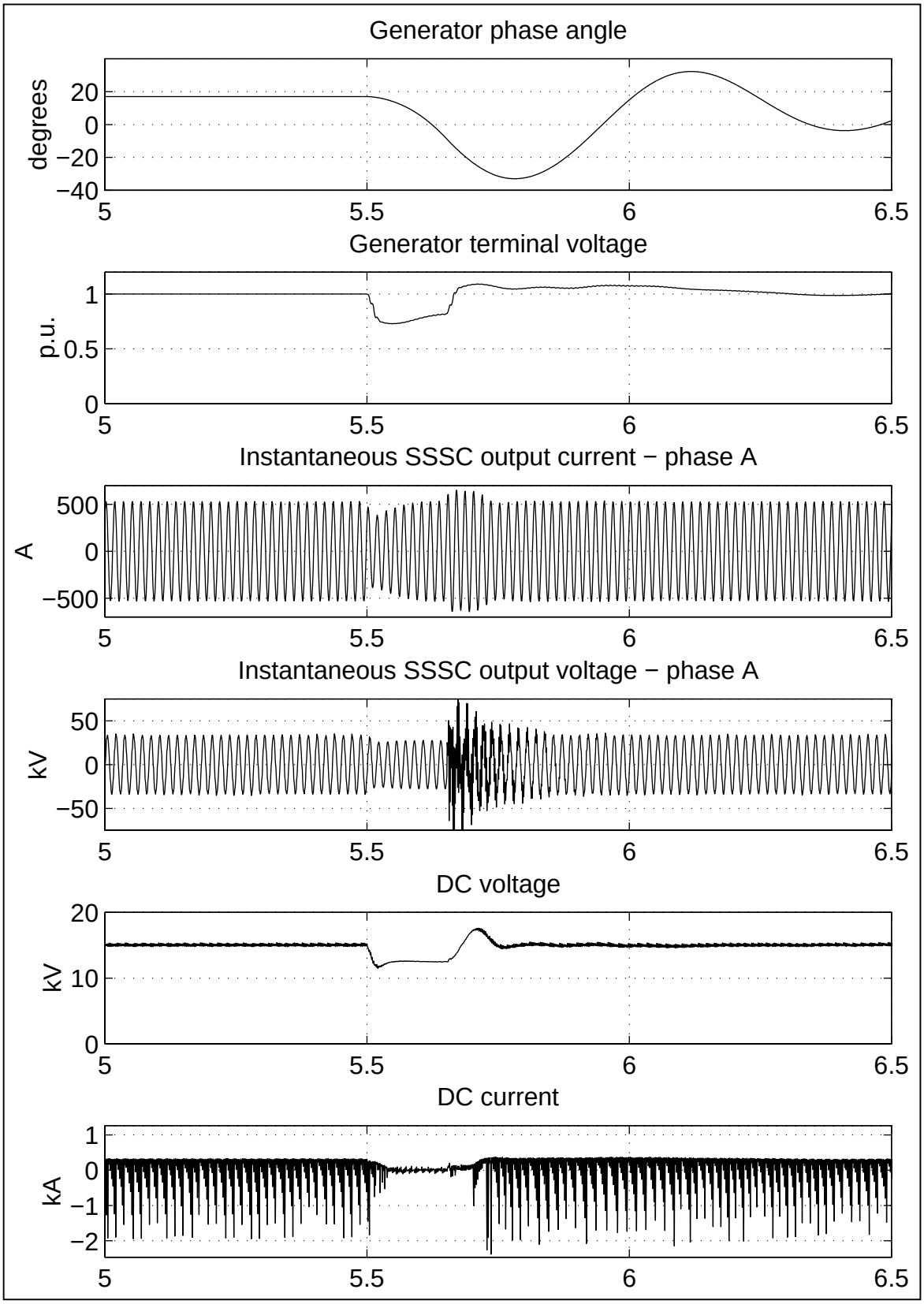


Figure 4.16 – Phase-controlled SSSC response to a three-phase fault

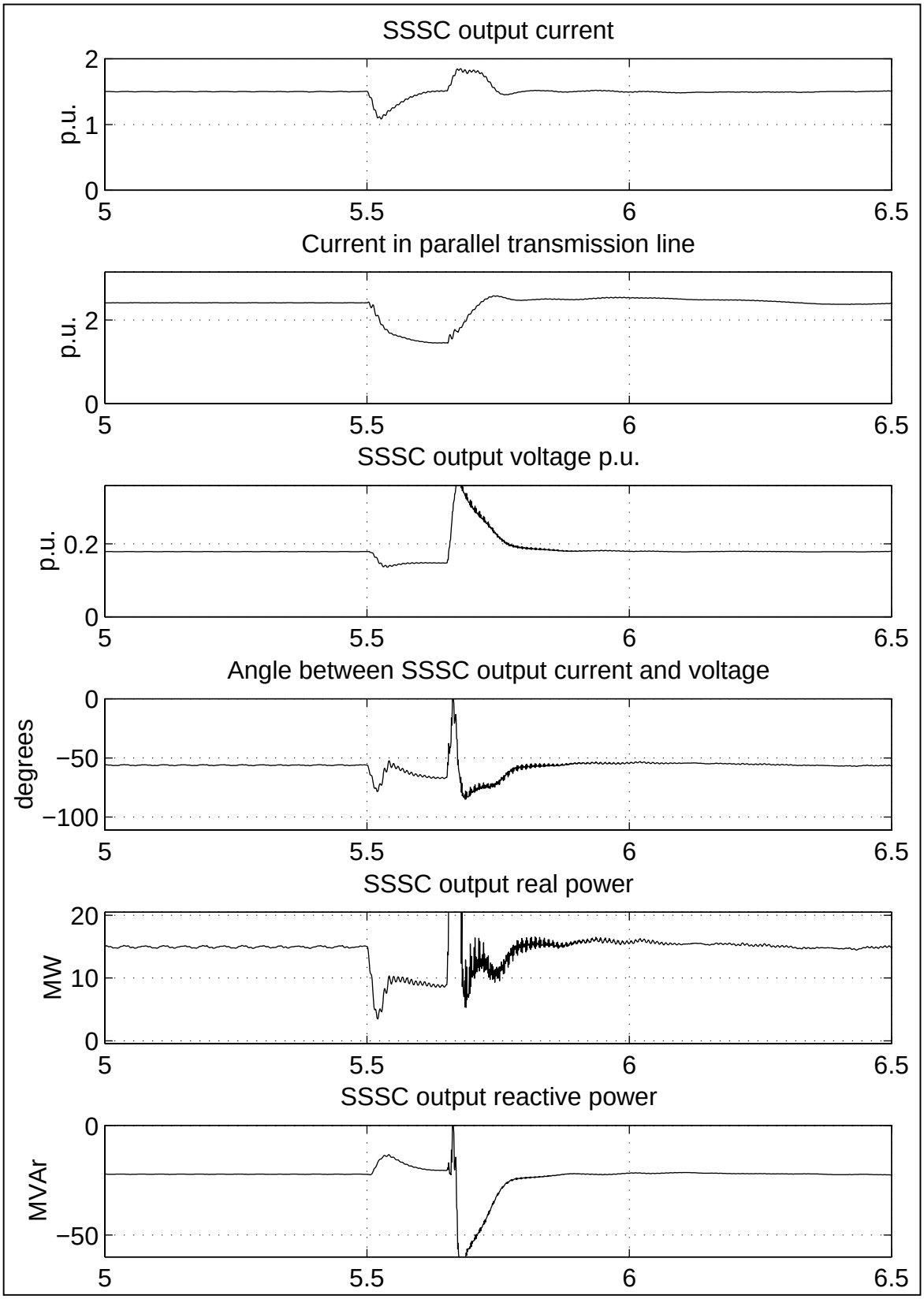


Figure 4.17 – Phase-controlled SSSC response to a three-phase fault

4.6.3 Test System with PWM - SSSC

The same tests performed for the phase-controlled SSSC were repeated for the PWM-controlled SSSC.

Figure 4.18 and Figure 4.219 show the PWM-controlled SSSC response to a change in load conditions. The load at Bus 10 in Figure 4.5 is increased in two steps, at 5 s and 6 s. The capacitor dc voltage is kept constant at 15 kV by the actions of the dc voltage regulator. The increase in load power demand prompts an increase in angle α, which leads to an increase in real power interchange in the SSSC. The amplitude modulation ratio, which is the output of the line current regulator, dynamically adjust the SSSC output voltage magnitude, thus adjusting the series reactive power compensation to keep the line current at 1.5 p.u. as the load conditions change.

The PWM-based controller shows satisfactory results with a time response of approximately 75 ms. The measured rms value of the SSSC output current is rippled due to the high harmonic content, even though a series inductance between the SSSC and series transformer is used to smooth the current. The added series inductance has an influence on the time response of the controller; the waveforms look more damped than in the case of the phase-controlled SSSC.

A three-phase fault, applied at Bus 6 at 5.5 s, is cleared after 150 ms. The SSSC controller response is satisfactory as shown in Figures 4.20 and 4.21; as soon as the fault is applied, the output of dc voltage and line current regulators responded to the fault conditions and depressed system voltages by increasing their values, trying to keep the dc voltage and line current constant at their pre-set values. After 70 ms the fault has been cleared and the SSSC returned to its pre-fault operating point.

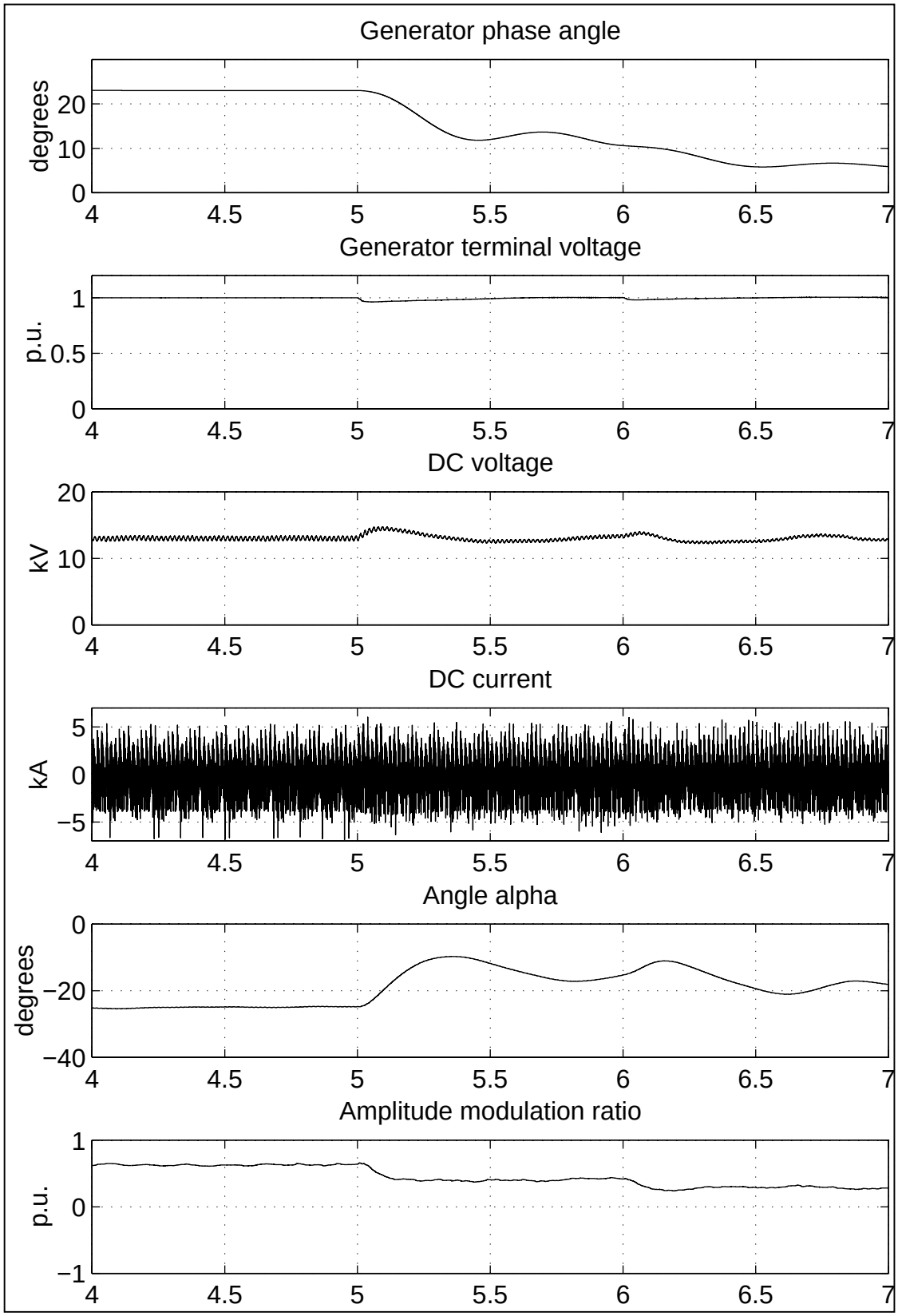


Figure 4.18 – PWM-SSSC response to changes in load conditions

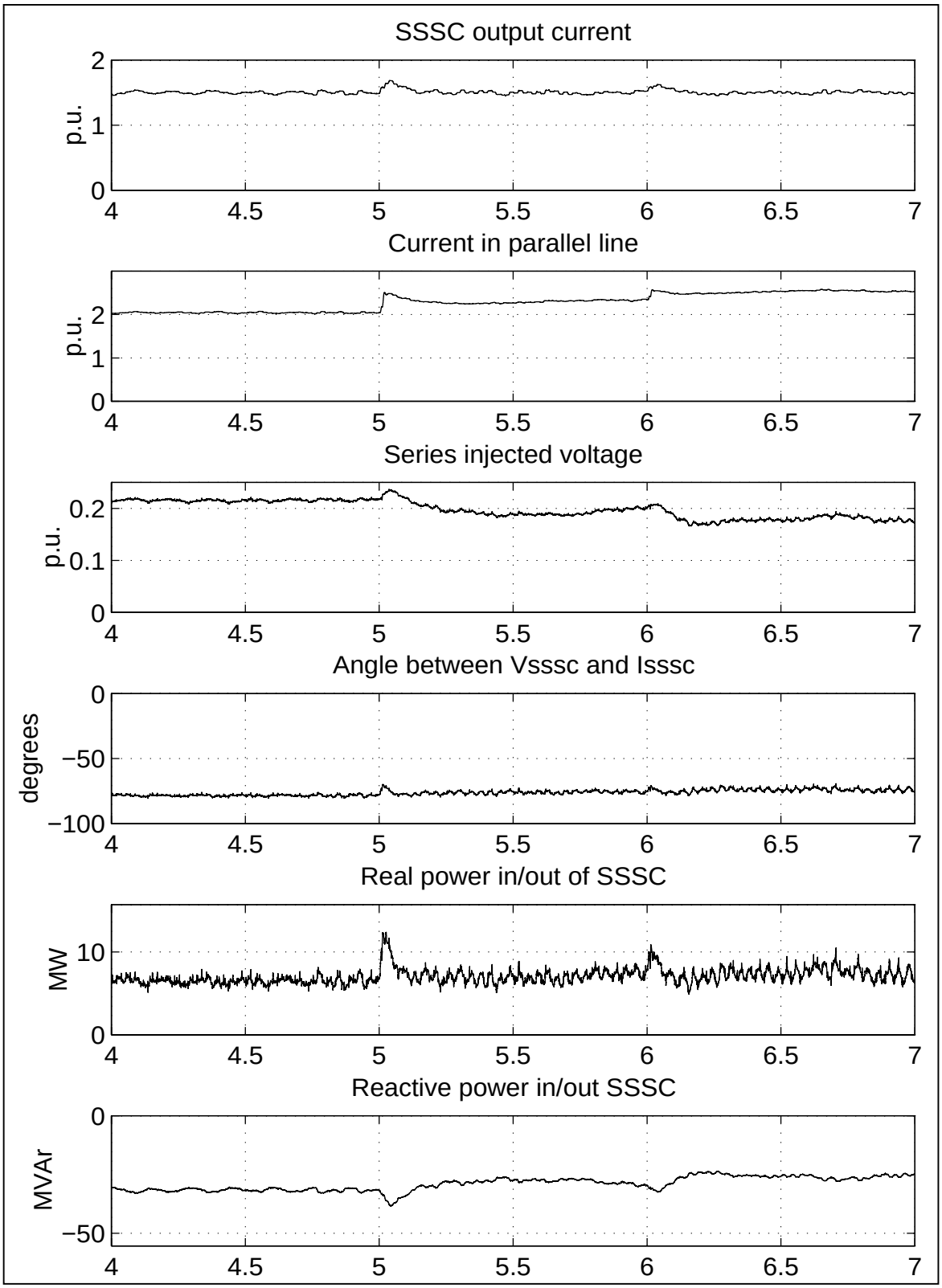


Figure 4.19 – PWM-SSSC response to changes in load conditions

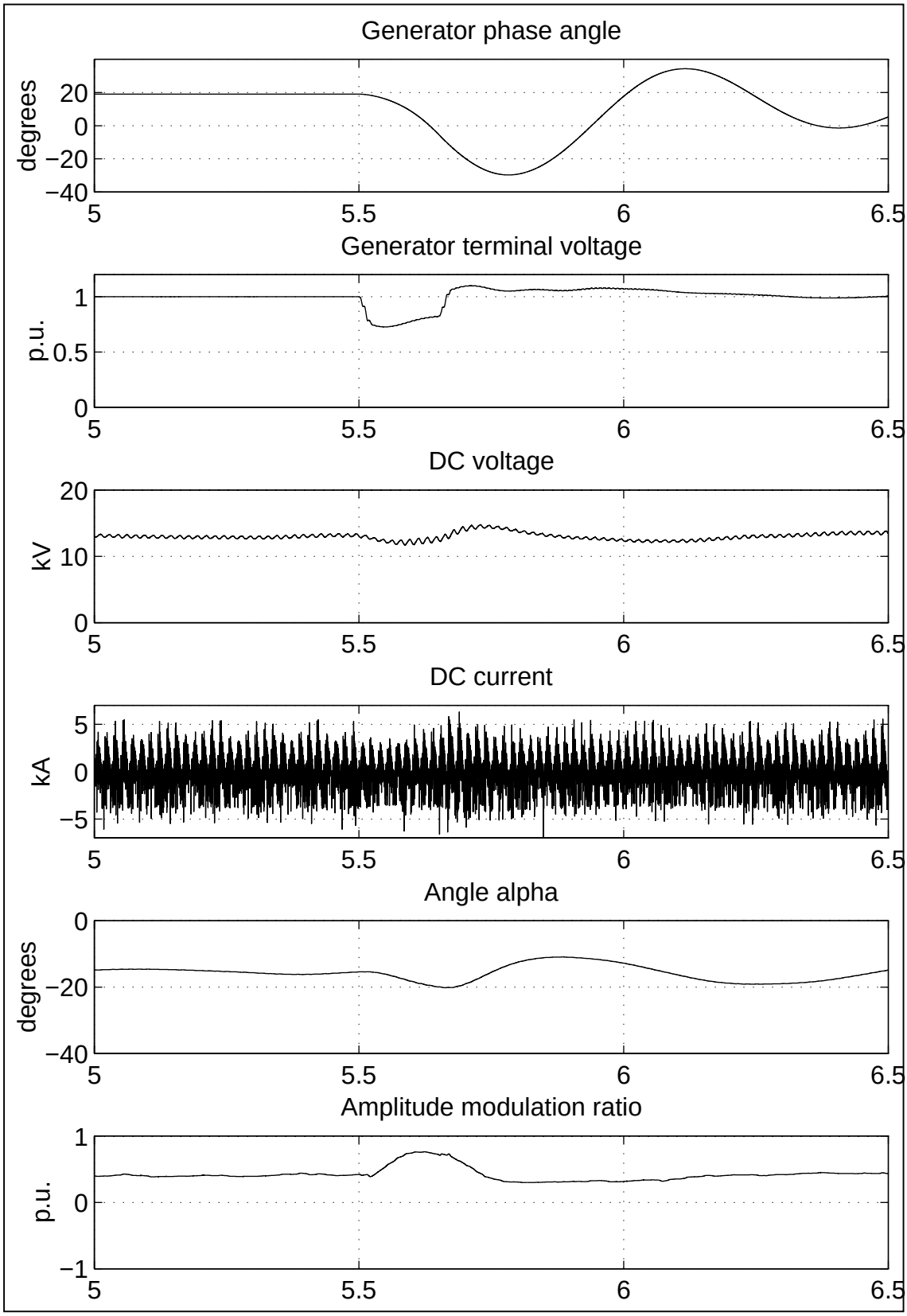


Figure 4.20 – PWM-SSSC response to a three-phase fault

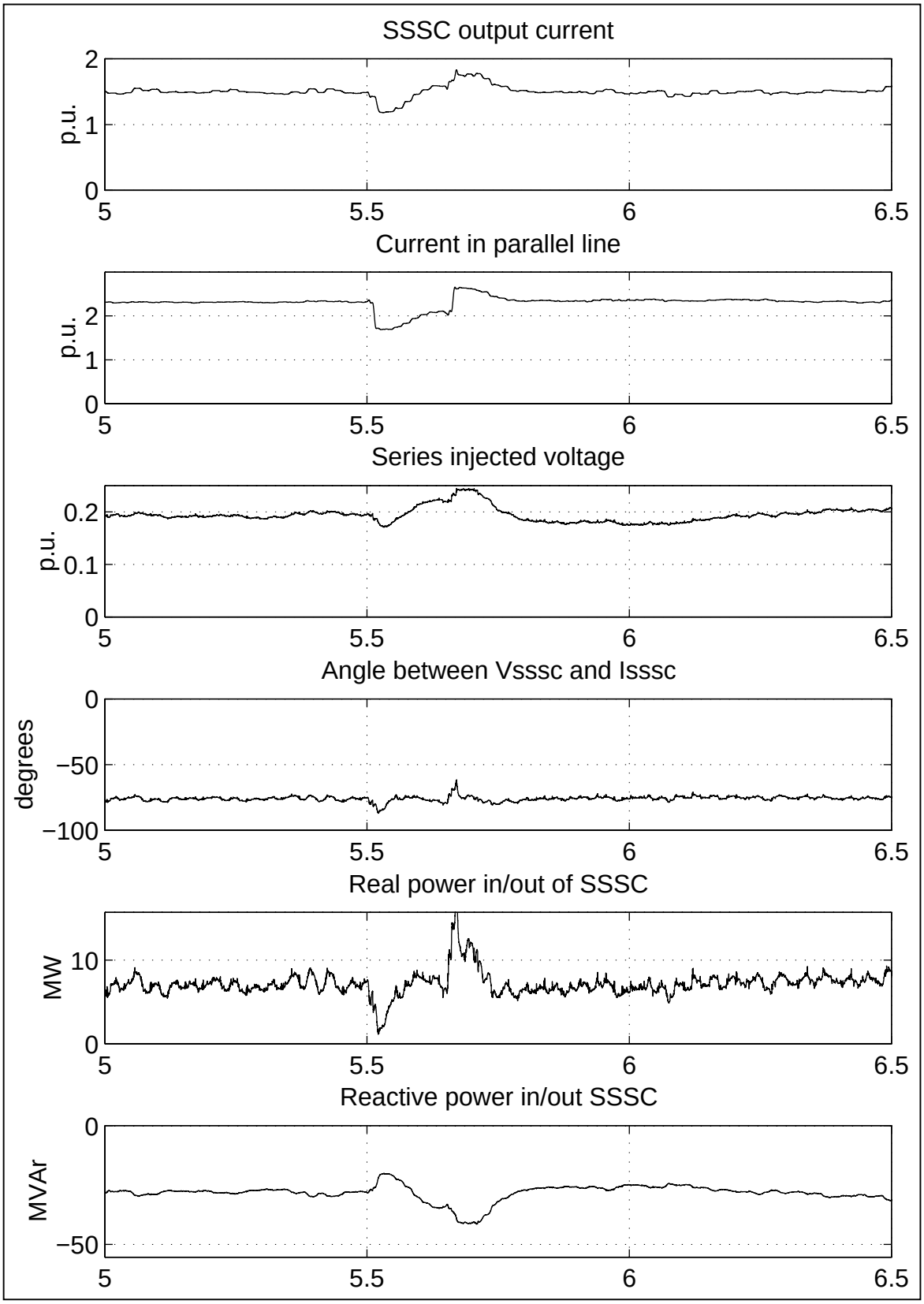


Figure 4.21 – PWM-SSSC response to a three-phase fault

4.7 Summary

The SSSC operating conditions and constraints are compared to the operating condition of a TCSC, showing that the SSSC offers several advantages over a TCSC. However, at the present time the total cost of a SSSC installation is higher than the cost of a TCSC.

Two SSSC control strategies, namely, phase and PWM-based control, are discussed and implemented. Both control strategies are based on novel direct manipulations of the control variables rather then using a d-q decomposition to separate active and reactive components, which is the typical implementation in most of today's controls. Thus, instead of controlling the dc side voltage by means of controlling the d-component of the SSSC output current, the dc side voltage is controlled directly via a phase-shift angle between the transmission line current and the converter output voltage.

The same applies to the transmission line current regulation, i.e., instead of controlling the q-component of the SSSC output current and consequently the series compensation of the transmission line, the transmission line current is controlled directly via the amplitude modulation ratio of the SSSC output voltage. This direct approach in design of the SSSC controls results in fewer regulators and filters in the control loops, improving the controller response.

Comparisons of two implemented control strategies clearly show that the PWM-based and phase controller have both disadvantages and advantages, which makes the design process somewhat complicated. The dc voltage pre-set value in PWM-based controllers has to be carefully selected. As the modulation ratio lies between zero and one, the dc voltage should not be lower than the maximum of the requested SSSC output phase voltage in order to obtain proper control. On the other hand, if the dc side voltage is too high, the rating of both the GTO valves and dc capacitor have to be increased, which means higher installation costs. Not only that, a higher dc side voltage means a lower amplitude modulation ratio, and the lower modulation ratio results in higher

harmonic distortion. Phase control allows the dc voltage to change according to the power system conditions, which is clearly advantageous, but it requires a more complicated controller and special and costly series transformers.

Chapter 5.

UNIFIED POWER FLOW CONTROLLER
UPFC

5.1 Introduction

The basic design, operating principles and control blocks of the UPFC are explained in this chapter together with the EMTP detailed model of the controller. The 230 kV test system is a realistic power system and shows the UPFC operation in practical system conditions. The presented detailed model properly represents the controller control and operating limits, which can be considered an advanced and novel model. The developed model will be of interest for practical control and protection circuit design.

For the UPFC control circuit design, the shunt and series converter control systems are treated completely separately, as indicated in section 5.3. The shunt converter control blocks use direct manipulation of the input variables, while for the series converter control circuit design, d-q transformations were necessary due to non-linear relationships between the output variables. The UPFC proposed control system is designed to directly control voltage at the receiving end of UPFC-controlled transmission line, instead of indirectly controlling this variable through reactive power control. The modification is validated and justified through appropriate mathematical models as shown in section 5.6.2.

This chapter also discusses in detail some of the existing UPFC controls that have been proposed in the literature, as well as proposing and justifying some variations of these controls, such as receiving-end voltage control and power/frequency oscillation damping control. Three different control schemes for the series converter are implemented in the EMTP and tested in the detailed UPFC model. The results obtained for a realistic test system are used to compare the different control strategies.

5.2 Basic Operating Principles

This chapter is concerned with the UPFC controller discussed in [11, 18, 19, 20, 21, 42], where two synchronous VSCs employed in combination are used for dynamic compensation and real time control of voltage and power flow in transmission systems. DC terminals of both converters are connected to a common dc capacitor. The basic three-phase UPFC scheme is shown in Figure 5.1. Figure 5.1 shows that if the series branch is disconnected, the parallel branch comprised of a dc capacitor, VSC-1 and a shunt connected transformer corresponds to a STATCOM. Since the STATCOM can generate or absorb only reactive power, the STATCOM output current is in quadrature with the terminal voltage.

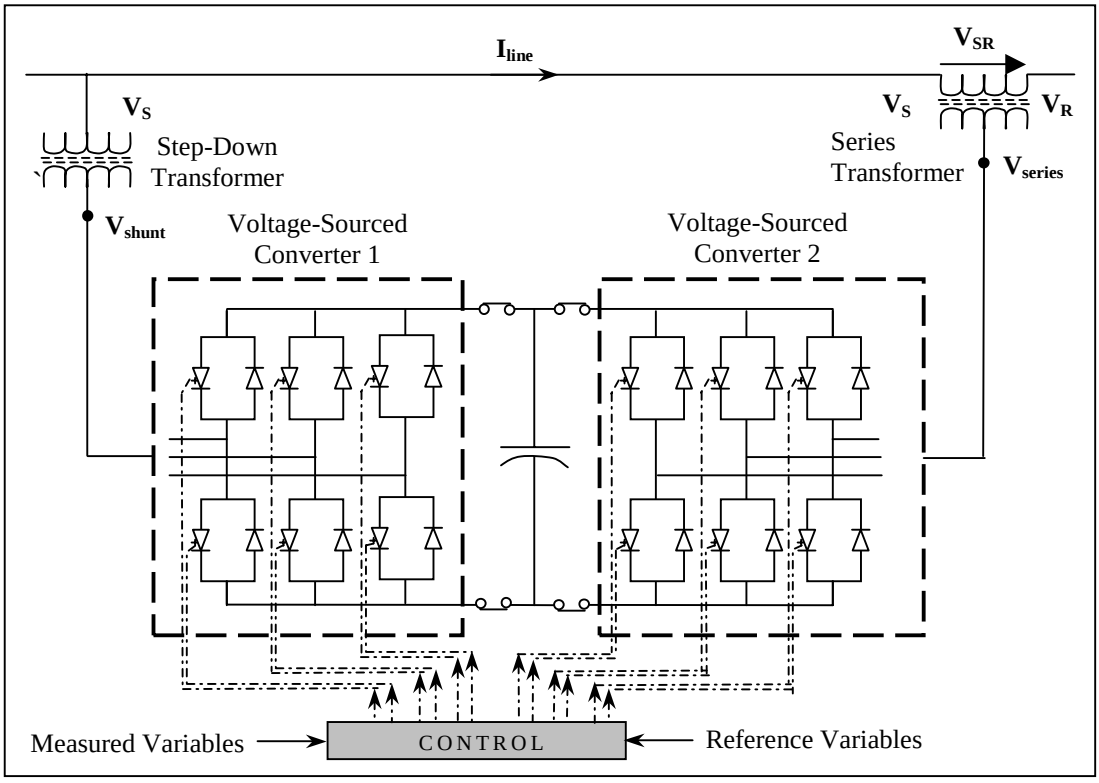


Figure 5.1 – Functional model of UPFC

If the parallel branch is disconnected, the series branch comprised of a dc capacitor, VSC-2 and a series injected transformer corresponds to a SSSC. The SSSC acts as a voltage source injected in series to the transmission line through the series transformer; the current flowing through the VSC is the transmission line current, and it is a function of the transmitted electric power and the impedance of the line. The injected voltage $\mathbf{V}_{SR}$ is in quadrature with the transmission line current $\mathbf{I}_{line}$ with the magnitude being controlled independently of the line current. Hence, the two branches of the UPFC can generate or absorb the reactive power independent of each other.

If the two VSCs are operating at the same time, the shunt and series branches of the UPFC can basically function as an ideal ac to ac converter in which the real power can flow in either direction through the dc link and between the ac terminals of the two converters. The real power can be transferred from VSC-1 to VSC-2 and vice versa, and hence it is possible to introduce positive or negative phase shifts between voltages $\mathbf{V}_S$ and $\mathbf{V}_R$. The series injected voltage $\mathbf{V}_{SR}$ can have any phase shift with respect to the terminal voltage $\mathbf{V}_S$. Therefore, the operating area of the UPFC becomes the circle limited with a radius defined by the maximum magnitude of V_{SR}, i.e., $V_{SR,max}$.

The VSC-2 is used to generate the voltage $\mathbf{V}_{SR}$ at fundamental frequency, variable magnitude $0 \le V_{SR} \le V_{SR,max}$ and phase shift $0 \le \beta \le 2\pi$. The harmonic content in the voltage $\mathbf{V}_{SR}$ depends on the design and control of the VSC. This voltage is added in series to the transmission line and directly to the terminal voltage $\mathbf{V}_S$ by the series connected coupling transformer. The transmission line current passes through the series transformer, and in the process exchanges real and reactive power with the VSC-2. This implies that the VSC-2 has to be able to deliver and absorb both real and reactive power.

The shunt-connected branch associated with VSC-1 is used primarily to provide the real power demanded by VSC-2 through the common dc link terminal. Also, since VSC-1 can generate or absorb reactive power independently of the real power, it can be used to regulate the terminal voltage $\mathbf{V}_S$; thus, VSC-1 regulates the voltage at the input terminals of the UPFC.

Another important role of the shunt UPFC branch is a direct regulation of the dc capacitor voltage, and consequently an indirect regulation of the real power required by the series UPFC branch. The amount of real power required by the series converter plus the circuit losses have to be supplied by the shunt converter. Real power flow from the series converter to the shunt converter is possible and in some cases desired, in this case, the series converter would supply the required real power plus the losses to the shunt converter.

5.3 Limits and Practical Rating of the UPFC Equipment

The UPFC's rating and hence, the amount of the real and reactive power that can be exchanged with the power system are determined by ratings of its shunt and series converters. The UPFC rating is basically a sum of the shunt and series converter ratings. As the possible UPFC role and performance depend on its power rating, it is important to distinguish between the functional control capabilities and the related rating requirements. For example, a UPFC that has as its primary role the control of power flow will certainly have a different rating than a UPFC used for power oscillation damping.

The power rating of a converter is derived from the product of the maximum continuous operating voltage and maximum continuous operating current. For VSC, the maximum continuous operating current is determined by the maximum current turn-off capability of the semiconductor switch. The series converter maximum voltage is determined based on the function that the UPFC is designed to perform. It could be power flow control in the transmission line or power oscillation damping. The maximum current is usually taken to be the thermal line current limit, which basically implies that the converter switches have to be designed to withstand that level of current to be compatible with the line.

The shunt converter has two functions: one is to supply real power to the series converter and the other one is bus voltage control. The lowest continuous shunt

converter rating is determined by the maximum real power exchanged between the series and the ac system, which is typically 20 to 50 % of the total power rating of the series converter [19]. The maximum continuous rating should take into account the amount of reactive power needed for voltage control at the point of connection with the ac system.

The UPFC protection strategy can be divided into the protection of the shunt converter and the protection of the series converter. The constraints imposed on the series converter operation are the series injected voltage magnitude and the transmission line current through the series VSC. The series voltage magnitude is limited by the fact that the dc capacitor voltage has to be limited between pre-specified minimum and maximum values. Thus, the dc bus voltage V_{dc} should not exceed the voltage rating of the dc capacitor; to prevent overvoltages, in most cases, arresters or fast switch-operated dc resistors connected in parallel with the dc capacitor can be used to keep the voltage V_{dc} below certain levels. On the other hand, to allow continuous and proper semiconductor valve operation, the dc voltage has to be kept above certain level; this minimum limit is quite low and is not a serious issue in the normal operating regime.

The maximum series converter output voltage is also limited by the fact that voltage stresses on the transmission line may become too high at some operating conditions [21]. As it can be seen in Figure 5.2, the UPFC ability to raise or lower the magnitude of voltage $\mathbf{V_R}$ (the UPFC output bus) depends on the series converter output voltage.

It is possible to observe that there is an upper and a lower limit locus for V_R; the shaded area in Figure 5.2 represents the achievable and allowable range for V_R. It is noticeable that the voltage drop or rise across the series transformer reactance X_{tr} has to be taken into account. This voltage depends on the line current and, therefore, can be significant for a highly loaded transmission line.

Limits imposed on the transmission line current based on the series converter should be specified according to transient and continuous overload characteristics of the power semiconductors. However, the transmission line current is a function of the voltages and

the phase angles at the sending and receiving ends as well as the transmission line impedance, and hence depends on hard to predict system conditions; this implies that the current cannot be limited by the series converter. In case of a line fault, the series converter has to be protected from fault currents. The easiest way to protect the series converter is to divert the fault current away from the converter by a fast bypass switch that should operate as soon as the overcurrent is sensed.

Similar protection strategies need to be implemented for the shunt converter. The shunt current has to be continuously measured to prevent damage to the converter circuit, particularly to the semiconductor switches. To match thermal rating, the limit on the overcurrent is time dependent. Two overcurrent limits can be distinguished: continuous and transient limits. The continuos limit is applied in the case of currents that are not so large to trigger immediate operation of the transient current protection; thus, there is a time delay on this protection that depends on the semiconductor characteristics as well as on the associated cooling system.

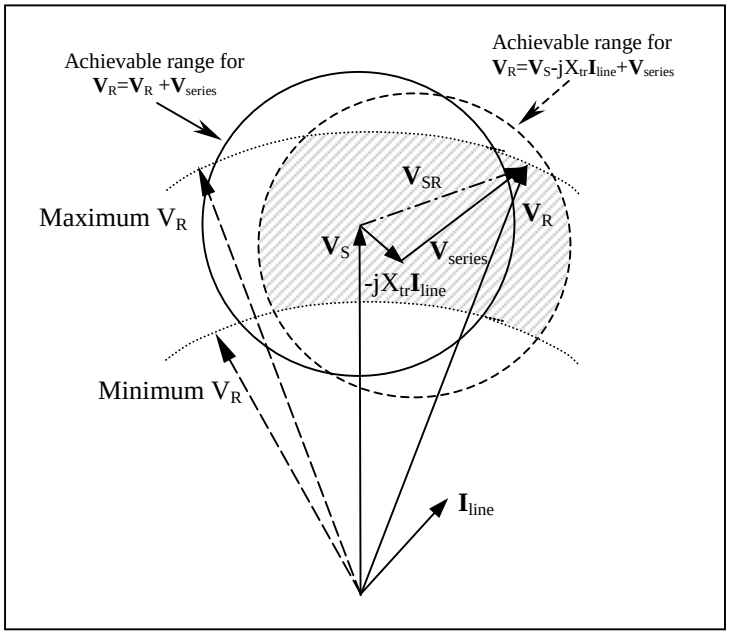


Figure 5.2 – Practical constraints for the UPFC of Figure 5.1 [42]

5.4 UPFC Control System

An efficient control system is essential in order to draw maximum benefit from the inherent capabilities of the UPFC. Due to the unique characteristics of the UPFC to independently control active and reactive power, the previously proposed control for phase control in two-level VSCs in Chapters 3 and 4 is inadequate. Thus, the dc capacitor voltage was controlled and independent control of real and reactive powers was not possible.

To accommodate the need for independent real and reactive power control in a UPFC, a three-level converter control or some extension of the PWM technique used in two-level converters has to be implemented. The installation and special features of a three-level based UPFC are given in [61, 62]. The UPFC equipment used in this case is based on two identical converters, each composed of multiple high power GTO valve structures feeding an intermediate transformer. The converter output voltage is a 48-pulse sinusoid produced by appropriate switching of the GTO valves between positive, zero and negative dc capacitor voltages. The UPFC control calculates the trigger pulses for each GTO valve individually according to the control input references.

The PWM yields also an appropriate sinusoid through fast switching of the semiconductor valves. The harmonic content in the output voltage waveform depends on the number of notches per cycle. Currently, this technique has not found favor for transmission systems due to high switching losses if standard GTOs are used, but with recent developments in high power semiconductors, this technique is becoming more competitive. It has the advantage of allowing independent and easy control of active and reactive powers, without the need for expensive and complex transformer arrangements used in the multi-converter approach.

In general, a UPFC controller can be broken down into three major parts: master, middle and converter control [63]. The authors in [42] suggest a division into internal and functional operational control. The internal or master control is external to the UPFC

and involves execution of functions required at the system operating level; at this level the two converters control active and reactive power or possibly damp power oscillations. The middle part deals with the protection of the converters; the protection control is internal to the converter and provides gating signals to the converter valves according to the orders given by the master control.

A vector-control approach originally developed for the STATCOM can be adapted to the UPFC control [45]. This vector-control uses a d-q transformation of the sinusoidal input signals to facilitate the decoupled control of the real and reactive current and voltage components. This decomposition is very appealing for the UPFC control, as the real and reactive power control has to be independent. In [58], the d-q transformation is used to build a control structure with a predictive control and a pre-control signal for dc voltage control. The vector-control approach is also used to control real power through the transmission line while regulating magnitudes of the voltages at its two ports [64].

Of various control strategies, in most cases, the UPFC would likely be used to control its sending or point of connection bus voltage magnitude by locally generating or absorbing the reactive power, while controlling power flows in the transmission line by regulating the magnitude and phase angle of the series injected voltage. These control modes are known as Automatic Voltage Control Mode for the shunt converter, and Automatic Power Flow Control Mode for the series converter [21].

Special caution should be used to ensure that the Automatic Power Flow Control Mode does not impede natural power oscillations in the line after a fault if that is beneficial for recovery. To prevent instability and even improve the stability of the system, it is possible to add some additional control functions such as the damping of the post-fault power oscillations [48, 64].

There are also other possibilities for the optimum selection of UPFC control strategies. For example, it is possible to use the shunt converter to control the shunt reactive current with respect to a requested reference, engaging the shunt converter into

so-called VAR Control Mode [21]. The series converter could be also used to inject into the line a constant voltage of requested magnitude and phase angle [66]; this is known as Voltage Injection Mode. There are some other control strategies for the series converter such as Line Impedance Control Mode and Phase Angle Control Mode.

5.5 Test System Description

The same test system of Chapter 4 shown in Figure 5.3 is used again to study the performance of the UPFC. After some EMTP simulations and the careful assessment of the UPFC role in the sample test system, it was determined that the UPFC could be used to increase the power flow in the lower ac parallel line (Buses 3-11) from 100 MW to up to 300 MW. The UPFC is also used to damp power oscillations caused by a test fault at Bus 6.

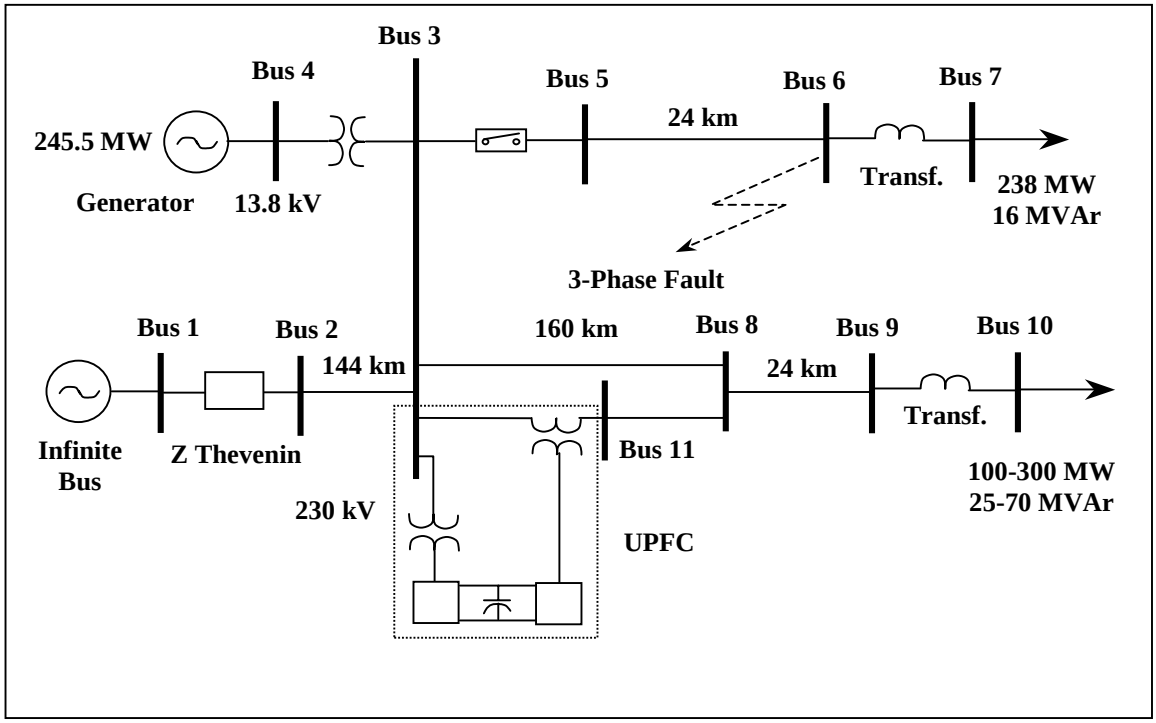


Figure 5.3 – One-line diagram of the test system

If the UPFC is considered to have two identical VSCs, the rating of the shunt and series converters as well as of the accompanying transformers should be calculated considering the full load line current of 773 A needed to supply a load of 300 MW, 70 Mvar at nominal voltage.

The series inserted voltage is assumed to be 1/3 of the power system voltage rating, i.e., the maximum magnitude of the series converter line to line voltage would be 76.67 kV, neglecting the voltage drop on the series transformer leakage reactance X_{se}. This voltage is chosen so that the maximum desired line current can be obtained, as well as to sufficiently damp the power oscillations.

Based on the calculations, the rating of the series converter and transformer should be $\sqrt{3} \cdot 76.67\text{kV} \cdot 0.773\text{kA} \approx 100\text{MVA}$. For this simulation, however, a 200 MVA rating was used, which would significantly increase the equipment costs but the UPFC would be able to support the current associated with the full thermal transmission line capabilities. This is sometimes a requirement of the system operators, as additional protection in case of UPFC protection failure.

The rating of the shunt converter is defined in a similar manner. Thus, to accomplish the desired power flow objectives, the anticipated maximum real power exchange between the two converters is 80 MW, although the full power transfer of 200 MW should be possible. Some reactive power is necessary to support the transmission line voltage at the required level; however, the summation of real and reactive power should not exceed 200 MVA. This implies that the UPFC protection should also monitor the shunt current.

The UPFC simulated in this chapter consists of two VSCs with a Sinusoidal Pulse Width Modulation (SPWM) control. Switching the controllable switches at a sufficiently high frequency generates the desired ac output voltage by converting the dc voltage on the dc capacitor to an ac output voltage. The frequency modulation ratio that specifies the harmonic content in the output voltage waveform is kept at a moderate level of 15 to

make the study realistic. The PWM reference signal is the result of the summation of two sinusoidal waveforms, one is a fundamental frequency whereas the second one is a third harmonic waveform, such that the fundamental component of the converter output voltage is increased [36]. Even and triple harmonics are not present in the output voltage waveform, and 13^{th}, 17^{th}, 29^{th} and 31^{st} harmonics are reduced using passive filters placed on the converter side of transformer.

The UPFC shunt and series transformers are modelled as banks of three single-phase two winding transformers with no saturation. The transformer ratings are calculated according to the permissible maximum shunt current, maximum shunt voltage, maximum series (transmission line) current, and maximum series injected voltage. Thus, the transformer ratings are basically identical to the converter ratings, i.e., the shunt and series transformers are rated 200 MVA each.

5.6 Implemented Control System

In theory, the UPFC should be treated as a multivariable control problem with four inputs (magnitude and phase angle of the shunt and series converter output voltages) and four outputs (real and reactive output powers of the shunt and series converters). However, in practice, it is possible to treat the shunt and series converter control separately in order to simplify the design as well as the implementation, because the coupling of the converters is mainly achieved through the common dc capacitor. The dc capacitor dynamics are dominated by the shunt converter control and do not involve the series converter control, as the series converter voltage rating is significantly smaller than that of the shunt converter. This implies that the series converter real power exchange on the dc terminals is much smaller the corresponding exchange in the shunt converter.

Compared with several possible schemes for the series converter, shunt converter control is fairly straightforward. In this thesis, it is used to control the sending-end bus voltage magnitude by locally generating and absorbing reactive power, as is already a fairly established practice. The series converter directly controls real and reactive line

power by regulating the magnitude and phase angle of the series injected voltage through its real and reactive components. It is possible, according to equations (1.13) and (1.14), to control the real power flow by controlling the series injected phase angle, while the reactive power flow can be controlled through the series injected voltage magnitude. This control scheme is feasible but would perform poorly due the nonlinear relationships shown in equations (1.13) and (1.14).

The adopted general control scheme is shown in Figure 5.4. The series converter controls the active and reactive powers on the transmission line by adjusting the amplitude and phase angle of the series injected voltage. The shunt converter controls the dc voltage and the bus voltage at the shunt converter transformer (referred to here as the sending-end bus voltage).

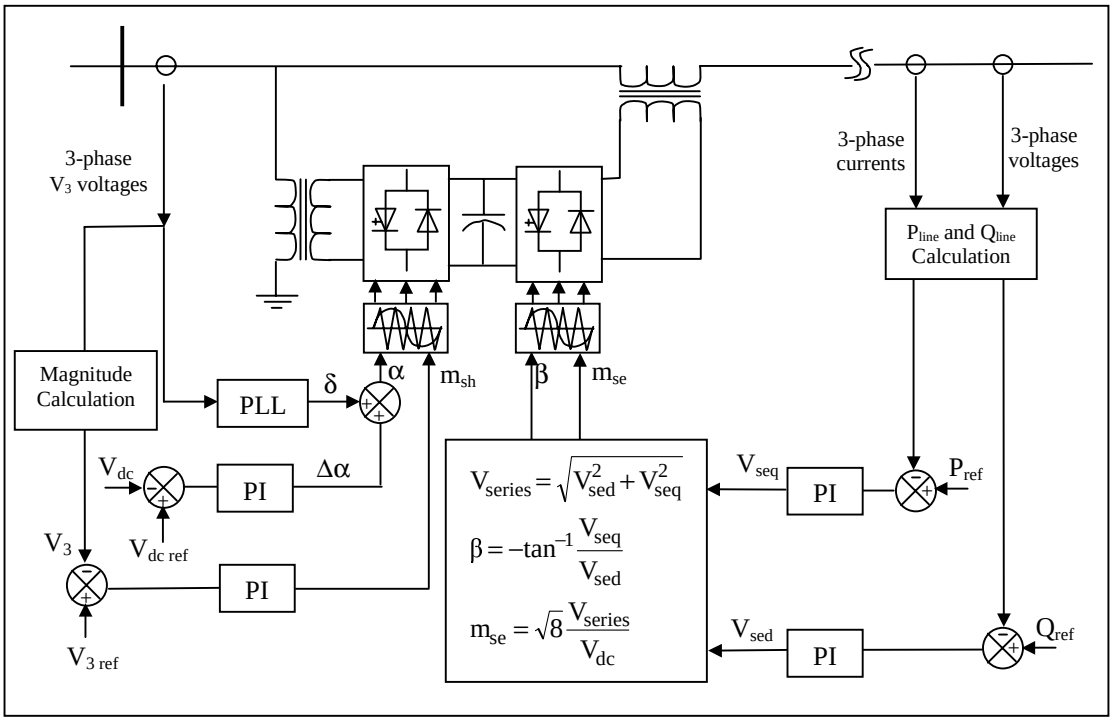


Figure 5.4 – General block diagram of the UPFC control system

5.6.1 Shunt Converter Controls

The shunt converter has two duties, namely, to control the voltage magnitude at the sending-end bus (Bus $\mathbf{V_3}$ in Figure 5.3) by locally generating or absorbing reactive power, and to supply or absorb real power at the dc terminals as demanded by the series converter. It is possible to achieve real power balance between the series and shunt converter by directly controlling the dc voltage V_{dc}, as any excess or deficit of real power will tend to increase or decrease the dc voltage, respectively. These basic ideas are used here to define the simple and effective shunt converter controller depicted in Figure 5.5. This control scheme is basically the same as the one proposed in [65] as a STATCOM control.

The shunt converter ac and dc voltages are controlled by using two separate PI controllers, taking advantage of the UPFC ability to independently control reactive and real power. The basic principle of real power flow being directly affected by changes in phase angles, while reactive power flow being directly associated with voltage magnitudes, is used here to design the UPFC control.

The reactive power flow in and out of the shunt converter is controlled by changes in the bus voltage magnitudes, which is achieved by controlling the shunt converter output voltage V_{sh}. The voltage V_{sh} is controlled through the changes in the amplitude modulation ratio m_{sh}, as the output voltage magnitude is directly proportional to m_{sh} according to the following equation:

$$V_{sh} = \frac{1}{2\sqrt{2}} m_{sh} V_{dc} \tag{5.1}$$

The dc voltage, on the other hand, is controlled by a PI controller that directly varies the phase angle α of the converter output voltage with respect to the UPFC sending-end voltage $V_3 \angle \delta$. Thus, when $\alpha < \delta$ ($\Delta\alpha < 0$), the shunt converter output voltage lags the sending-end bus voltage and hence the dc capacitor charges, whereas when $\alpha > \delta$ ($\Delta\alpha >$

0), the converter ac voltage leads the sending-end bus voltage and hence the dc capacitor discharges.

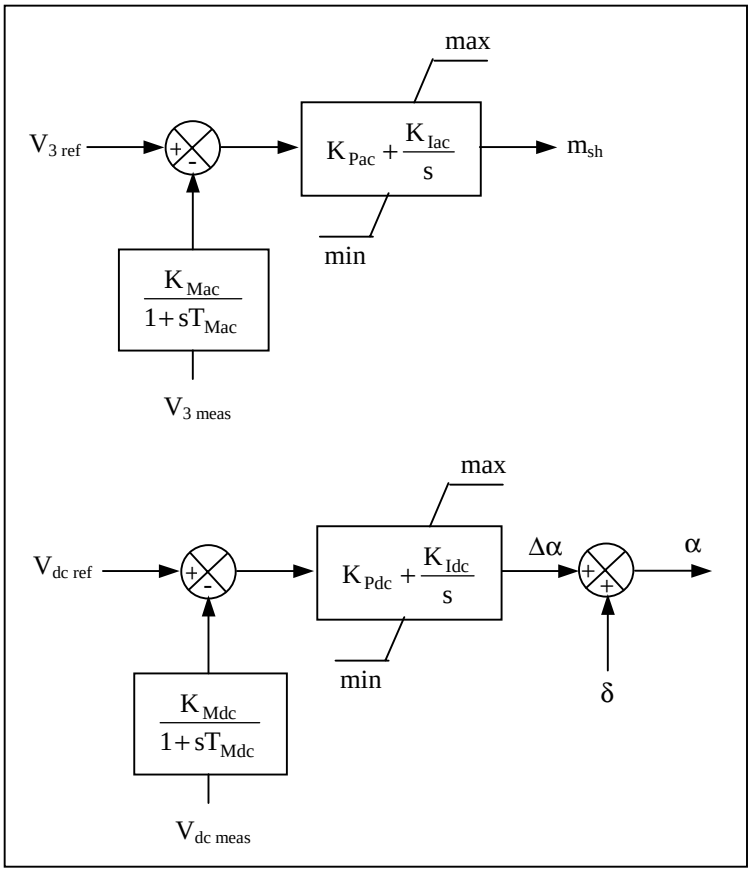


Figure 5.5 – Shunt converter control of the UPFC

The amplitude modulation ratio is limited to $0 \leq m_{sh} \leq 1$ to avoid over-modulation forcing the shunt converter operation within the linear range. This also limits the shunt converter output voltage, limiting as well the shunt converter output current and the associated reactive power flow. These limits were placed on the PI controller responsible for the control of the sending-end bus voltage magnitude. Limits on the phase angle difference $\Delta\alpha$ are also imposed on the PI controller used for the dc voltage control; these basically impose limits on the real power transfer capability of the controller.

5.6.2 Series Converter Controls

Two different control schemes for the series converter were implemented and tested to evaluate their performance. A scheme to control the real power flow on the transmission line and voltage magnitude at the receiving-end bus is discussed as Case A; another control scheme for controlling the real and reactive power flows on the transmission line is Case B. Finally, Case C uses an additional control block for power oscillation damping.

Case A. Power and Voltage Control

The first control scheme is a modified version of a control proposed in [67]. The objective of this novel series converter controller is to control the receiving-end bus voltage V_8, as opposed to the typical control of the reactive power flow on the line Q_{line}. In conjunction with the control of the receiving-end voltage magnitude, the series converter also controls the real power flow on the line P_{line}.

Usually, only three conductors connect the UPFC converters to the ac system, which forces the output currents not to have any zero sequence component; according to this, it can be assumed that the three-phase system can be transformed into a synchronously rotating orthogonal system. The system reference voltage is chosen to be the sending-end voltage v_3, i.e., $v_{3d} = v_3$ and $v_{3q} = 0$. This control is based also on the assumptions that the series converter output voltage is sinusoidal and that the sending-end bus voltage is kept constant by the actions of the shunt converter, i.e., $\Delta v_{3d} = 0$. Finally, it is also assumed that the dc capacitor voltage is kept constant by the actions of the shunt converter, i.e., $\Delta v_{dc} = 0$, and, therefore, it is completely omitted from the system equations.

Under all these assumptions, the system equations for a small disturbance signal Δx can be reduced to the following equations, as shown in Appendix B (the equations are given in per-unit):

$$\frac{d\Delta i'_{sed}}{dt} = -\frac{\omega_B R'_L}{L_L}\Delta i'_{sed} + \omega\Delta i'_{seq} + \frac{\omega_B}{L'_L}\left(-\Delta v'_{sed} - \Delta v'_{8d}\right) \tag{5.2}$$

$$\frac{d\Delta i'_{seq}}{dt} = \omega\Delta i'_{sed} - \frac{\omega_B R'_L}{L_L}\Delta i'_{seq} + \frac{\omega_B}{L'_L}\left(-\Delta v'_{seq} - \Delta v'_{8q}\right) \tag{5.3}$$

where R'_L and L'_L represent the transmission line total resistance and inductance; $\Delta i'_{se} = \sqrt{\Delta i'^2_{sed} + \Delta i'^2_{seq}}$ is the transmission line current; $\Delta v'_8 = \sqrt{\Delta v'^2_{8d} + \Delta v'^2_{8q}}$ and $\Delta v'_{se} = \sqrt{\Delta v'^2_{sed} + \Delta v'^2_{seq}}$ are the receiving-end bus and series converter output voltages, respectively; and ω and ω_s are the system frequency and it base value, respectively.

The three-phase real and reactive power in the transmission line at the receiving-end are given by the following equations:

$$p'_{line} = \frac{3}{2}\left(v'_{8d} \cdot i'_{sed} + v'_{8q} \cdot i'_{seq}\right) \tag{5.4}$$

$$q'_{line} = \frac{3}{2}\left(v'_{8q} \cdot i'_{sed} - v'_{8d} \cdot i'_{seq}\right) \tag{5.5}$$

The variations in the real and reactive powers due to the changes in input signals can then be expressed as:

$$\Delta p'_{line} = \frac{3}{2}\left(\Delta v'_{8d} \cdot i'_{sedo} + v'_{8do} \cdot \Delta i'_{sed} + \Delta v'_{8q} \cdot i'_{seqo} + v'_{8qo} \cdot \Delta i'_{seq}\right) \tag{5.6}$$

$$\Delta q'_{line} = \frac{3}{2}\left(\Delta v'_{8q} \cdot i'_{sedo} + v'_{8qo} \cdot \Delta i'_{sed} - \Delta v'_{8d} \cdot i'_{seqo} - v'_{8do} \cdot \Delta i'_{seq}\right) \qquad (5.7)$$

where $i'_{seo} = \sqrt{i'^2_{sedo} + i'^2_{seqo}}$ and $v'_{8o} = \sqrt{v'^2_{8do} + v'^2_{8qo}}$ represent steady-state values for the transmission line current and the receiving-end bus voltage, respectively.

Hence, the state-space model for the series converter in the UPFC can be described as follows:

$$\Delta\dot{\mathbf{x}} = \mathbf{A} \cdot \Delta\mathbf{x} + \mathbf{B} \cdot \Delta\mathbf{u} \qquad (5.8)$$

$$\Delta\mathbf{y} = \mathbf{C} \cdot \Delta\mathbf{x} + \mathbf{D} \cdot \Delta\mathbf{u} \qquad (5.9)$$

where the vectors of the state and input variables are:

$$\Delta\mathbf{x} = \left[\Delta i'_{sed}\ \Delta i'_{seq}\right]^T \qquad (5.10)$$

$$\Delta\mathbf{u} = \left[\Delta v'_{sed} \quad \Delta v'_{seq} \quad \Delta v'_{8d} \quad \Delta v'_{8q}\right]^T \qquad (5.11)$$

$$\Delta\mathbf{y} = \left[\Delta p'_{line} \quad \Delta q'_{line}\right]^T \qquad (5.12)$$

the state or plant matrix **A** is

$$\mathbf{A} = \begin{bmatrix} -\dfrac{\omega_B R'_L}{L'_L} & \omega \\ -\omega & -\dfrac{\omega_B R'_L}{L'_L} \end{bmatrix} \qquad (5.13)$$

the input matrix **B** is

$$\mathbf{B} = \begin{bmatrix} -\frac{\omega_B}{L'_L} & 0 & -\frac{\omega_B}{L'_L} & 0 \\ 0 & -\frac{\omega_B}{L'_L} & 0 & -\frac{\omega_B}{L'_L} \end{bmatrix} \tag{5.14}$$

and the output and feedforward matrices are given, respectively, by:

$$\mathbf{C} = \begin{bmatrix} v'_{8do} & v'_{8qo} \\ v'_{8qo} & -v'_{8do} \end{bmatrix} \tag{5.15}$$

$$\mathbf{D} = \begin{bmatrix} 0 & 0 & i'_{sedo} & i'_{seqo} \\ 0 & 0 & -i'_{seqo} & i'_{sedo} \end{bmatrix} \tag{5.16}$$

The system transfer function can be readily obtained from the state-space model described in equation (5.17) as follows:

$$\begin{bmatrix} \Delta p'_{line} \\ \Delta q'_{line} \end{bmatrix} = \left[\mathbf{C} \cdot (s\mathbf{I} - \mathbf{A})^{-1} \cdot \mathbf{B} + \mathbf{D}\right] \cdot \begin{bmatrix} \Delta v'_{sed} \\ \Delta v'_{seq} \\ \Delta v'_{8d} \\ \Delta v'_{8q} \end{bmatrix} = \begin{bmatrix} g_{11}(s) & g_{12}(s) & g_{13}(s) & g_{14}(s) \\ g_{21}(s) & g_{22}(s) & g_{23}(s) & g_{24}(s) \end{bmatrix} \cdot \begin{bmatrix} \Delta v'_{sed} \\ \Delta v'_{seq} \\ \Delta v'_{8d} \\ \Delta v'_{8q} \end{bmatrix}$$

where

$$g_{11}(s) = \frac{\Delta p'_{line}}{\Delta v'_{sed}},\ g_{12}(s) = \frac{\Delta p'_{line}}{\Delta v'_{seq}},\ g_{13}(s) = \frac{\Delta p'_{line}}{\Delta v'_{8d}},\ g_{11}(s) = \frac{\Delta p'_{line}}{\Delta v'_{8q}} \tag{5.18}$$

$$g_{21}(s) = \frac{\Delta q'_{line}}{\Delta v'_{sed}},\ g_{22}(s) = \frac{\Delta q'_{line}}{\Delta v'_{seq}},\ g_{23}(s) = \frac{\Delta q'_{line}}{\Delta v'_{8d}},\ g_{24}(s) = \frac{\Delta q'_{line}}{\Delta v'_{8q}} \tag{5.19}$$

Now, if the transmission line is assumed to be feeding a large system (see Appendix B), one can assume that $v_8^{'}$ is approximately constant, i.e., $\Delta v_{8d}^{'} = \Delta v_{8q}^{'} = 0$. In this case, equation (5.17) becomes:

$$\begin{bmatrix} \Delta p_{line}^{'} \\ \Delta q_{line}^{'} \end{bmatrix} = \begin{bmatrix} g_{11}(s) & g_{12}(s) \\ g_{21}(s) & g_{22}(s) \end{bmatrix} \cdot \begin{bmatrix} \Delta v_{sed}^{'} \\ \Delta v_{seq}^{'} \end{bmatrix} \tag{5.20}$$

Equation (5.20) shows that two control schemes can be developed: one control scheme would employ the direct coupling terms $\Delta p_{line}^{'} / \Delta v_{sed}^{'}$ and $\Delta q_{line}^{'} / \Delta v_{seq}^{'}$, while the other one would make use of the cross-coupling terms $\Delta p_{line}^{'} / \Delta v_{seq}^{'}$ and $\Delta q_{line}^{'} / \Delta v_{sed}^{'}$. These two control schemes can result in very similar closed-loop performances as has been shown in [44]. However, these controls do not perform well and are difficult to tune properly when the receiving-end voltage of the transmission line varies significantly with the power flow, as is the case for the test system used here. In this case, a coupled control like the one described in the next Case B is more appropriate.

Figure 5.6 shows the control scheme used for the series converter. Both control objectives, i.e., P_{line} and Q_{line} and P_{line} and V_8 have been implemented and tested in the EMTP. The EMTP tests show that both reactive power and terminal voltage controllers have a similar performance, as the voltage v_8 is closely associated with the reactive power flow in the line.

The outputs of the PI controllers are d and q components of the series injected voltage V_{se}, i.e., V_{sed} and V_{seq}, respectively. The magnitude of the series voltage can be calculated by the following equation:

$$V_{se} = \sqrt{V_{sed}^2 + V_{seq}^2} \tag{5.21}$$

The amplitude modulation ratio is:

$$m_{se} = \sqrt{8}\,\frac{V_{se}}{V_{dc}} \tag{5.22}$$

The phase angle of the series injected voltage with respect to the reference waveform, i.e., the sending end voltage v_8, is given as follows:

$$\beta = -\tan^{-1}\frac{V_{seq}}{V_{sed}} \tag{5.23}$$

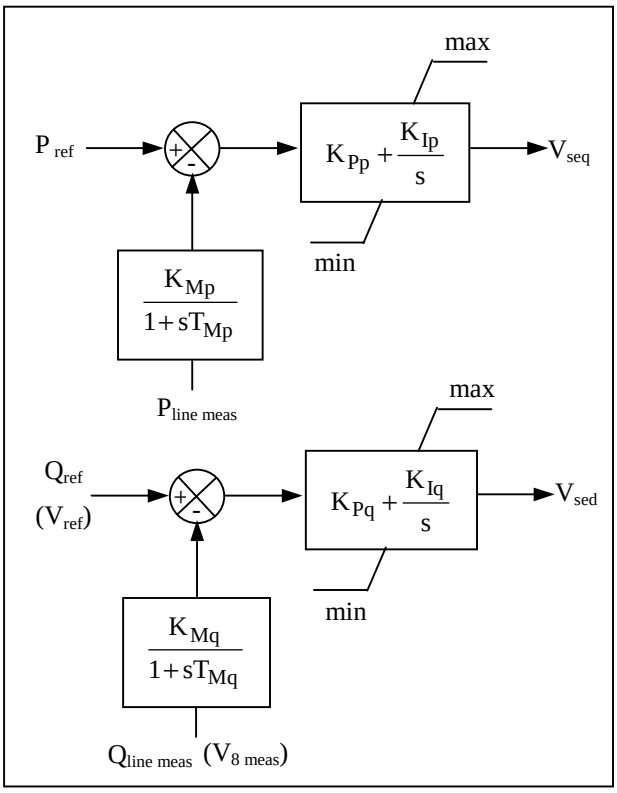


Figure 5.6 – Series converter control of the UPFC

Case B. Real and Reactive Power Control

The second control scheme for the series converter, initially proposed in [58, 64] and based on the d-q transformation of the ac input signals, has also been adopted here. It should be noted that all signals needed for this controller such as sending-end voltage magnitude V_3, receiving-end voltage magnitude V_8, and line current I_{line} are measured, in all three phases, and then transformed into a p.u. d-q synchronously rotating reference frame; the control signals obtained by this transformation are dc signals. More about the d-q transformation can be found in Appendix A.

In this control scheme, the inputs are d- and q- components of the series injected voltage and the outputs are transmission line currents. The line current references are derived from the real and reactive power orders and the measured receiving-end bus voltages. The idea for this control scheme follows basically from the system equations explained in detail in Appendix B.

Thus, if the balanced three-phase system is transformed into a d-q synchronously rotating reference frame and the new coordinate system is defined such that the d-axis is always coincident with instantaneous voltage vector at the sending-end bus v_3, i.e., $v_{3d}=|v_3|$, $v_{3q}=0$, the d- and q- components of the line current are:

$$\frac{d\Delta i'_{lined}}{dt} = -\frac{\omega_B R'_L}{L'_L}\Delta i_{lined} + \omega\Delta i'_{lineq} + \frac{\omega_B}{L'_L}(\Delta v'_{3d} - \Delta v'_{sed} - \Delta v'_{8d}) \qquad (5.24)$$

$$\frac{d\Delta i'_{lineq}}{dt} = -\omega\Delta i'_{lined} - \frac{\omega_B R'_L}{L'_L}\Delta i_{lineq} + \frac{\omega_B}{L'_L}(-\Delta v'_{seq} - \Delta v'_{8q}) \qquad (5.25)$$

Equations (5.24) and (5.25) result in the control blocks for the series converter shown in Figure 5.7. The two new variables x'_1 and x'_2 shown in equations (5.26) and (5.27) below are used as the output of the control system consisting of two PI controllers.

$$x_1' = \frac{\omega_B}{L_L'}\left(\Delta v_{3d}' - \Delta v_{sed}' - \Delta v_{8d}'\right) \tag{5.26}$$

$$x_2' = \frac{\omega_B}{L_L'}\left(-\Delta v_{seq}' - \Delta v_{8q}'\right) \tag{5.27}$$

Hence, the control system is given by the following two equations, where values $i_{lined,ref}'$ and $i_{lineq,ref}'$ are the reference values of the real and reactive series converter current components, and K_p and K_I are the controller proportional and integral gains, respectively.

$$x_1' = \left(K_P + \frac{K_I}{s}\right)\left(\Delta i_{lined,ref}' - \Delta i_{lined}'\right) - \omega \cdot i_{lineq}' \tag{5.28}$$

$$x_2' = \left(K_P + \frac{K_I}{s}\right)\left(\Delta i_{lineq.ref}' - \Delta i_{lineq}'\right) + \omega \cdot i_{lined}' \tag{5.29}$$

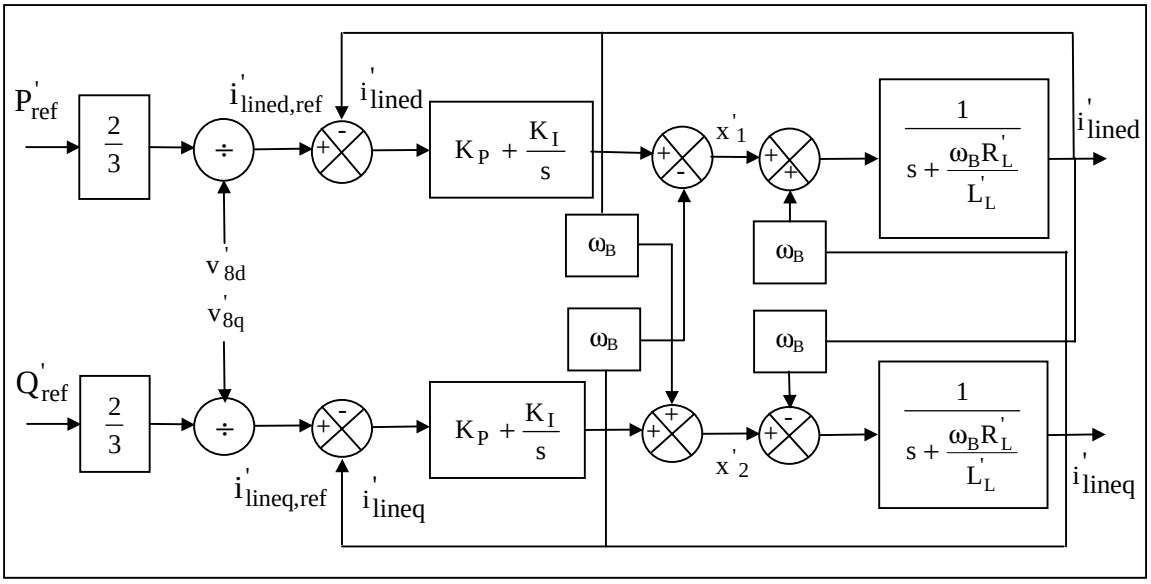


Figure 5.7 – Series converter d-q-based control of the UPFC

It is important to notice that the d- and q- components of three-phase line currents have a linear relationship with the d- and q- components of the series injected voltage. Thus, the designed control system is linear and the response of the closed loop depends strictly on the performance of the designed regulators.

Case C. Power/Frequency Oscillation Damping

The stability of a machine depends on the existence of two torque components; a synchronizing torque T_S that is in phase with the power (torque) angle perturbations $\Delta\delta$, and a damping torque T_D that is in phase with the speed deviations $\Delta\omega$. Thus, the change in electrical torque of a synchronous machine ΔT_e following a perturbation can be represented by [27]:

$$\Delta T_e = T_S \Delta\delta + T_D \Delta\omega \tag{5.30}$$

For a machine to remain in synchronism after the perturbation, both torque components T_D and T_S have to be positive and sufficiently large. Lack of sufficient damping leads to oscillatory behavior of machine output quantities, and sometimes even to instability.

Since the UPFC is able to act almost instantaneously to changes in power, it is possible to improve damping and transient stability of a power system by coordinated control actions of the UPFC. Thus, power oscillations resulting from swings in rotor angles can be readily damped by using the series branch voltage of the UPFC to control the system power flow.

Finally, the modulation controller from Figure 5.8, which was originally proposed in [64], is modified and used here to damp power/frequency oscillations in the test network. This controller uses directly the machine slip $\Delta\omega$ of any given machine to modify the real

power signal reference p'_{line} in any of the two power controls proposed here for the series converter. The problem with applying this controller in large systems is to select the most appropriate machine for using its signal in the power oscillation controls well as to communicate the measured variables, as explained in [28]. In practical systems, it is better to use local power or frequency signals to damp the oscillations; however, the problem then is whether the control location is appropriate for any significant damping, considering that the controller location may be chosen with this sole objective in mind.

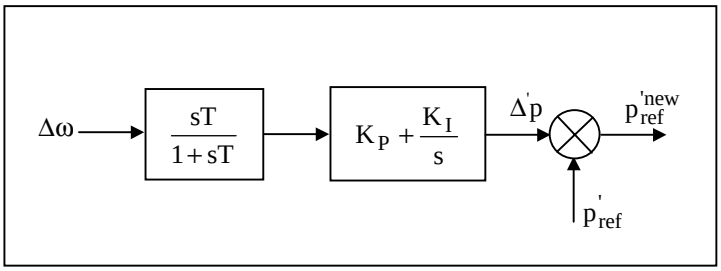


Figure 5.8 – Power modulation control

5.7 EMTP Time-Domain Simulations

The test system is subjected to different perturbations to simulate the detailed UPFC model response. Thus, the following cases are studied:

(1) The load at the end of the UPFC line (Buses 3-11) is increased in three steps until the full load has been reached. For these studies, the power–voltage scheme depicted in Figure 5.6 is used to control the series injected voltage. The shunt converter is used to keep the sending-end voltage at a reference value.

(2) A three-phase fault through an impedance is applied at Bus 6 in close proximity to the UPFC. The control scheme shown in Figure 5.7 is used

here to control the real power flow in the transmission line and the bus voltage magnitude at the load side.

(3) The UPFC is used to damp oscillations on the generator output power caused by a three-phase fault at Bus 6. The real and reactive power flows in the transmission line are controlled using the control scheme shown in Figure 5.8.

5.7.1 Variable Load Results

Load variations at 5 s and 6 s are simulated on Bus 10 to study the UPFC response, as well as to validate the detailed UPFC model for small-disturbance stability analysis. A relatively large pre-fault simulation period permits the initial transients caused by the UPFC start-up to die out. The EMTP results for this case are shown in Figures 5.9 and 5.10.

The UPFC shunt converter is set to control the sending end voltage at 1.0 p.u., while the dc voltage is controlled at 22 kV. The series converter output voltage magnitude and phase angle are controlled so that the real power on the transmission line is kept at 70 MW/phase, while the receiving end voltage magnitude is maintained at 0.97 p.u. The EMTP results show the UPFC performance is adequate in redirecting the real power flow as well as keeping the sending and receiving-end voltages at the ordered magnitudes. It is also interesting to notice that the UPFC, due to the voltage regulation at the sending and receiving-ends, basically works as a phase shifter introducing a series inserted voltage of appropriate magnitude and phase angle between the two ends of the line. It is also important to appreciate that the series converter control used in these simulations was not easy to tune. The main reason for this problem lies in a fact that this control scheme relies on having strong reactive support on the receiving-end of the line as previously explained.

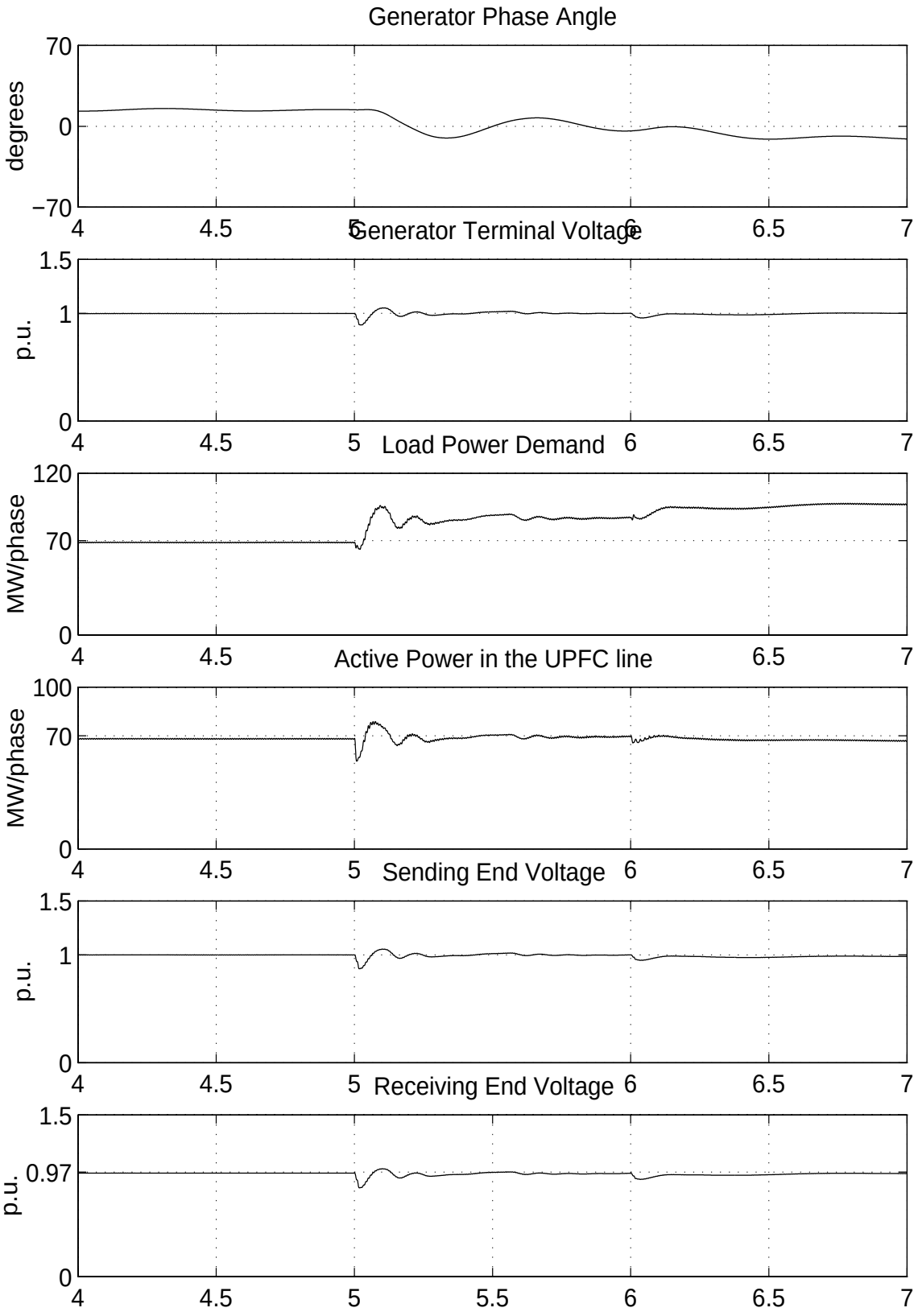


Figure 5.9 – Load variation results for the UPFC

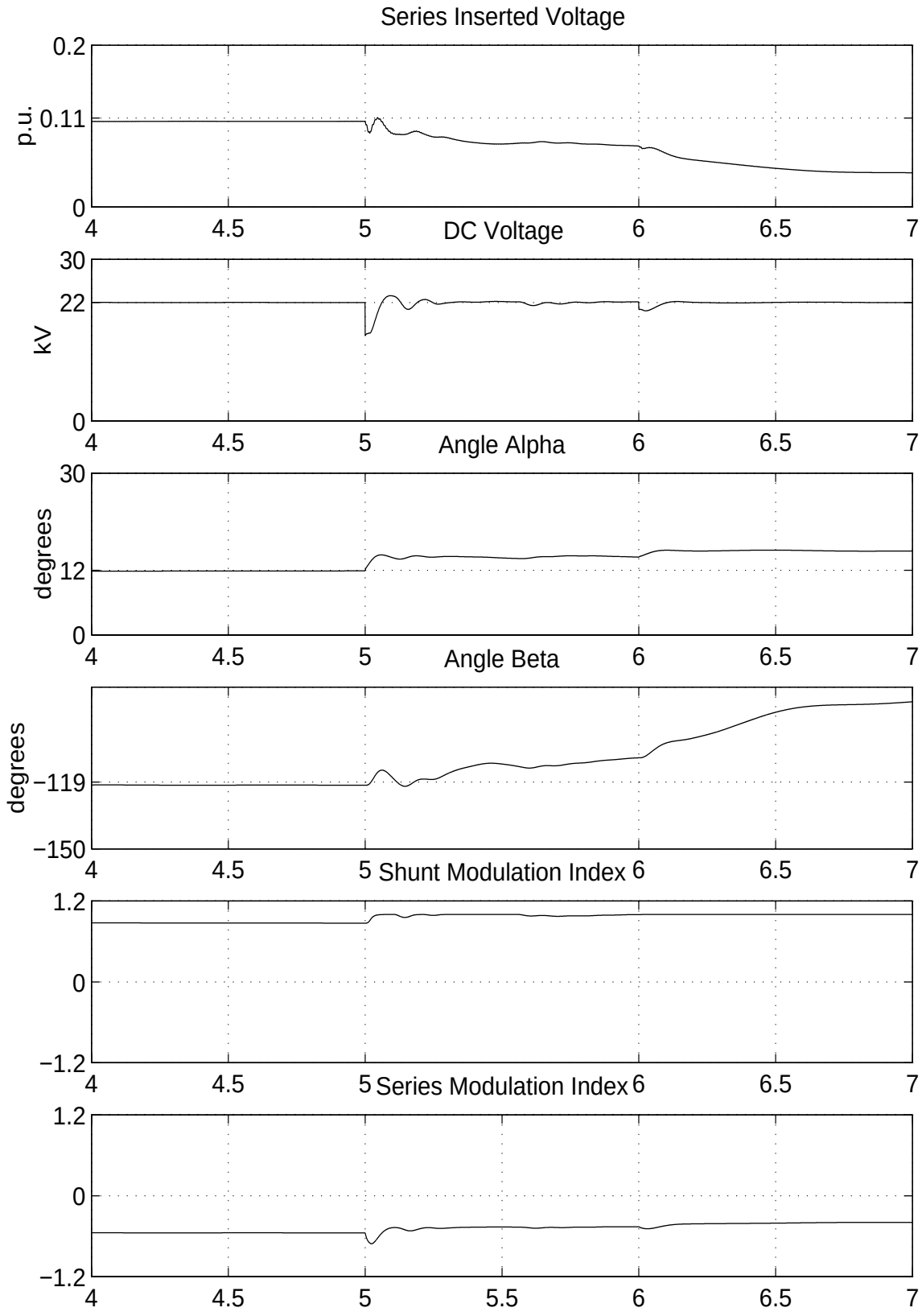


Figure 5.10 – Load variation results for the UPFC

5.7.2 Three-Phase Fault Results

A three-phase fault through a relatively small impedance is applied at Bus 6 at 4.0 s for full load conditions at Bus 10. Nine cycles after the fault, i.e., at 4.15 s, the circuit breaker between Buses 4 and 5 is opened, clearing the fault and disconnecting the load at Bus 7. The generator at Bus 3, which is equipped with an AVR to keep its terminal voltage at 1.0 p.u., recovers successfully after clearing the fault, as it can be seen on the corresponding waveforms shown in Figures 5.11 and 5.12.

The series converter controls the real power flow at 80 MW/phase and recovers successfully after the fault. The upper parallel ac line delivers the rest of the total load demand, i.e. 25 MW/phase for a total load of 315 MW. The receiving-end voltage magnitude is also controlled successfully at the reference voltage by the series converter. The shunt converter control also operates as expected, keeping the voltage magnitude at the sending-end and the dc voltage at 1.0 p.u. and 22 kV, respectively. It should be noted that the series converter protection did not operate in this case, as the transmission line current limits were not reached.

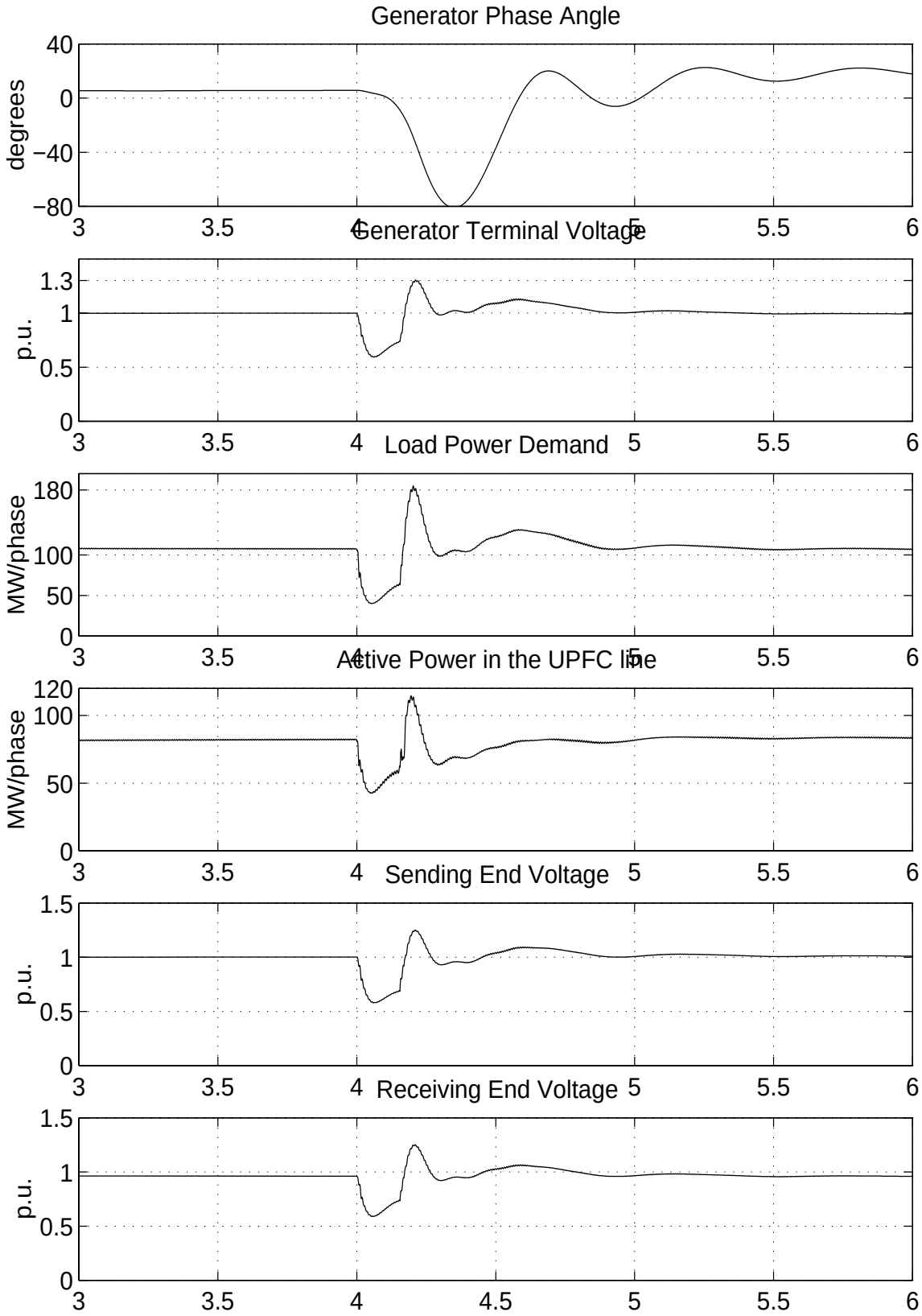


Figure 5.11 – Three-phase fault results for the UPFC

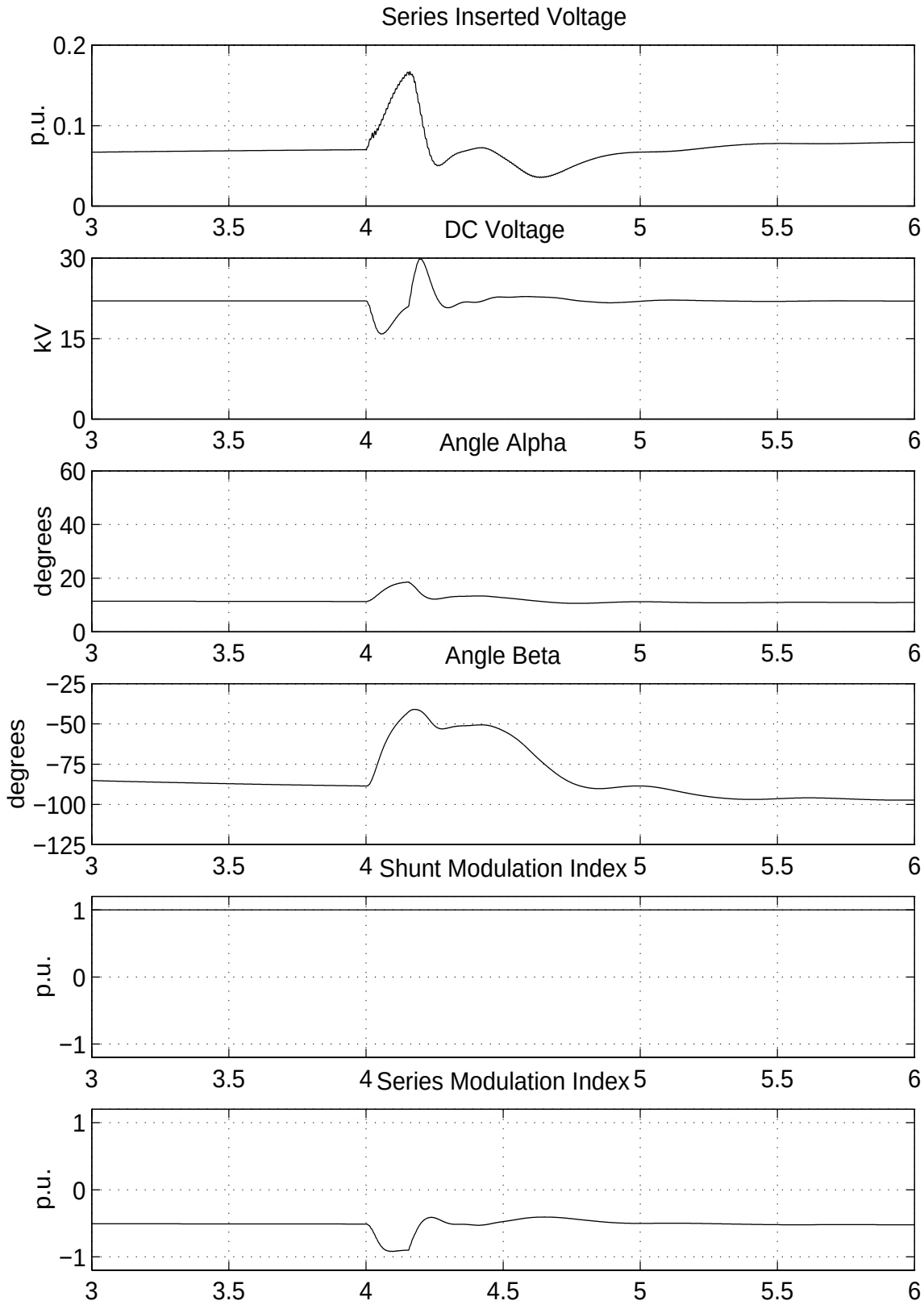


Figure 5.12 – Three-phase fault results for the UPFC

5.7.3 Power Oscillation Damping

The Automatic Power Control Flow Mode used in previous examples is now changed to a Power Oscillation Damping Control Mode by introducing a damping controller, as explained in Case C. The basic series converter control scheme used here is depicted in Figure 5.8. In this control scheme, good response is achieved due to the linear relationship between the input d- and q-components of three-phase line current and the d- and q-components of the output series voltage.

The results depicted in Figure 5.13 show the results obtained with the UPFC controlling the real power flow in the line, whereas Figure 5.14 shows the results for the very same controller but with the additional power oscillation damping control. The comparison between these two sets of results demonstrates the adequate performance of the power oscillation damping scheme. The generator phase angle oscillations are damped faster, and hence the system becomes more stable. However, in order to damp the phase angle oscillations, the transmission line real power flow oscillates too which could be a problem for the dynamic load connected at the end of the line.

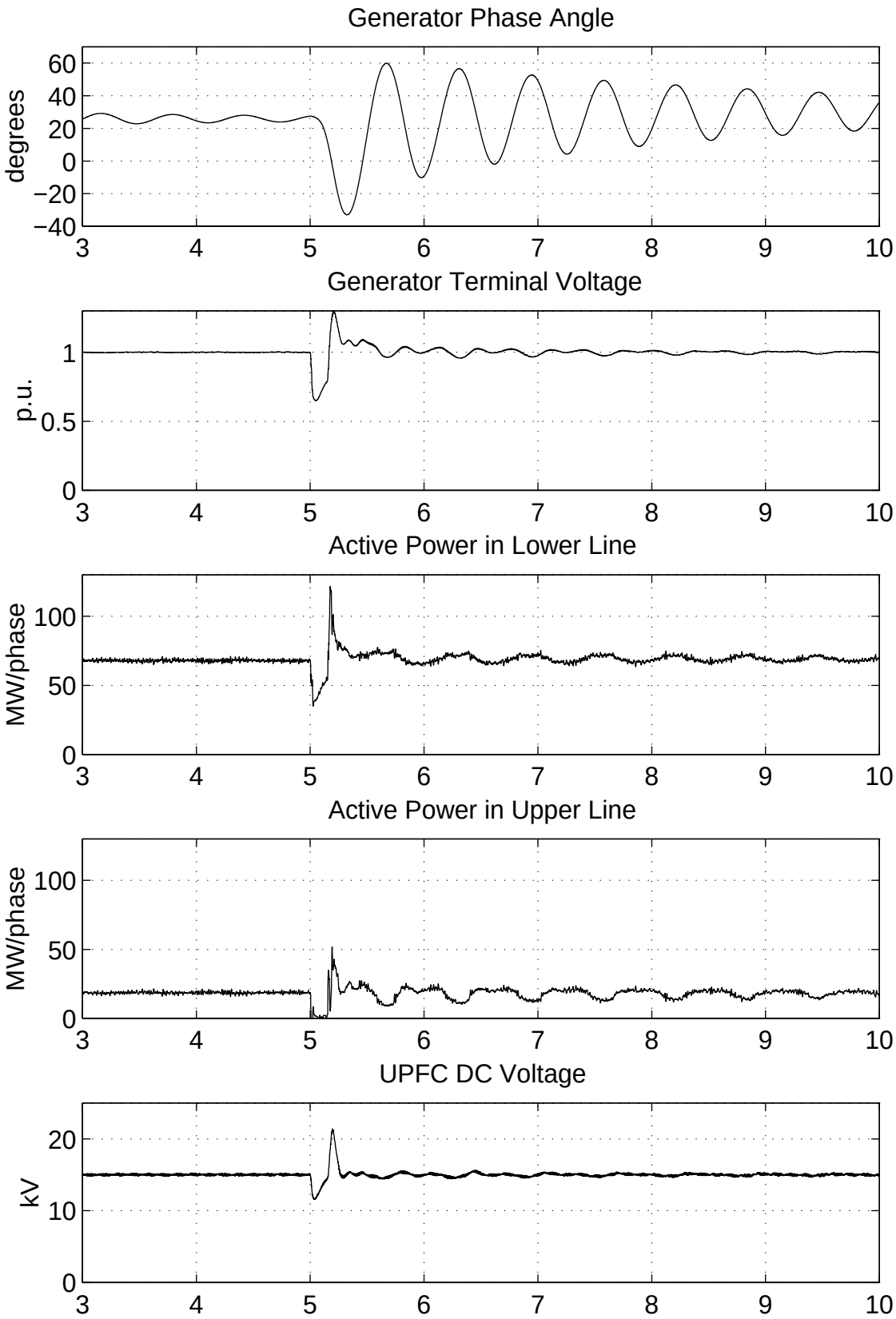


Figure 5.13 – Fault results for the UPFC in Automatic Power Control Mode

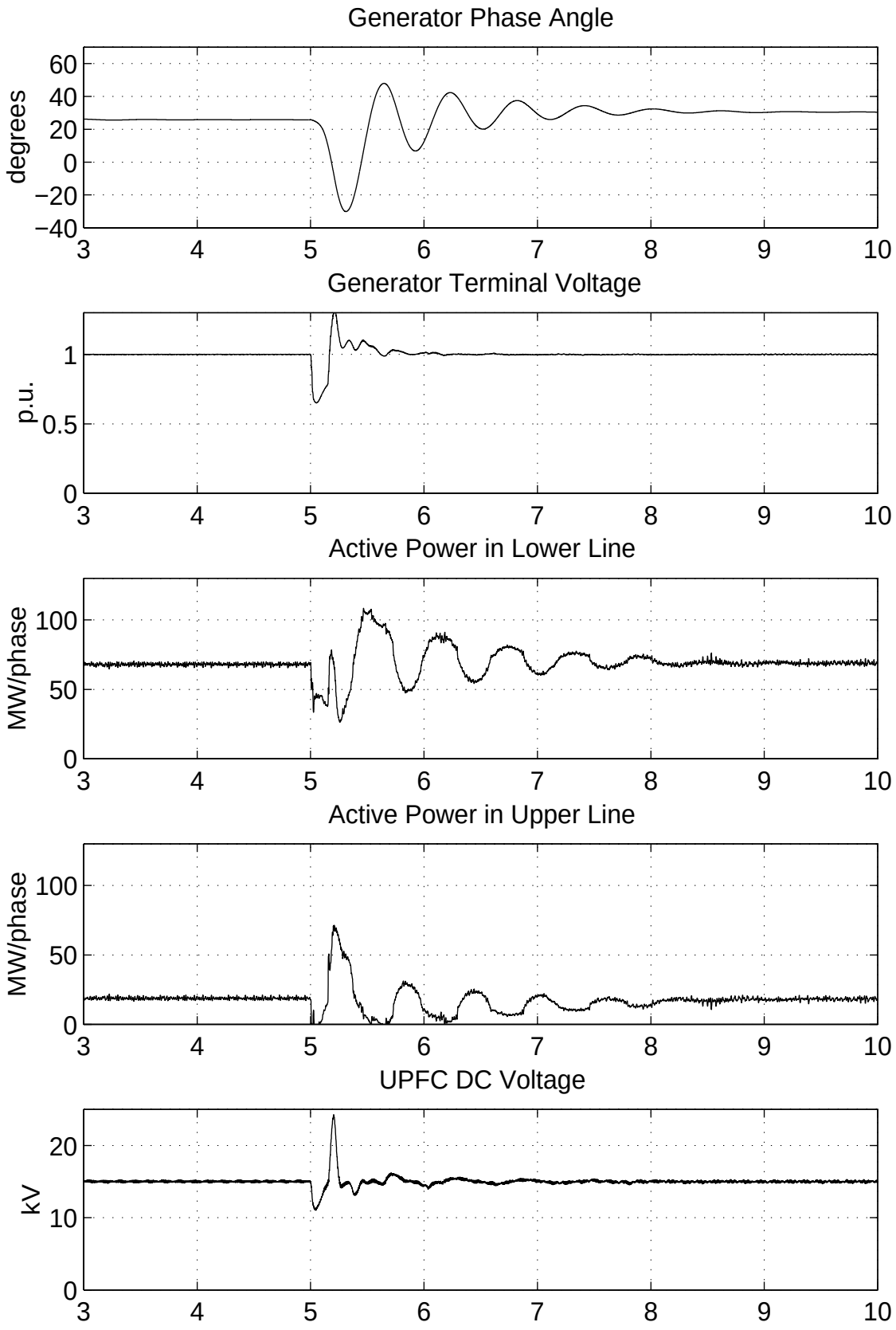


Figure 5.14 – Fault results for the UPFC in Power Damping Oscillation Mode

5.8 Summary

This chapter presents the fundamentals of a UPFC, explaining in detail the operating principles and limits as well as practical ratings of the equipment. Also, for the purpose of demonstrating the power flow control capabilities of the UPFC, the basic relationships and differences between a UPFC compensated and an uncompensated transmission line have are discussed.

An EMTP implementation of the UPFC is explained, together with a detailed description of the various SPWM-based control schemes. Since independent control of real and reactive powers within the equipment limits is possible, the UPFC control objectives and schemes can vary significantly, thus, some of the most significant control schemes and objectives are described in detail here.

The UPFC with SPWM-based controller allows for the control of the amplitude and phase angle of both shunt and series converter output voltages. It is shown here that the UPFC control de-coupling is possible and even desirable due to its simplicity and price reduction. The shunt converter scheme presented here is being previously proposed by other researchers, and is based on the general idea that the necessary balance between the ac and dc real powers can be successfully controlled through the dc voltage, while controlling in the same time the sending-end voltage magnitude. It is important to notice that the d- and q- decomposition of the shunt converter output voltage is not necessary to control this converter, as shown here, although that is usual practice in the present literature.

It is shown here that direct control of the series injected voltage is not desirable, due to the non-linear relationships between the amplitude and phase angle of the injected voltage and the converter real and reactive power outputs. Hence, the series converter output voltage is decomposed suing a d-q transformation with respect to the sending-end bus voltage, so that d- and q- components can be controlled independently and through two separate PI controllers.

Three different control schemes for the series converter, together with a novel approach of directly controlling the receiving-end voltage magnitude instead of the transmission line reactive power flow, are described and evaluated here. The results of time-domain simulations in the EMTP demonstrate the adequacy of proposed control schemes, given the fast and proper response of the series converter. Similar performance is observed for all the different control schemes described here; however, the implementation as well as the design of the proposed decoupled control is simpler than the coupled d-q control.

Finally, the EMTP results obtained for the UPFC with power oscillation damping control show that the proper damping can be provided by a UPFC of adequate rating.

Chapter 6.

TRANSIENT STABILITY AND POWER FLOW MODELS OF FACTS CONTROLLERS

6.1 Introduction

In simulation studies including FACTS controllers, detailed three-phase FACTS models [69] may be required as well as simplified three-phase models. Detailed three-phase studies should include all necessary elements of a FACTS controller together with its non-linearities. The control blocks should be modeled in great detail, representing all necessary firing pulses for each of the valves. Such models for the STATCOM, SSSC and UPFC have been described in previous chapters.

Steady state and stability studies include power flow, transient stability and eigenvalue computations in investigating interactions between the FACTS controller and power system at or near the fundamental frequency of operation. The models for these studies should be simplified to reduce computational time; yet, they should accurately capture the controller behavior at the desired fundamental frequency. The controls should be represented with all functions that are relevant for these studies.

Several authors have demonstrated the importance of realistic modeling of FACTS controllers for steady state and transient stability studies [76, 77, 78, 80]. The STATCOM and SSSC have been typically modeled as ideal voltage or current sources [81, 82] without operating and control limits, i.e. capable of generating or absorbing unlimited amounts of reactive power. Recently, more accurate dynamic and steady state models, similar to the ones presented in this thesis have been proposed based on power balance principles between the ac and dc sides of the VSC [79]. However, these models have been discussed at a theoretical level and only tested in systems subjected to small perturbations. The STATCOM and SSSC models proposed in this chapter are tested in

more realistic power system scenarios, which clearly identify the need for representing properly operating and control limits.

The UPFC model proposed in [62] is modeled in the EMTP and represented as controllable voltage sources connected in shunt and series to a power system. In [83], the UPFC model consists of a controllable voltage source added in series with the transmission line, plus two current sources added in shunt to balance the power flow through the controller. The UPFC given in [84] is made up of two ideal synchronous voltage sources, while in [23], the authors use the external macro capabilities of a popular power system analysis tool to model the UPFC. The UPFC is modeled using coupled-source models, as a series voltage source is generally not available in commercial power system software packages. The UPFC model presented in [85] includes the dc side of the UPFC, which makes this model more appropriate since the dc voltage limits can also be included in the model; however, the losses in the VSC circuit are not represented properly in the model. The UPFC model presented here properly represents the ac as well as the dc side of the controller and, therefore, properly models all operating and control limits. Although the model is incorporated and tested only in the EMTP, it can be easily incorporated in to any other popular software package for power system analysis.

This chapter hence concentrates on describing and validating transient stability and power flow models of the STATCOM, SSSC and UPFC. The novel models presented here accurately represent the behavior of the controllers for steady-state and transient stability studies. The proposed models are studied and validated using the EMTP, where the proposed simplified models are implemented and compared with the detailed models. Tests are carried out using a realistic power system example using various realistic scenarios.

6.2 STATCOM Modeling

The STATCOM transient and steady state models presented here include all operating and control characteristics and limits needed to properly represent this controller in stability and steady-state studies.

6.2.1 STATCOM Transient Stability Model

In transient stability modeling, it is typically assumed that the converter output voltage is a balanced and harmonic free waveform at fundamental frequency since typical transient system oscillations are in the order of 2 –3 Hz under balanced operating conditions. Hence, for transient stability studies, the VSC can be accurately represented as a sinusoidal voltage source operating at fundamental frequency.

In order to develop a fundamental frequency balanced model of the STATCOM, a power balance technique, similar to the one used in [45] for developing dq-axis controls of VSC-based static compensators or in [73] for steady state modeling of VSC-based drives, is used here.

The proposed model allows the representation of different types of controls and contains all relevant physical variables required to simulate various phase or PWM control strategies, as already described in [65].

For the STATCOM, instantaneous power flowing into the converter from the ac bus, when neglecting transformer losses, may be represented by:

$$p = 3\frac{a\, V_{sh} V_{ac}}{X} \sin \alpha \qquad (6.1)$$

where V_{ac} is the rms voltage of the bus where the STATCOM is connected, V_{sh} is the rms converter output voltage, *a* stands for the turns ratio of the shunt coupling transformer, and X represents the coupling transformer equivalent leakage reactance. Angle α is the phase shift between the bus phase voltage v_{ac} and the corresponding converter output voltage v_{sh}, i.e.,

$$v_{ac} = \sqrt{2}\, V_{ac} \sin(\omega t + \delta) \tag{6.2}$$

$$v_{sh} = \sqrt{2}\, V_{sh} \sin(\omega t + \delta - \alpha) \tag{6.3}$$

Inspection of equations (6.2) and (6.3) shows that when the converter output voltage lags the system bus voltage ($\alpha > 0$), the real power flows from the ac bus into the VSC to charge the dc capacitor. When the converter output voltage leads the system bus voltage ($\alpha < 0$), the direction of real power is from the VSC to the ac system, thus discharging the dc capacitor.

The dc capacitor voltage and the converter output voltage are proportional, i.e.,

$$V_{sh} = k \cdot V_{dc} \tag{6.4}$$

where V_{dc} is the average dc voltage on the dc capacitor, and V_{sh} is the rms value of the converter output voltage. The k factor comes from the magnitude of the fundamental frequency component of the Fourier series representation of the VSC output voltage. This factor for the 12-pulse phase-controlled VSC is constant and equal to 0.9; for the VSC with higher number of pulses this constant changes accordingly. For PWM control, k is variable and controlled through the amplitude modulation ratio m_a, as $k = n \cdot m_a$, where for the two-level converter, $n = 1/2\sqrt{2}$.

If the converter switching and transformer losses are neglected, from the power balance equation, the instantaneous power flowing from the ac system into the VSC, and vice versa, is equal to the power on the dc side of the VSC, i.e.,

$$P_{ac} = P_{dc} \tag{6.5}$$

This power balance can be also expressed as

$$\begin{aligned} 3\frac{aV_{sh}V_{ac}}{X}\sin\alpha &= V_{dc}I_{dc} \\ &= V_{dc}C\frac{dV_{dc}}{dt} \end{aligned} \tag{6.6}$$

Hence, from the equation (6.4) and (6.6), it follows that the V_{dc} voltage changes are defined by the nonlinear differential equation:

$$\frac{dV_{dc}}{dt} = \frac{3\,a\,k\,V_{ac}}{C\,X}\sin\alpha \tag{6.7}$$

From equation (6.7), it is possible to see that for $\alpha > 0$, $dV_{dc}/dt > 0$ which leads to the dc capacitor charging. For $\alpha < 0$, $dV_{dc}/dt < 0$, with the dc capacitor discharging. When $\alpha = 0$ then $dV_{dc}/dt = 0$, resulting in the dc voltage remaining constant.

The transformer losses can be neglected, as these usually represent a very small portion of the total STATCOM losses. Converter losses, on the other hand, can be significant, depending on the number of switches as well as the switching frequency. These losses can be readily included into these equations by adding a resistance R_C in parallel with the dc capacitor. Thus, equation (6.7) can be modified as follows:

$$\frac{dV_{dc}}{dt} = \frac{3\,a\,k\,V_{ac}}{C\,X}\sin\alpha - \frac{1}{R_C\,C}V_{dc} \tag{6.8}$$

In this case, steady state operation leads to an $\alpha = \alpha_0$, due to the real power required to cover the converter losses. Hence, α_0 can be determined from the following equation:

$$\frac{3\,a\,k\,V_{ac}}{C\,X}\sin\alpha_0 = \frac{\Delta V_{dc}}{R_C} \tag{6.9}$$

where ΔV_{dc} represents the change in the STATCOM capacitor voltage with respect to an initial value. This equation can be used to determine the value of R_C from a given value of α_0 obtained from a detailed representation and simulation of the converter.

The results of modeling the STATCOM at fundamental frequency in the EMTP are shown and discussed in Section 6.5.1. With the help of a fundamental frequency tracking system based on a Fourier filter already used and explained in Chapter 3, the VSC is represented in the EMTP as a controlled voltage source based on equations (6.3), (6.4) and (6.8). The controllable voltage source is connected to the ac system through a step-down transformer and filtering devices equivalent to those of the detailed model represented in Chapter 3. All system control blocks remain unchanged, with the exception of the valve switching logic, which is removed.

The STATCOM model is shown in Figure 6.1. It is used here to represent a 12-pulse VSC under phase control, as well as PWM operation of a 6-pulse VSC. The STATCOM model is therefore universal and applicable for any transient stability study, which assumes balanced operating conditions and small frequency excursions.

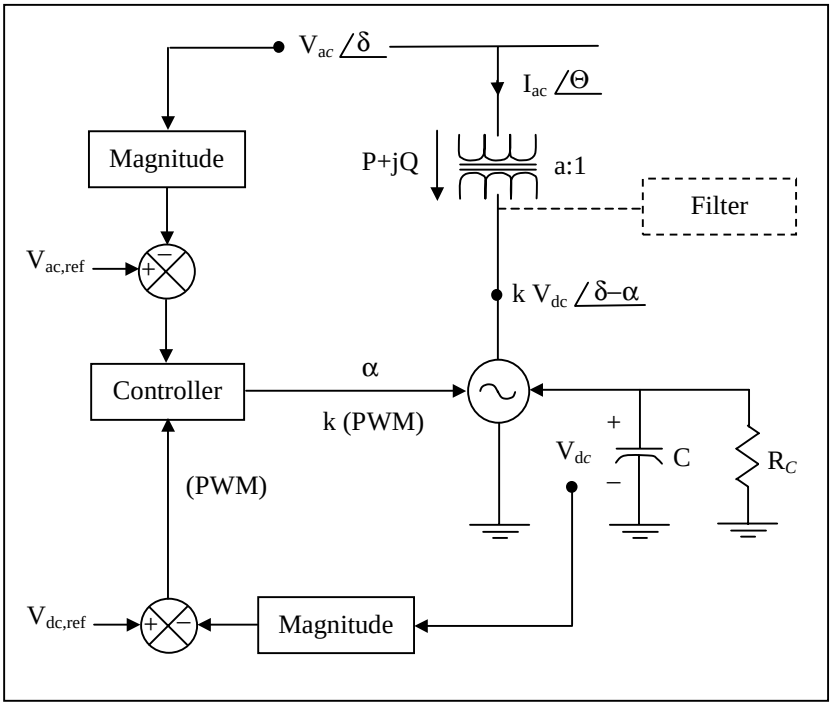


Figure 6.1 – Transient stability model of a STATCOM

Assuming balance fundamental frequency voltages, the controller can be accurately represented in transient stability studies using the basic model shown in Figure 6.1. The p.u. differential-algebraic equations (DAE) corresponding to this model can be summarized as follows:

$$\begin{bmatrix} \dot{x}_c \\ \dot{\alpha} \\ \dot{k} \end{bmatrix} = f_c\left(x_c, \alpha, k, V_{ac}, V_{dc}, V_{ac,ref}, V_{dc,ref}\right) \tag{6.10}$$

$$\dot{V}_{dc} = \frac{3\,a\,k\,V_{ac}}{C\,X}\sin\alpha - \frac{1}{R_C\,C}V_{dc} \tag{6.11}$$

$$0 = 3\,V_{ac}I_{ac}\cos(\delta-\Theta) - \frac{V_{dc}^2}{R_C} \tag{6.12}$$

$$0 = \begin{bmatrix} P + \dfrac{a\,k\,V_{dc}V_{ac}}{X}\sin(\delta - \alpha) \\ Q - \dfrac{V_{ac}^2}{X} + \dfrac{a\,k\,V_{dc}V_{ac}}{X}\cos(\delta - \alpha) \end{bmatrix} \tag{6.13}$$

where x_c and $f_c(\cdot)$ stand for the internal control variables and equations, respectively, and vary depending on which STATCOM internal control structure is used.

This model allows the full representation of control blocks except the valve switching logic. This means that the STATCOM operating limits can be easily included. The controller limits are defined in terms of the converter output current and the dc voltage limits. In simulations, the limits on the maximum converter output current can be implemented such that as soon as the maximum current is sensed, the integrator blocks are stopped.

In the EMTP simulation of this model for the phase controlled STATCOM, the integration of the phase angle α is stopped when the measured converter output current reaches the limit, which in turn kept the dc voltage and hence the converter output voltage at its last value. In the PWM-based STATCOM, the controller has two outputs: the amplitude modulation factor m_a and the output angle α. If the STATCOM reaches its maximum current limit, the amplitude modulation factor is held at its last value, while the maximum and minimum dc voltage are controlled through the phase angle α.

6.2.2 STATCOM Steady State Model

The steady state or power flow model can be readily obtained from the stability model equations (6.10), (6.11) and (6.12) by replacing the corresponding equations with the steady state equations for the dc voltage and the steady state V-I characteristics. Thus, the steady state equations are

$$0 = V_{ac} - V_{ac,ref} \pm X_{SL} I_{ac} \tag{6.14}$$

$$0 = \frac{3\,a\,k\,V_{ac}}{C\,X} \sin\alpha - \frac{1}{R_C\,C} V_{dc} \tag{6.15}$$

$$0 = \frac{3\,a\,k\,V_{ac}}{X} \sin\alpha - \frac{V_{dc}}{R_C} \tag{6.16}$$

$$0 = \begin{bmatrix} P + \dfrac{a\,k\,V_{dc}V_{ac}}{X} \sin\alpha \\ Q - \dfrac{V_{ac}^2}{X} + \dfrac{a\,k\,V_{dc}V_{ac}}{X} \cos\alpha \end{bmatrix} \tag{6.17}$$

The positive sign in equation (6.14), which defines the steady state control characteristics with a slope X_{SL} and a reference voltage $V_{ac,ref}$, is used when the STATCOM is operating in its capacitive region, while a negative sign is used in the inductive mode. Equation (6.15) represents the power balance equation, while (6.16) corresponds to the dynamic dc voltage equation (6.11). Equation (6.17) defines the real and reactive power that STATCOM exchanges with the ac system.

The limits on the current I_{ac} as well as any limits in any other steady state variables can be directly introduced in this model. The STATCOM operating limits on the maximum and minimum STATCOM output current and dc voltage can be readily incorporated into these equations since the control variables which define these two variables are explicitly represented in the model.

6.3 SSSC Modeling

6.3.1 SSSC Transient Stability Model

In order to develop a fundamental frequency model of the SSSC, a power balance equation is used here. Thus, assuming that all system voltages and currents are balanced, the three-phase instantaneous power exchanged between the ac system and the converter may be represented as

$$p = 3\,V_{SR}\,I_{line}\cos(\delta - \Theta) \tag{6.18}$$

where $V_{SR}\angle\delta$ and $I_{line}\angle\Theta$ are the rms phasors of the SSSC inserted voltage and the transmission line current, respectively.

For the SSSC, control of the phase shift between the SSSC inserted voltage v_{SR} and the transmission line current i_{line} controls the real power exchanged with the ac system. The real power is associated with over the switching losses and the charge/discharge of the dc capacitor.

$$v_{SR} = \sqrt{2}\,V_{SR}\sin(\omega t + \delta) \tag{6.19}$$

$$i_{line} = \sqrt{2}\,I_{line}\sin(\omega t + \Theta) \tag{6.20}$$

The difference between the controlled voltage and the output voltage at the primary side of the coupling transformer is due to the voltage across the series transformer reactance, i.e.,

$$\mathbf{V}_{SR} = a\,\mathbf{V}_{SSSC} \pm \mathbf{I}_{line}\,X \tag{6.21}$$

where the positive sign corresponds to the capacitive operation, while the negative sign indicates inductive operation of the SSSC; *a* stands for the series transformer ratio, and V_{SSSC} is the rms phasor of the SSSC output voltage.

The rms value of the SSSC output voltage and on the converter side of the coupling transformer is:

$$v_{SSSC} = \sqrt{2}\, V_{SSSC} \sin\left(\omega t + \Theta \pm \frac{\pi}{2} - \beta\right) \tag{6.22}$$

where V_{SSSC} is directly proportional to the dc voltage,

$$V_{SSSC} = k\, V_{dc} \tag{6.23}$$

Again, *k* is a constant for the phase controlled SSSC, and equal to 0.9 in case of a 12-pulse VSC. If the SSSC is PWM-based, then the factor *k* is variable, as $k = 1/2\sqrt{2} \cdot m_a$, where the modulation factor m_a is a control output that depends on the system conditions.

In case of a heavily loaded transmission line, the voltage across the transformer reactance may be significant and should be included in the model. In this case, the rms voltage on transformer line side of the SSSC, can be calculated as

$$V_{SR} = V_s - V_r \tag{6.24}$$

where V_s and V_r are the rms voltages at the sending and receiving ends. Hence, the dc voltage behavior can be described by the following nonlinear differential equation:

$$\frac{dV_{dc}}{dt} = \frac{3\, V_{SR}\, I_{line}}{C\, V_{dc}} \cos(\delta - \Theta) - \frac{1}{R_C\, C} V_{dc} \tag{6.25}$$

Figure 6.2 shows the one-line diagram of the proposed transient stability model of SSSC, as modeled in the EMTP. The model includes the series coupling transformer, the three-phase controllable voltage source, and all control blocks, except those related to the valve switching logic. The magnitude of the controllable voltage source shown in equation (6.22) can be calculated by using equation (6.23) and (6.25). The phase angle β is calculated with respect to the transmission line current i_{line} as shown in equation (6.22).

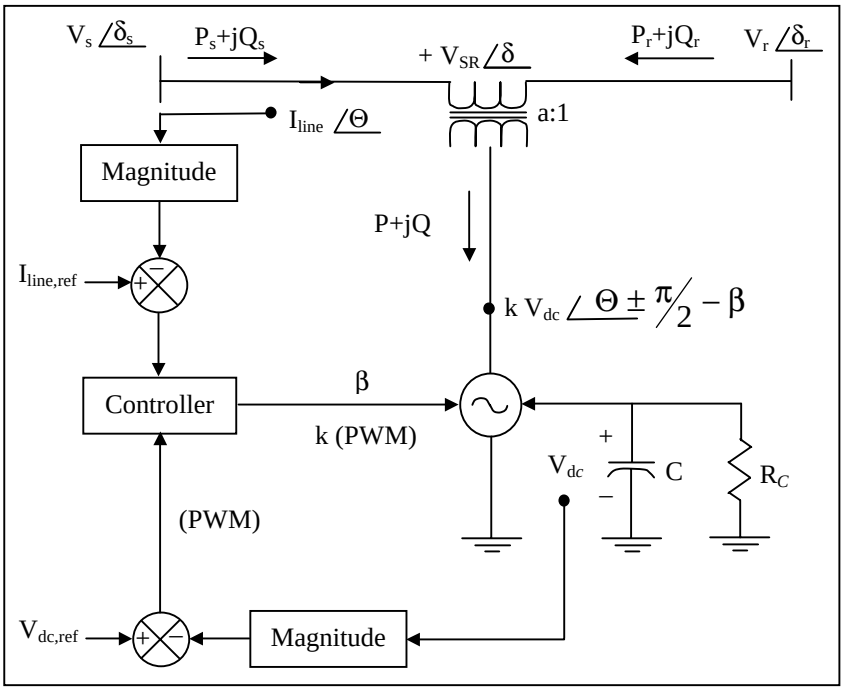


Figure 6.2 – Transient stability model of a SSSC

The SSSC transient stability model can be universally represented with the following DAEs:

$$\begin{bmatrix} \dot{x}_c \\ \dot{\beta} \\ \dot{k} \end{bmatrix} = f_c\left(x_c, \beta, k, V_{pq}, V_{dc}, I_{line,ref}, V_{dc,ref}\right) \tag{6.26}$$

$$\frac{dV_{dc}}{dt} = \frac{3\,V_{SR}\,I_{line}}{C\,V_{dc}}\cos(\delta - \Theta) - \frac{1}{R_C\,C}\,V_{dc} \tag{6.27}$$

$$0 = \begin{bmatrix} P_s - V_s I_{line}\cos(\delta_s - \Theta) \\ Q_s - V_s I_{line}\sin(\delta_s - \Theta) \\ P_r + V_r I_{line}\cos(\delta_r - \Theta) \\ Q_r + V_r I_{line}\sin(\delta_r - \Theta) \\ P - P_r + P_s \\ Q - Q_r + Q_s \\ P + \frac{a\,k\,V_{dc}V_{SR}}{X}\sin\left(\delta - \Theta \pm \frac{\pi}{2} - \beta\right) \\ Q + \frac{V^2_{SR}}{X} - \frac{a\,k\,V_{dc}V_{SR}}{X}\cos\left(\delta - \Theta \pm \frac{\pi}{2} - \beta\right) \end{bmatrix} \tag{6.28}$$

where x_c and $f_c(\cdot)$ stand for the internal control variables and equations, respectively, and vary depending on the SSSC internal control structure used.

The proposed SSSC transient stability model contains all physical variables that define the controller. Hence, the SSSC actual control and operating limits can be easily incorporated into this model. Based on the MVA rating of the SSSC and the rating of the system to which the SSSC is connected, there is an upper limit of the series injected voltage. This maximum injection voltage can be readily defined and incorporated into the model; thus, if the magnitude of the injected voltage V_{SR} is larger than a $V_{SR,max}$, then V_{SR} is fixed to this value. Also, the SSSC overload currents must be monitored, so that the controller currents are allowed to reach certain levels for predefined time periods. The transmission line current can also be monitored so that in case of reaching transient

overcurrent limit, the SSSC can be bypassed permanently or for a certain period of time during simulation.

6.3.2 SSSC Steady State Model

The SSSC steady state model can be obtained from equations (6.26) and (6.27) replacing the existing differential and control equations with the corresponding steady state equations for the dc voltage and the line control characteristics of the SSSC as shown in Figure 4.4. The developed model is suitable for either a phase controlled or a PWM-based SSSC.

Thus, from the control equations, the following equation can be obtained:

$$0 = I_{line} - I_{line,ref} \tag{6.29}$$

The following two equations are obtained from the power balance equation and dc voltage dynamic equation, respectively,

$$0 = 3\,V_{SR}\,I_{line}\cos(\delta - \Theta) - \frac{V_{dc}^2}{R_C} \tag{6.30}$$

$$0 = \frac{3\,V_{SR}\,I_{line}}{C\,V_{dc}}\cos(\delta - \Theta) - \frac{1}{R_C\,C}\,V_{dc} \tag{6.31}$$

Equations (6.29), (6.30), and (6.31) plus the equation (6.28), define the steady state model of the SSSC.

6.4 UPFC Modeling

6.4.1 UPFC Transient Stability Model

In balanced conditions, the converter output voltage can be assumed to be a harmonic free sinusoidal waveform at fundamental frequency. This implies that the shunt and series converters in the UPFC structure can be modeled as shunt and series voltage sources, connected to the ac system through shunt and series transformers, respectively. Based on this idea, the proposed UPFC model is appropriate for transient stability studies, where transient oscillations are in the order of 2-3 Hz under balanced operating conditions. The one-line diagram of the UPFC transient stability model proposed here is shown in Figure 6.3.

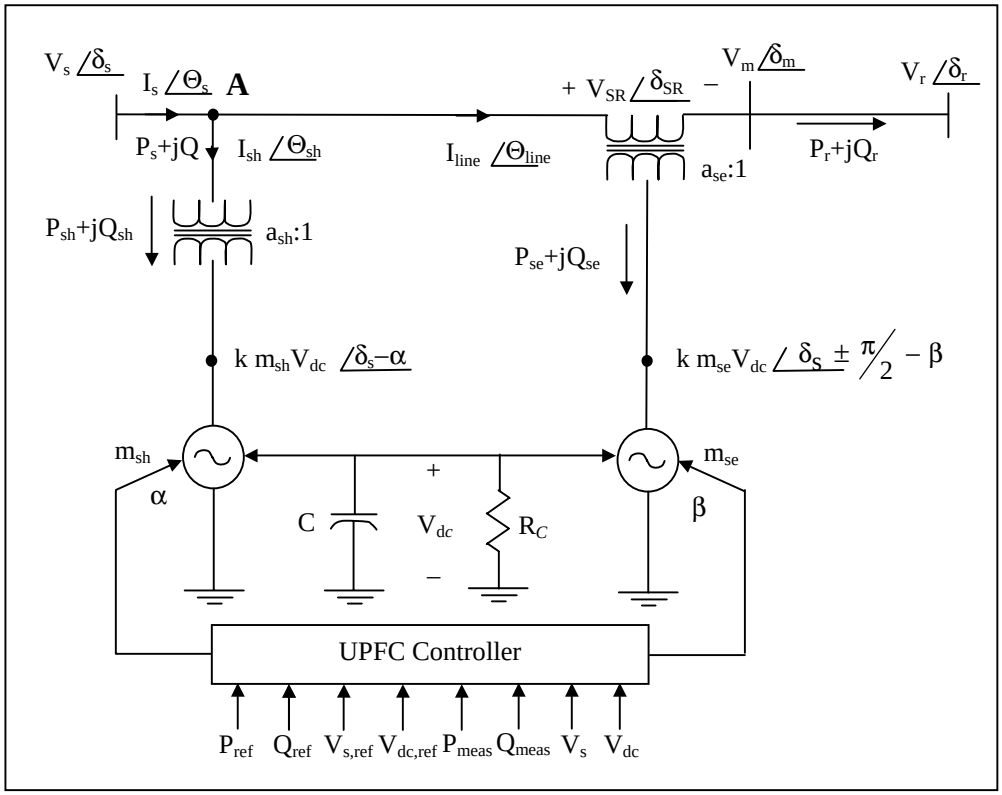


Figure 6.3 – Transient stability model of a UPFC

The model is based on a power balance assumption [74]; the real power going into the shunt converter is equal to the real power going out of the series converter plus the circuit and switching losses and the power stored in the dc circuit, i.e.,

$$P_{sh} = P_{dc} + P_{losses} + P_{se} \tag{6.32}$$

The three–phase instantaneous ac power flowing into/out the shunt converter, neglecting transformer losses and assuming fundamental frequency and balanced conditions, can be defined as

$$p_{sh} = 3\frac{a_{sh} V_{sh} V_s}{X_{sh}} \sin\alpha \tag{6.33}$$

where $V_s\angle\delta_s$ is the rms phasor of the sending-end voltage, $V_{sh}\angle(\delta_s - \alpha)$ is the rms value of the shunt converter output voltage, a_{sh} is the shunt transformer voltage ratio, X_{sh} is the shunt transformer equivalent leakage reactance, and α is the dc voltage control loop output.

On the other hand, the three-phase instantaneous power that the series converter exchanges with the ac system, neglecting transformer losses and assuming fundamental frequency and balanced conditions, is equal to

$$p_{se} = 3 V_{SR} I_{line} \cos(\delta_{SR} - \Theta_{line}) \tag{6.34}$$

where $V_{SR}\angle\delta_{SR}$ is the rms phasor of the series converter output voltage, and $I_{line}\angle\Theta_{line}$ is the rms phasor of the transmission line current.

In the actual implementation of a UPFC controller, one phasor is usually chosen as a reference phasor and the shunt and series converter output voltage are synchronized with

respect to it. Thus, in this case, the sending-end bus voltage phasor is chosen as the reference, i.e.,

$$v_s = \sqrt{2}\, V_s \sin(\omega t + \delta_s) \tag{6.35}$$

$$v_{sh} = \sqrt{2}\, V_{sh} \sin(\omega t + \delta_s - \alpha) \tag{6.36}$$

$$v_{se} = \sqrt{2}\, V_{se} \sin(\omega t + \delta_s - \beta) \tag{6.37}$$

where the rms values of the shunt and series converter output voltages are equal to

$$V_{sh} = k\, m_{sh} V_{dc} \tag{6.38}$$

$$V_{se} = k\, m_{se} V_{dc} \tag{6.39}$$

with $k = 1/2\sqrt{2}$ for PWM-based converters. V_{dc} is the voltage at the dc capacitor, and m_{sh} and m_{se} represent the amplitude modulation ratios for the shunt and series converters, respectively.

The relationship between the series converter phasor voltages at the converter output and the transmission line side is given by

$$\mathbf{V}_{SR} = a_{se}\mathbf{V}_{se} \pm jX_{tr}\,\mathbf{I}_{line} \tag{6.40}$$

The last equation indicates that the voltage across the series transformer reactance depends on the transmission line current. Hence, if the shunt and series converter losses are added together and modeled as a resistance R_C in parallel with the dc capacitor, then equation (6.32) can be represented as

$$3\frac{a_{sh}V_{sh}V_s}{X_{sh}}\sin\alpha = V_{dc}\left(C\frac{dV_{dc}}{dt}\right) + \frac{V_{dc}^2}{R_C} + 3\,V_{SR}\,I_{line}\cos(\delta_{SR} - \Theta_{line}) \quad (6.41)$$

which yields to the dynamic equation for the dc capacitor voltage V_{dc} that can be used to determine the shunt and series converter output voltages; thus,

$$\frac{dV_{dc}}{dt} = \frac{3\,k\,a_{sh}m_{sh}V_s}{C\,X_{sh}}\sin\alpha - \frac{3\,V_{SR}\,I_{line}}{C\,V_{dc}}\cos(\delta_{SR} - \Theta_{line}) - \frac{V_{dc}}{R_cC} \quad (6.42)$$

The UPFC fundamental frequency model proposed here is simulated in the EMTP and the results are shown and discussed later in Section 6.5.3. The VSCs are modeled as controllable voltage sources with their rms values being defined by equations (6.36) and (6.38) for the shunt converter, and (6.37) and (6.39) for the series converter. The variables m_{sh}, m_{se}, α and β are outputs from the UPFC control blocks implemented in TACS, whereas the reference variable, i.e., the sending-end bus voltage is tracked by using the Fourier filter discussed in Section 3.3.2. The UPFC fundamental frequency model as simulated in the EMTP is shown in Figure 6.3.

The UPFC transient stability model of Figure 6.3 can be represented with the following set of DAEs:

$$\begin{bmatrix}\dot{x}_{c1}\\ \dot{x}_{c2}\end{bmatrix} = f_c\begin{pmatrix}x_{c1}, x_{c2}, \alpha, \beta, m_{sh}, m_{se}, V_{sh}, V_{se},\\ V_{dc}, V_{dc,ref}, V_{s,ref}, P_{r,ref}, Q_{r,ref}\end{pmatrix} \quad (6.43)$$

$$\frac{dV_{dc}}{dt} = \frac{3\,k\,a_{sh}m_{sh}V_s}{C\,X_{sh}}\sin\alpha - \frac{3\;V_{SR}\;I_{line}}{C\,V_{dc}}\cos(\delta_{SR} - \Theta_{line}) - \frac{V_{dc}}{R_cC} \quad (6.44)$$

$$0 = \begin{bmatrix} P_{sh} + \dfrac{3\,k\,a_{sh} m_{sh} V_{dc} V_s}{X_{sh}} \sin\alpha \\ Q_{sh} + \dfrac{V_s^2}{X_{sh}} - \dfrac{3\,k\,a_{sh} m_{sh} V_{dc} V_s}{X_{sh}} \cos\alpha \\ P_{se} + \dfrac{3\,k\,a_{se} m_{se} V_{dc} V_{SR}}{X_{se}} \sin(\delta_{SR} - \delta_s - \beta) \\ Q_{se} + \dfrac{V_{SR}^2}{X_{se}} - \dfrac{3\,k\,a_{se} m_{se} V_{dc} V_{SR}}{X_{se}} \cos(\delta_{SR} - \delta_s - \beta) \end{bmatrix} \tag{6.45}$$

$$0 = \begin{bmatrix} P_s - P_{sh} - V_s\, I_{line} \cos(\delta_s - \Theta_{line}) \\ Q_s - Q_{sh} - V_s\, I_{line} \sin(\delta_s - \Theta_{line}) \\ P_r - V_m I_{line} \cos(\delta_m - \Theta_{line}) \\ Q_r - V_m I_{line} \sin(\delta_m - \Theta_{line}) \\ P_s - P_r - P_{sh} - P_{se} \\ Q_s - Q_r - Q_{sh} - Q_{se} \end{bmatrix} \tag{6.46}$$

$$0 = \begin{bmatrix} P_s - V_s\, I_s \cos(\delta_s - \Theta_s) \\ Q_s - V_s\, I_s \sin(\delta_s - \Theta_s) \end{bmatrix} \tag{6.47}$$

Most of the variables used in these equations have been previously defined and are clearly depicted in Figure 6.3. The variables x_{c1} and x_{c2} stand for the control variables of the shunt and series converters (e.g. α in Figure 6.3), whereas the control system equations are represented by $f_c(\cdot)$, which may be linear or nonlinear control equations depending on the specific control system.

The nonlinear differential equation (6.44) describes the dc voltage changes. Algebraic equations (6.45) describe the shunt and series converter power equations, and equation (6.46) and (6.47) represent the different relationships between the various system powers and the bus voltages and line current.

6.4.2 UPFC Steady State Model

The PWM-based UPFC steady state model can be readily derived from equations (6.43) to (6.47). The steady state control variables and equations get reduced to

$$0 = \begin{bmatrix} V_s - V_{s,ref} \pm X_{SL}\, I_{sh} \\ V_{dc} - V_{dc,ref} \\ P_r - P_{r,ref} \\ Q_r - Q_{r,ref} \end{bmatrix} \tag{6.48}$$

The equation (6.41) in steady state can be written as:

$$0 = P_{sh} - P_{se} - \frac{V^2_{dc}}{R_c} \tag{6.49}$$

$$0 = \frac{3\,k\,a_{sh} m_{sh} V_s}{C\,X_{sh}} \sin\alpha - \frac{3\,V_{SR}\;I_{line}}{C\,V_{dc}} \cos(\delta_{SR} - \Theta_{line}) - \frac{V_{dc}}{R_c C} \tag{6.50}$$

Equations (6.45), (6.46), and (6.47) are also part of the steady state model and they remain unchanged.

It is important to properly introduce the controller limits into this model. To define these limits, the actual current limits in both converters and any other physical limits, such as limits on the power transfer between two converters and the series voltage, have to be considered. Besides the actual physical limits, the relationships among the different variables as well as the available variables in the equations mathematically describing the particular model have to be taken into account.

6.5 EMTP Time-Domain Simulation Results

To validate the proposed fundamental frequency models for the STATCOM, SSSC and UPFC, they are incorporated in the EMTP and tested in various power system scenarios. The power system is subjected to different perturbations to simulate both detailed and transient stability models of the controllers under similar operating conditions. The detailed models include all necessary elements needed to model the controllers, including the full representation of the their control systems together with the control blocks for the valve switching logic, as previously explained in Chapter 3, 4, and 5.

The fundamental frequency models or reduced models should also capture the transient behaviour of the controllers in a full detail in typical stability studies. They are also suitable for control system design, since the models include all control blocks used in a detail controller analysis, except for the valve switching logic. The models, explained earlier in this chapter, are made of controllable voltage sources connected to the ac system through appropriate coupling transformers. The coupling transformers have different structure than the ones in the detailed models, as there is no need for intermediate transformers, but have the same MVA rating and leakage reactance. Since the transformers are modelled without saturation, they are not suitable for the converter harmonic analysis; it is known that the harmonic spectra can be transferred from the ac side to the dc side of the converter having as a consequence possible saturation of the coupling transformer. However, the transformer saturation curve can be easily incorporated in the reduced models for other type of analyses if a detailed model of the transformer is included.

It should be also mentioned that the detailed and reduced models have different time responses as there is some additional "damping" in the detailed model response due to the switching of the valves. To present this time delay in the detailed model responses, a transfer function $1/(1+sT_C)$ with converter time constant T_C is introduced in the reduced models, immediately before the control outputs, i.e., α, β, m_{sh} or m_{se}

The reduced models are fundamental frequency models and, therefore, suitable for power system analyses where the frequency excursions are not larger than 2 –3 Hz. They assume a symmetrical and balanced power system voltages and currents, and as such can only be used in analyses such as three-phase fault studies. The reduced models can be also used in other quasi-steady state stability studies such as voltage stability studies, as the operating and control limits of the controllers are represented in the model in full detail.

The STATCOM, SSSC and UPFC reduced models are introduced in the same test systems used earlier for the detailed model analyses. The reduced models have the same rating as the detail models and are placed at the exact same locations. The following cases are studied on these test systems:

1. The load at the end of the lower ac branch is increased in three steps until reaching full load.

2. A three-phase fault through fault impedance is placed at Bus 6, which is in a close proximity to the controllers.

It should be mentioned that although start-up mechanisms could be devised based on the different control strategies, no particular start-up strategy is used here. For example, in practice the STATCOM start-up sequence consists of several steps, starting with connecting the controller to the ac system through the circuit breaker but with the GTO valves blocked to allow the dc bus voltage to built up to the desired value through the anti-parallel diodes; the GTO valves start switching only after the dc bus voltage reaches the reference value, but with STATCOM output current set to zero to avoid any possible stress on the VSCs. During that time the STATCOM is in a constant current control mode, mentioned in Chapter 3, and only later is switched to automatic voltage control.

The SSSC start-up sequence consists of several steps similar to the STATCOM start-up. Thus, the dc voltage is built up to the reference value through the anti-parallel diodes

and only then the mechanical breaker by-passing the series transformer is opened. The SSSC is placed in the constant voltage mode, i.e., inserts a fixed voltage in series with the transmission line, ramping up from zero to the reference value. The SSSC is later switched to constant power or current control.

The UPFC start-up procedure is basically the start-up sequence for the STATCOM and SSSC together, and only then the flow of real power from the shunt to the series converter is allowed.

The actual start-up sequence, although possible to be modeled in the EMTP detailed representation, was not incorporated into the simulation. Instead, the dc voltage in the STATCOM, SSSC, or UPFC is allowed to build-up using the EMTP initialization process. Hence, a start-up delay of 4 s is incorporated to allow the power system variables to reach their steady-state values; this delay is not shown in the results.

6.5.1 STATCOM Reduced and Detailed Model Results

The test system depicted in Figure 3.8 is used to test and validate the proposed STATCOM reduced models. The STATCOM is rated at 100 Mvar with the coupling transformer ration of 138 kV / 6 kV. The transformer resistance is assumed very small and therefore neglected, while the total leakage reactance was considered to be 14.5 %. The STATCOM is designed to control the voltage at Bus 8, and thus regulate the load bus voltage at Bus 10.

Load variations at 5 s and 6 s are simulated on Bus 10 to depict the behaviour of the reduced model in steady state, thus validating the proposed model for small voltage variations (less than 20 %), similar validation studies were presented in [51, 65]. It was shown that the reduced model was not very sensitive to the value of R_C, due to the small voltage variations. An initial dc voltage of 8 kV in the reduced model was chosen, so that the initial value of the control output angle α is reached; an appropriate converter

time constant T_C is chosen to match the time response of both detailed and reduced models during the dynamic process at 5 s and 6 s. Figure 6.5 depicts the system behaviour for both detailed and reduced models. Both models show adequate voltage regulation and rather similar dynamic responses, even for the internal variables V_{dc} and α.

To validate and test the limits of the proposed reduced model for large system disturbances, a severe three-phase fault through a small fault impedance is applied at 4.5 s at Bus 6, and then removed at 4.65 s by tripping the corresponding transmission line. The results of this classical transient stability study are depicted in Figure 6.5. In this case, even for the large voltage and angles variations, both STATCOM models show very similar results. It is noticeable that during the fault, there is a small difference in the results, as it would be expected, since the voltage and currents tend to deviate from the sinusoidal shapes due to irregular switching; similar behaviour is observed in fundamental frequency models of HVDC systems [75]. These results basically validate the STATCOM proposed reduced model.

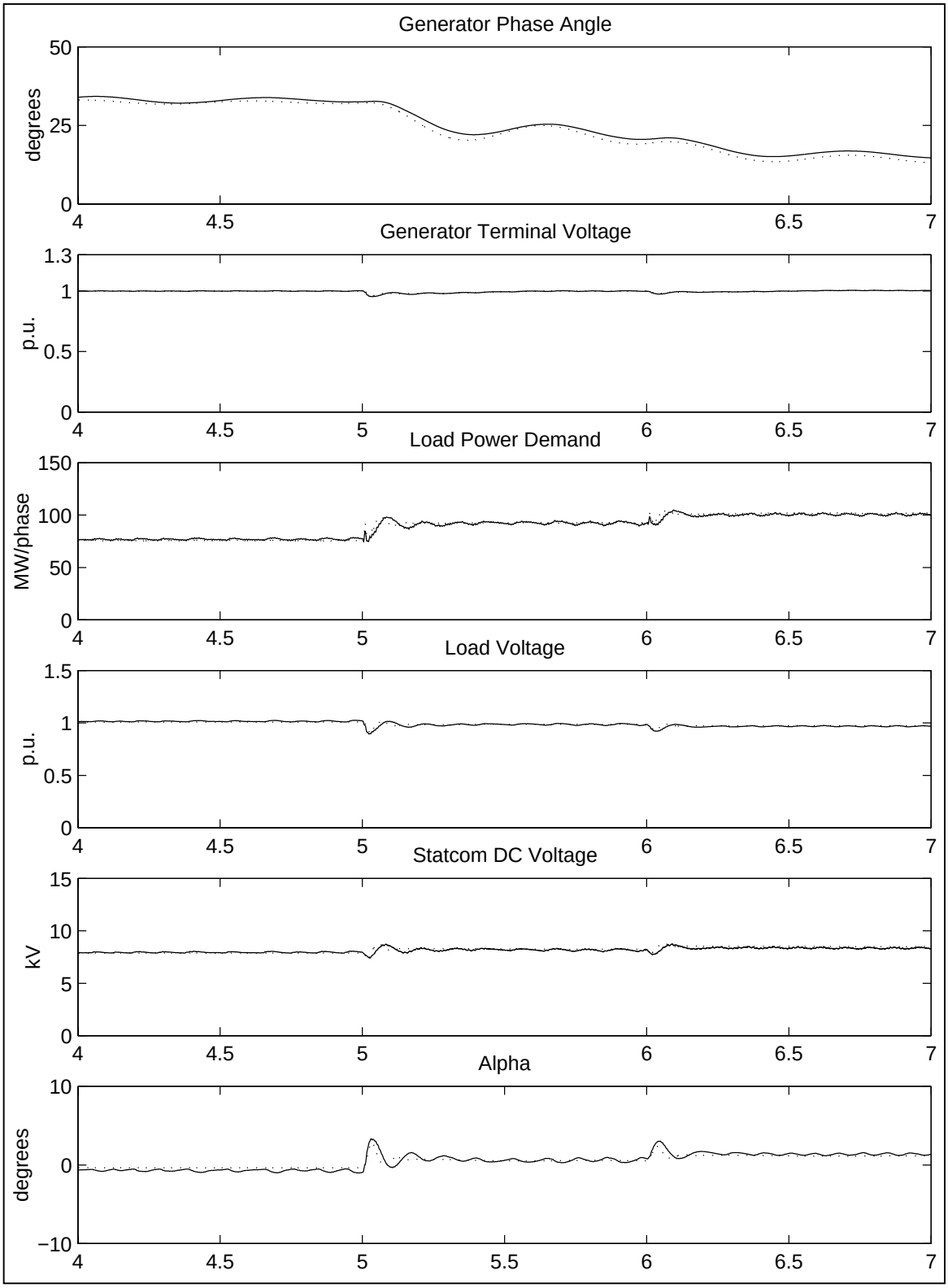


Figure 6.4 – Load variation results with a phase-controlled STATCOM.

Key: ── detailed model, ┈┈ reduced model

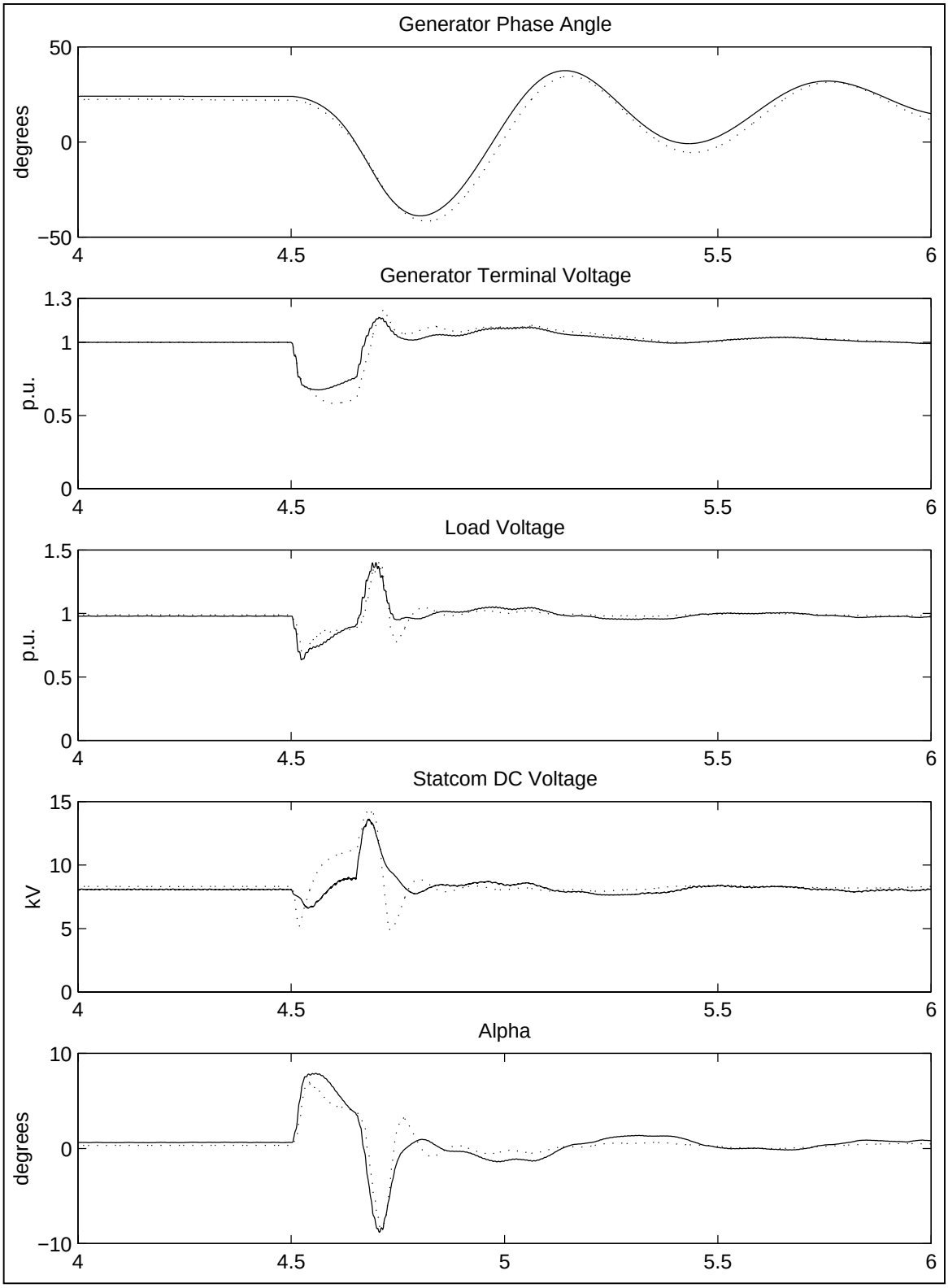


Figure 6.5 –Three-phase fault results with a phase-controlled STATCOM.

Key: ── detailed model, ····· reduced model

6.5.2 SSSC Reduced and Detailed Model Results

The test system shown in Figure 4.6 and used in the tests and simulation of the SSSC detailed model is used again here. The reduced SSSC model is rated at 70 Mvar 30 kV as the detailed SSSC model, and placed at the lower ac parallel line to regulate the transmission line current. To illustrate performance of both the SSSC detailed and reduced models with small system perturbations, load variations at 5 s and 6 s are simulated again at Bus 10. Figure 6.6 illustrates the generator voltage regulation and its internal angle variations, as well as the p.u. rms currents on both parallel lines. Both models show almost identical results.

The results of applying an identical three-phase fault to the test system as in the case of the test system with the SSSC are shown in Figure 6.7. Once again, the results show very similar results for the reduced and detailed models, validating the proposed reduced model.

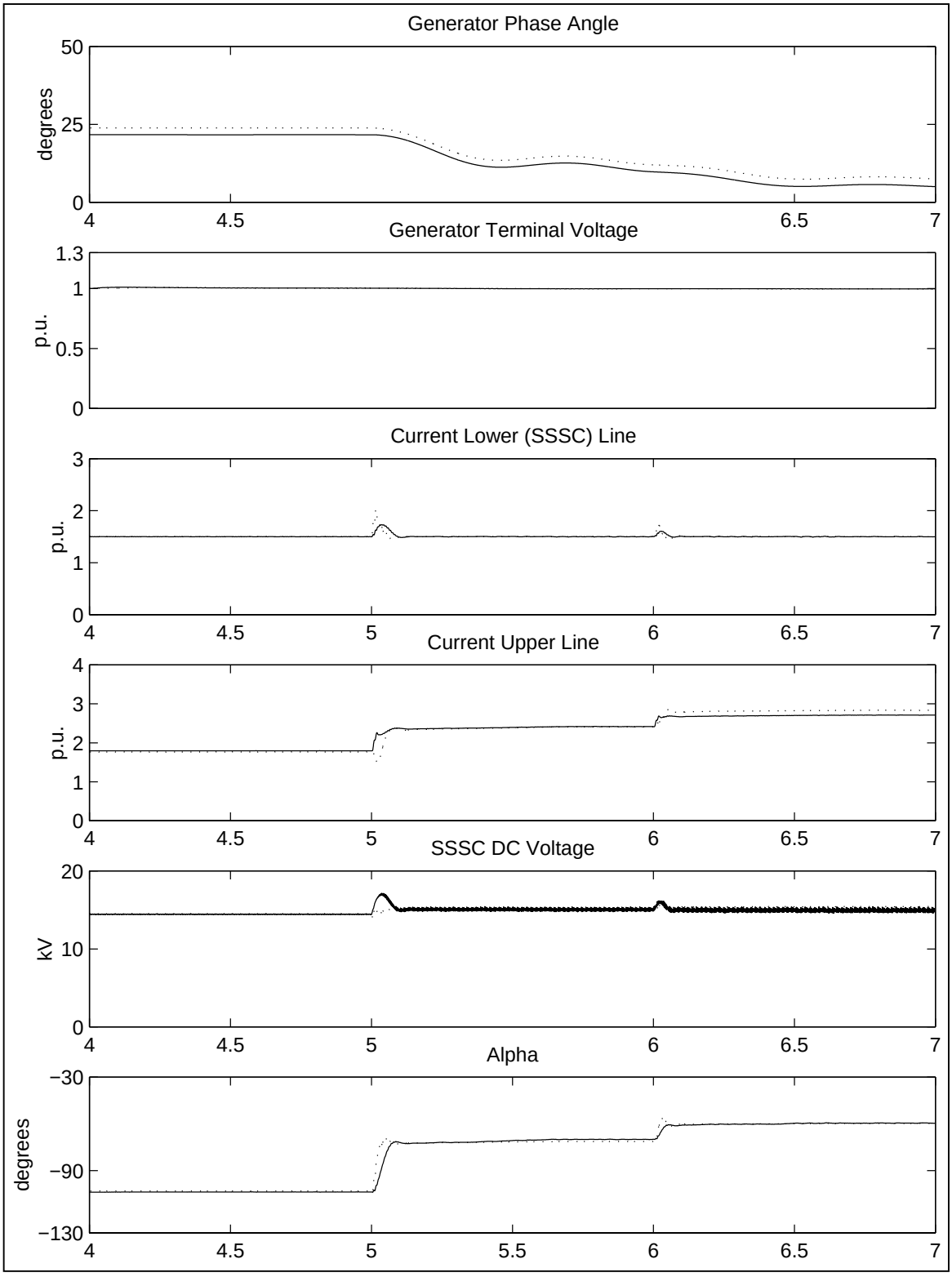


Figure 6.6 – Load variation results with a phase-controlled SSSC.

Key: ── detailed model, ┈┈ reduced model

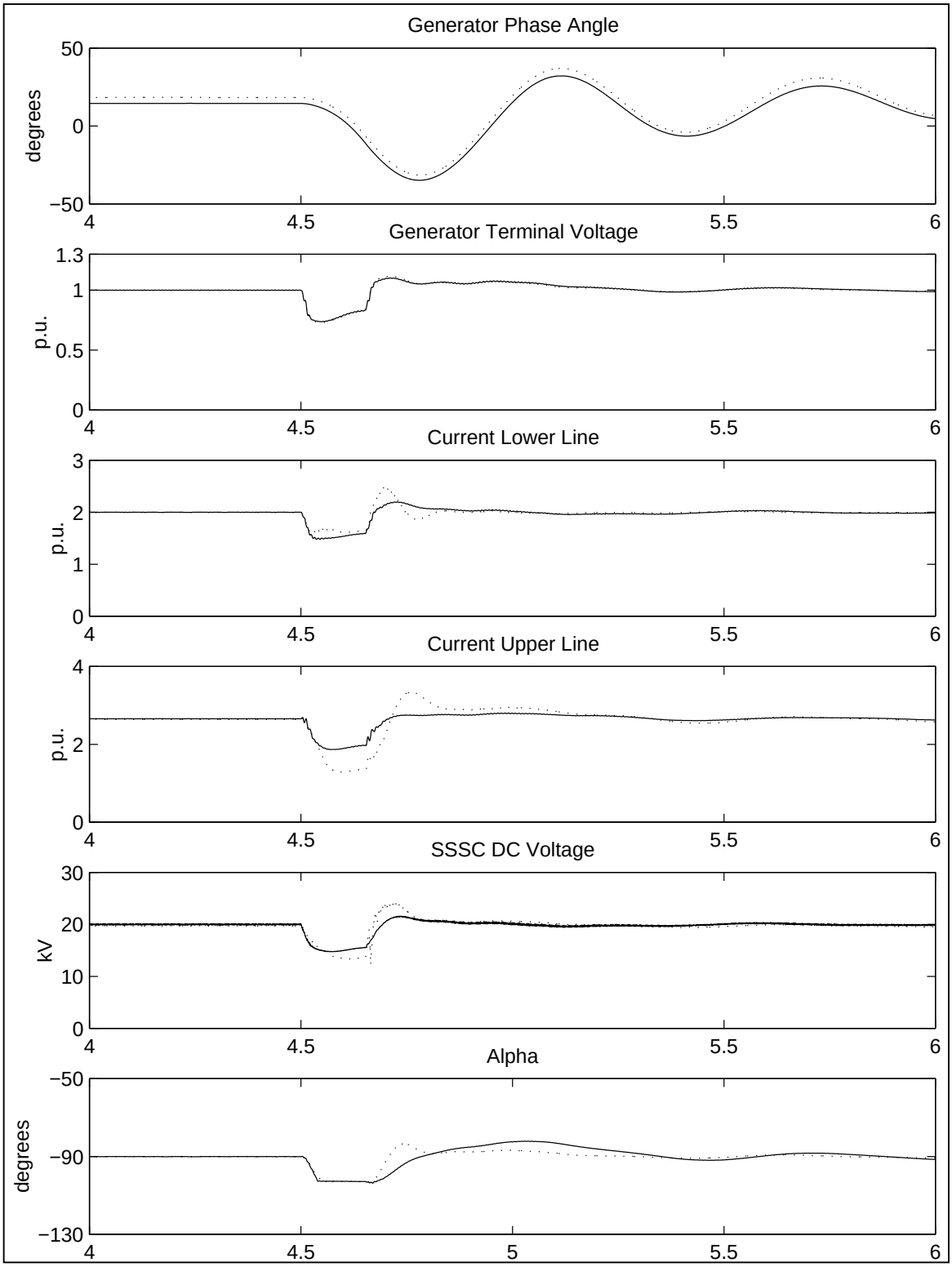


Figure 6.7 – Three-phase fault results with a phase-controlled SSSC.

Key: ── detailed model, ····· reduced model

6.5.3 UPFC Reduced and Detailed Model Results

Load variations at 5 s and 6 s are simulated in the test system presented in Chapter 5, Figure 5.3 to compare the behaviour of the UPFC detailed and fundamental frequency models, and to validate the proposed reduced model for small disturbance stability analysis. A relatively large start-up time of 4 s was chosen to let initial transients die down, so that better comparison between the two models can be carried out, as the start-up processes on both models are fairly distinct due to the significant modeling differences.

The UPFC shunt converter is designed to keep the sending-end voltage at 1.0 p.u., whereas the dc voltage is kept at 22 kV. The series inverter varies the magnitude and phase of its output voltage to maintain the real power on the transmission line at 70 MW/phase, and to keep the voltage magnitude at the receiving-end of the line at 0.97 p.u. The results obtained for both detailed and transient stability models are presented in Figures 6.8 and 6.9. As it can be observed, both models present similar trends. It is interesting to notice that the UPFC, due to tight voltage regulation at the sending and receiving-ends, works as a phase shifter introducing a series inserted voltage of appropriate phase angle between the two ends of the line.

To simplify the calculations, all converter losses were concentrated on the dc resistance R_C, and the ac resistors were neglected, which should not introduce significant errors in the simulations. The actual value of the dc resistor can be computed from the steady-state equation (6.50), based on a steady-state point obtained from the detailed simulations. When the operating point obtained by the detailed model calculation is not available, the dc resistance should be calculated based on the fact that these resistive losses should be equal to some already predicted losses that depend on the valve structure.

The difference between the responses tends to be more pronounced in the area of increased power flow (see Figure 6.9) due to the fact that the converter losses change for

different steady state operating points; hence, it is necessary to compute different value of R_C for each load setting or operating point. However, for many study purposes, the discrepancies may be acceptable.

A 3-phase fault through an impedance is applied at Bus 6 at 4 s for full loading conditions in the test system. Nine cycles after the fault, the circuit breaker between Buses 4 and 5 is opened, clearing the fault and disconnecting the load at Bus 7. The generator at Bus 3, which has an AVR to keep its terminal voltage at 1.0 p.u., recovers successfully after the fault, as it can been seen from the corresponding waveforms in Figure 6.10. The series converter continues to control real power and voltage magnitude at the receiving-end using the same control scheme used in all previous simulations. The series voltage magnitude and dc voltage, as well as the control outputs are shown in Figure 6.11.

The results for the two models do not reveal large differences. Even during the fault period the responses of the detailed and reduced models are almost identical, showing that the reduced model can be successfully used for stability analyses.

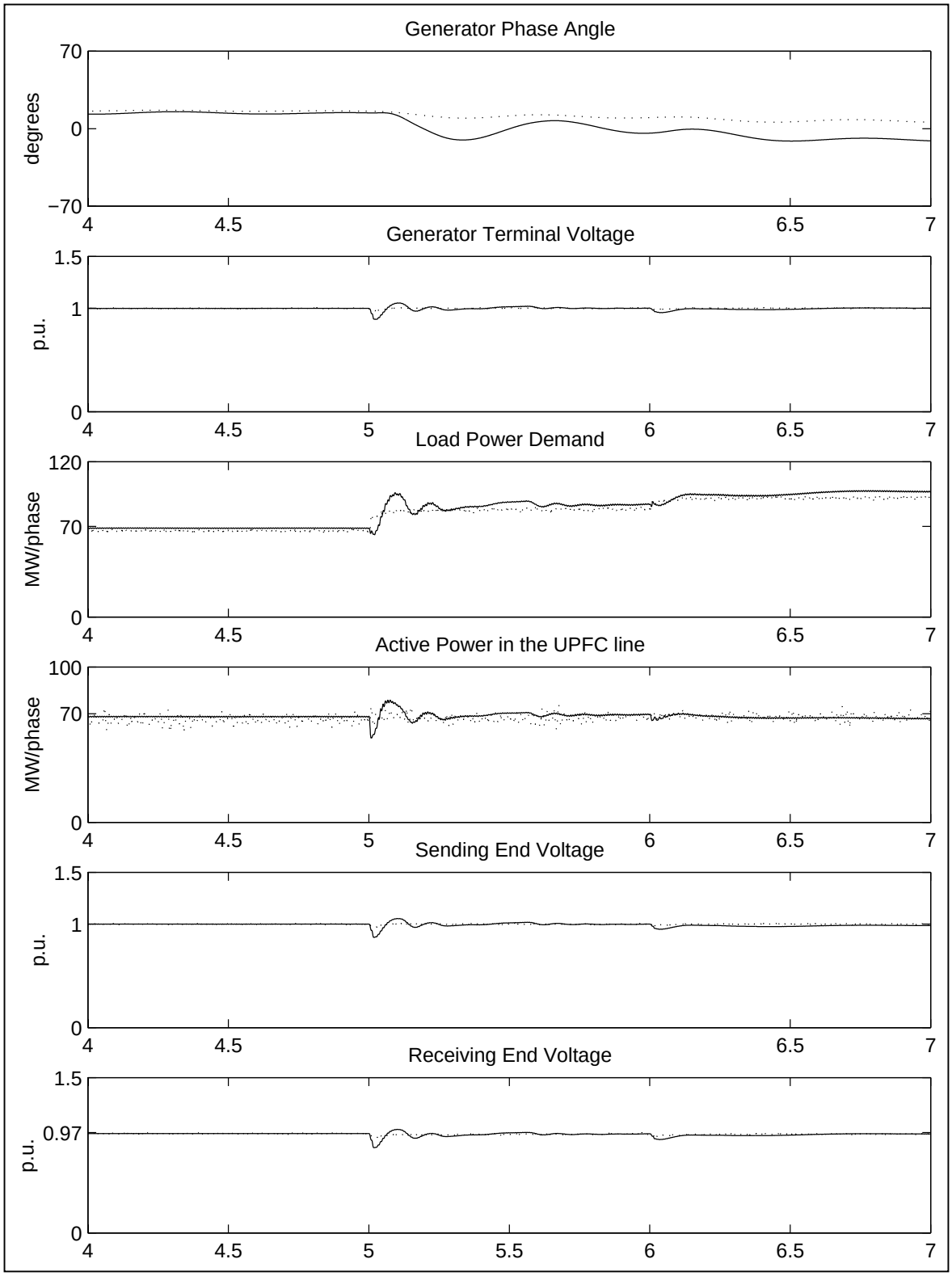


Figure 6.8 – Load variation results with a PWM-controlled UPFC.

Key: ── detailed model, ┈┈ reduced model

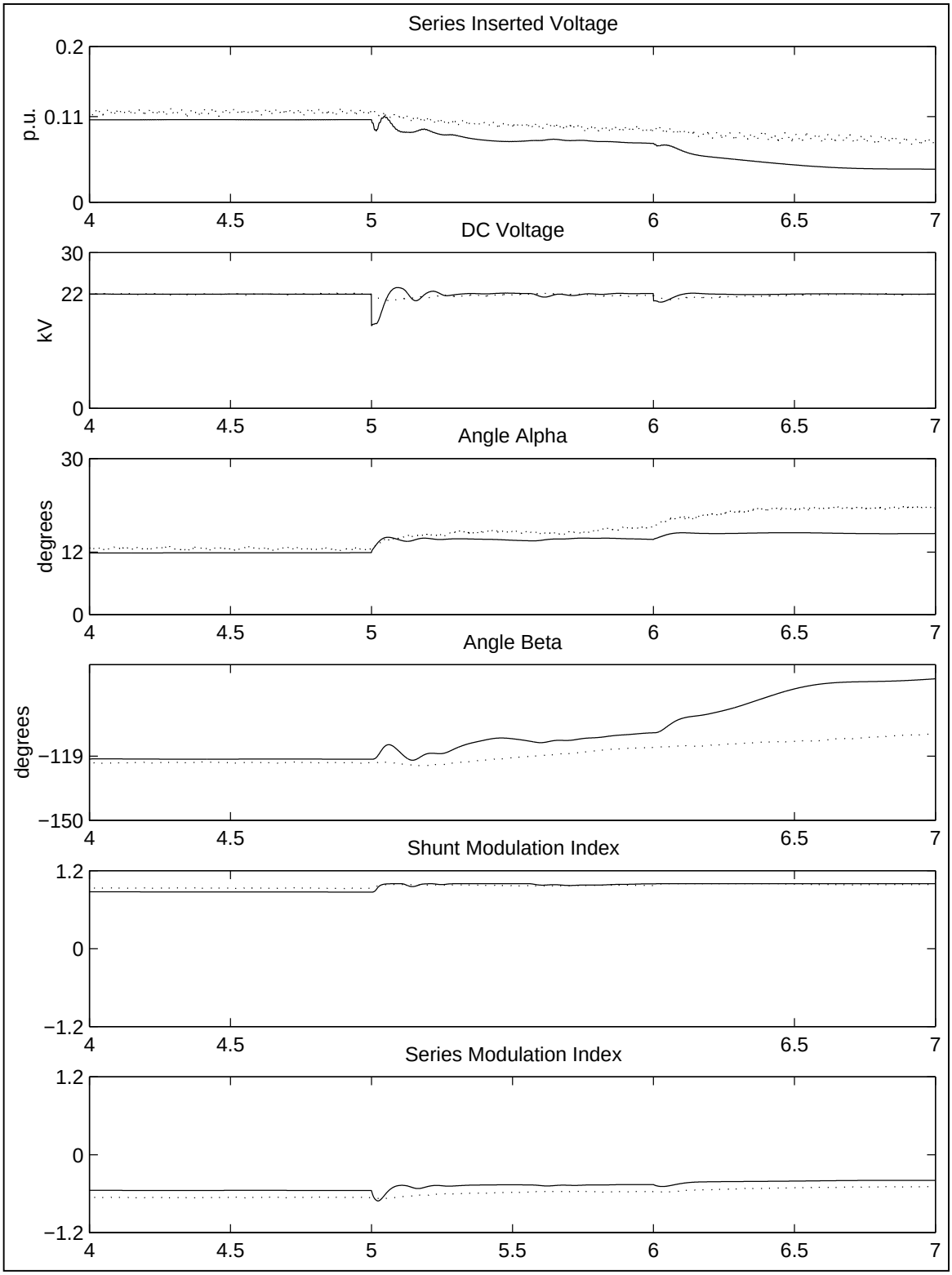


Figure 6.9 – Load variation results with a PWM-controlled UPFC.

Key: ── detailed model, ┈┈ reduced model

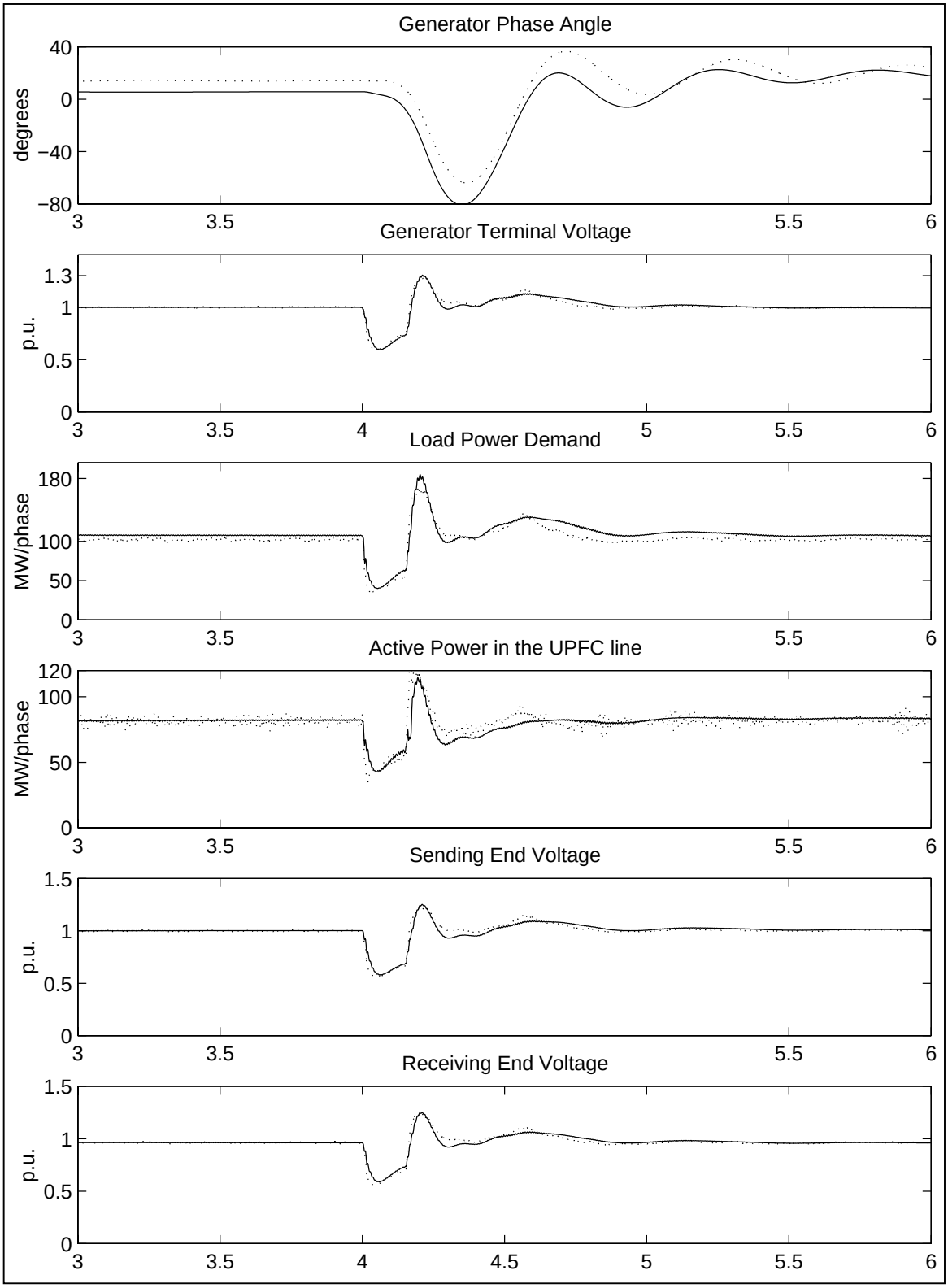


Figure 6.10 – Three-phase fault results with a PWM-controlled UPFC.

Key: ── detailed model, ┈┈ reduced model

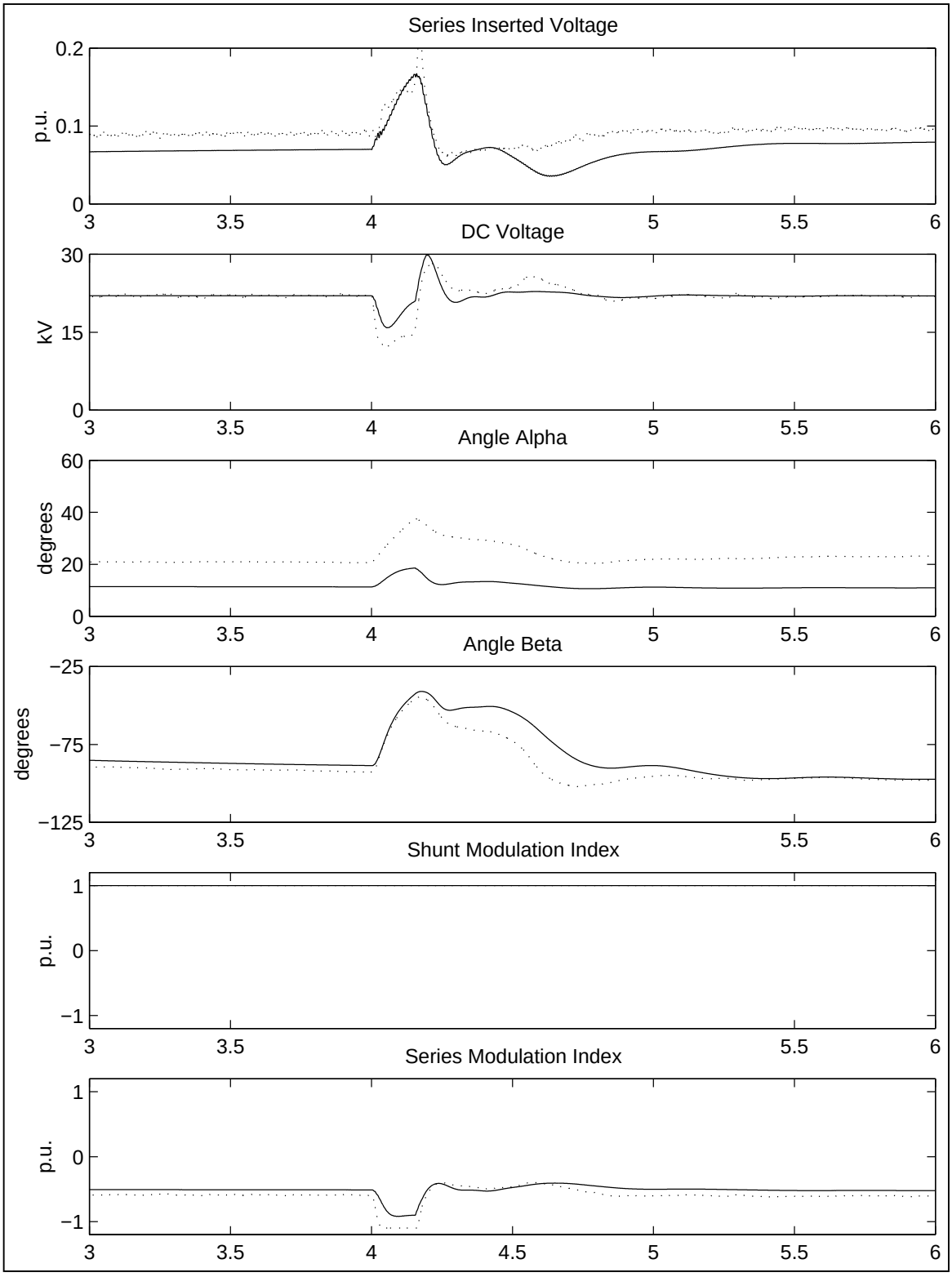


Figure 6.11 – Three-phase fault results with a PWM UPFC.

Key: ── detailed model, ┈┈ reduced model

6.6 Summary

This chapter proposes and justifies novel and complete transient stability and steady-state models for the STATCOM, SSSC, and UPFC. The models are successfully validated by obtaining matching results in the EMTP at various realistic operating conditions of a test system for both reduced and detailed models of the controller.

The proposed models can be directly implemented in any software package that has some external programming capabilities, or can be readily integrated in any power flow, voltage stability, and/or transient stability programs. It should be noted that the model is independent of the type of control used in any of these controllers. The results for the STATCOM and SSSC are based on a phase control scheme, while for the UPFC model the results were obtained for a PWM-based control technique.

The proposed models include and properly represent the ac as well as dc side of all controllers, so that operating and control limits can be properly represented in these models. The models can be used in balanced and fundamental frequency studies of power system, such as steady state, small signal, voltage and transient stability analyses.

Chapter 7.

CONCLUSIONS

7.1 Summary of Main Results

In this thesis, two-level force-commutated voltage-sourced converters for power system applications have been studied by examining the STATCOM, SSSC, and UPFC controller applications. A brief introduction to FACTS controllers is given in Chapter 1. Chapter 2 explains the fundamentals of forced-commutated VSCs, with emphasis on high power applications. Also, the basic operating principles of the phase controlled and PWM-based VSCs are given in this Chapter.

The general concepts of shunt compensation and the STATCOM power system application are given in Chapter 3. The 12-pulse and PWM-based STATCOMs are successfully modeled in the EMTP, including a detailed representation of the valves and the snubber circuits. The presented time-domain simulations verify the adequate STATCOM operation, demonstrating successful operation of two kind controllers, i.e., PWM and phase controllers. Also, a brief comparison of the STATCOM and SVC performances is given in Chapter 3.

The general concepts of series compensation and the theory of operation and basic equations of a SSSC are described in Chapter 4. The SSSC operating conditions and constraints are compared to the operating condition of a TCSC, showing that the SSSC offers several advantages over the TCSC. The detailed models of the 12-pulse and PWM-based SSSCs are implemented in the EMTP and their successful operation is verified in realistic power system application.

Chapter 5 presents the fundamentals of a UPFC application, explaining in detail the operating principles and limits as well as practical ratings of the equipment. The UPFC

detailed model is implemented in the EMTP using the sinusoidal PWM-based control system. The UPFC operation is verified in the realistic test system and various credible power system scenarios.

Chapter 6 proposes and explains in detail novel transient stability and steady state models for the STATCOM, SSSC and UPFC. The models are successfully validated in the EMTP at various realistic operating conditions.

7.2 Contributions

The main contributions of this thesis are summarized below:

- The detailed models of the STATCOM, SSSC, and UPFC were implemented and tested in the EMTP. These models include a detailed representation of the valves and the snubber circuits, as well as the full control circuit representation. The models are applicable for transient stability analysis, and cover broader range of frequency oscillations, and are also suitable for simulations in unbalanced power conditions.

- Two kinds of controllers, i.e. phase-controlled and PWM-based, are successfully implemented for the STATCOM and SSSC. Both control strategies are based on direct manipulations of the control variables rather then using a d-q decomposition to separate active and reactive components, which is the usual implementation in most of today's controls. It has been also shown that classical and simple PI controllers are suitable for the controller designs.

- The UPFC PWM-based control circuit has been designed and implemented in the EMTP. It has been shown that the UPFC control decoupling is possible and even desirable due to its simplicity and consequent price reduction. Three different control schemes for the series converter in the UPFC configuration, together with a novel approach of directly controlling the receiving-end voltage, have been described and

evaluated. The presented time-domain simulations in EMTP, together with the theoretical evaluation, validate the proposed control design.

- It has been shown that the UPFC can be used to successfully damp power oscillation caused by a nearby fault. The additional damping control circuit has been designed and verified in the EMTP simulation.

- This thesis proposes and justifies novel transient stability and steady state models for the STATCOM, SSSC, and UPFC. The models are successfully validated in the EMTP for various operating conditions and in a realistic test system. The proposed models can be directly implemented in any power software package that has some external programming capabilities, or can be readily integrated in power flow, voltage stability, and transient stability programs.

- The proposed models are independent of the type control used, and they include and properly represent ac and dc sides of the VSCs, with operating and control limits being included in the models.

7.3 Future Work

The future work should include introduction of the developed transient and steady state models to eigenvalue, voltage, transient stability and power flow programs, respectively. The models should be further used in stability studies for planning and operation of actual power systems.

Appendix A

Mathematical α–β and d-q transformations

A.1 Background

In the late 1920s, R. H. Park introduced a new approach to electric machine analysis, where the stator variables were referred to a frame of reference fixed in a synchronous machine rotor. Park's transformation eliminated time-varying inductances from the voltage equations of the synchronous machine, which in turn simplified synchronous machine analyses and calculations [70].

Park's transformation initiated a new way of dealing with time-varying variables, and these were later introduced to induction machine analysis by H. C. Stanley [71]. Today, general transformation techniques based on the Park's transformation are being used for different types of power system studies [45].

A.2 General Transformation

Although changes to variables was first introduced in the analysis of ac machines to eliminate time-varying inductances, changes of variables are also employed in the analysis of various static, constant parameter power system components. Thus, the variables associated with the transformers, transmission lines, loads, capacitor banks, etc., can be transformed to a synchronous rotating reference frame.

A set of three instantaneous phase variables can be uniquely represented by a single point in a plane if their sum is equal to zero. Thus, sinusoidal variable y(t) can be described as:

$$y(t) = \hat{Y}\cos(\omega t + \varphi) = \frac{1}{2}(\hat{Y} \cdot e^{j(\omega t+\varphi)} + \hat{Y} \cdot (e^{j(\omega t+\varphi)})^{*}) \qquad (A.1)$$

If the complex vector is set to be

$$\bar{y}(t) = \hat{Y} \cdot e^{j(\omega t+\varphi)} \tag{A.2}$$

then the three-phase sinusoidal quantities can be represented by a single complex vector. The complex vector for three-phase quantities, denoted by $\bar{f}(t)$, is chosen such that the projection of the vector in three directions e^{j0}, $e^{-j\frac{2\pi}{3}}$ and $e^{j\frac{2\pi}{3}}$ give the three-phase instantaneous variables $f_a(t)$, $f_b(t)$ and $f_c(t)$. Thus,

$$f_a(t) = \Re(\bar{f}(t) \cdot (e^{j0})) = \frac{1}{2}(\bar{f}(t) \cdot (e^{j0}) + \bar{f}(t)^* \cdot (e^{j0})^*) \tag{A.3a}$$

$$f_b(t) = \Re(\bar{f}(t) \cdot (e^{-j\frac{2\pi}{3}})) = \frac{1}{2}(\bar{f}(t) \cdot (e^{-j\frac{2\pi}{3}}) + \bar{f}(t)^* \cdot (e^{-j\frac{2\pi}{3}})^*) \tag{A.3b}$$

$$f_c(t) = \Re(\bar{f}(t) \cdot (e^{j\frac{2\pi}{3}})) = \frac{1}{2}(\bar{f}(t) \cdot (e^{j\frac{2\pi}{3}}) + \bar{f}(t)^* \cdot (e^{j\frac{2\pi}{3}})^*) \tag{A.3c}$$

Manipulating (A.3) gives, it is possible to obtain

$$\begin{aligned} & f_a(t) + f_b(t) \cdot e^{j\frac{2\pi}{3}} + f_c(t) \cdot e^{-j\frac{2\pi}{3}} = \\ & = \frac{1}{2}\left\{\left[(\bar{f}(t) + \bar{f}(t)^*\right] + \left[(\bar{f}(t) + \bar{f}(t)^* \cdot e^{j\frac{4\pi}{3}}\right] + \left[(\bar{f}(t) + \bar{f}(t)^* \cdot e^{-j\frac{4\pi}{3}}\right]\right\} = \\ & = \frac{1}{2} \cdot 3 \cdot \bar{f}(t) \end{aligned} \tag{A.4}$$

Therefore, a complex vector can be calculated from the three-phase instantaneous quantities as follows:

$$\bar{f}(t) = \overline{K}\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{A.5}$$

where

$$\overline{K} = \frac{2}{3}\begin{bmatrix} 1 & e^{j\frac{2\pi}{3}} & e^{-j\frac{2\pi}{3}} \end{bmatrix} \tag{A.6}$$

It is possible to define a three-phase system using symmetrical components, i.e., positive, negative, and zero sequence components. Thus,

$$\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} = F_p\begin{bmatrix} \cos(\omega t + \varphi_p) \\ \cos(\omega t + \varphi_p - \frac{2\pi}{3}) \\ \cos(\omega t + \varphi_p + \frac{2\pi}{3}) \end{bmatrix} + F_n\begin{bmatrix} \cos(\omega t + \varphi_p) \\ \cos(\omega t + \varphi_p + \frac{2\pi}{3}) \\ \cos(\omega t + \varphi_p - \frac{2\pi}{3}) \end{bmatrix} + F_o\begin{bmatrix} \cos(\omega t + \varphi_o) \\ \cos(\omega t + \varphi_o) \\ \cos(\omega t + \varphi_o) \end{bmatrix} \tag{A.7}$$

Multiplying equation (A.7) by $\overline{K}$ yields

$$\bar{f} = F_p \cdot e^{+j\omega t} + F_n \cdot e^{-j\omega t} + 0 \tag{A.8}$$

Equation (A.8) shows that the vector will rotate anticlockwise with a constant amplitude and angular velocity ω, if the three-phase variables contain only the positive sequence fundamental frequency component. Figure A.1 illustrates the vector with only positive sequence.

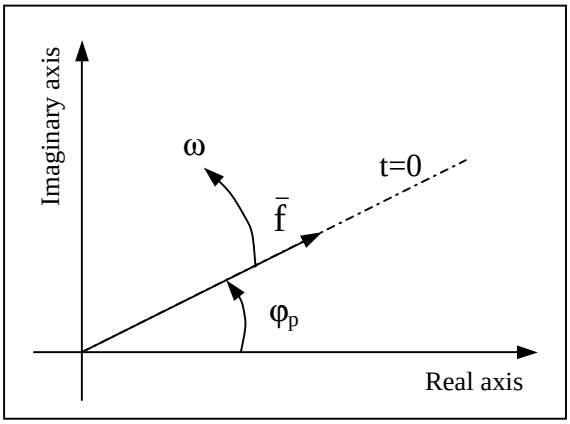


Figure A.1 – Representation of a complex vector with only positive sequence component in the Cartesian plane

The vector will rotate clockwise with constant amplitude and angular velocity ω, if the three-phase variables contain only the negative sequence fundamental frequency component. If the three phase variables are unbalanced with both positive and negative sequence components, the vector will be as illustrated in Figure A.2. If the three-phase quantities are of zero sequence, the resulted complex vector will be equal to zero.

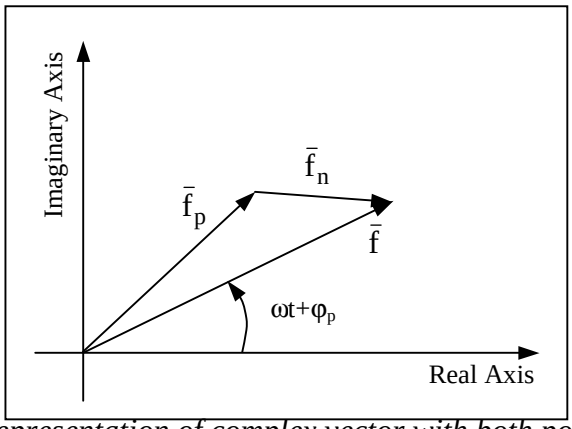


Figure A.2 – Representation of complex vector with both positive and negative sequence component in the Cartesian plane

A.3 ds,qs Components and dq Components

The ds and qs components are defined as the real and imaginary parts of the complex vector $\bar{f}(t)$, respectively, i.e.,

$$\bar{f}_{ds,qs}(t) \equiv \bar{f}(t) = f_{ds}(t) + j \cdot f_{qs}(t) \tag{A.9}$$

The transformation matrix from phase variables to ds,qs coordinates is as follows:

$$[T] = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.10}$$

and the ds, qs coordinates can be calculated as follows:

$$\begin{bmatrix} f_{ds} \\ f_{qs} \\ 0 \end{bmatrix} = [T] \begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{A.11}$$

The total instantaneous power may be then expressed in abc variables as

$$P_{abc} = v_a i_a + v_b i_b + v_c i_c = \frac{3}{2}\Re(\bar{v}(t) \cdot \bar{i}^*(t)) \tag{A.12}$$

The total power expressed in the qs,ds variables must equal the total power expressed in the abc variables, i.e.,

$$P_{ds,qs} = P_{abc} = \frac{3}{2}(v_{qs}i_{qs} + v_{ds}i_{ds}) \tag{A.13}$$

where v_{ds}, v_{qs}, i_{ds}, and i_{qs} are calculated according to the previously described transformation. The $3/2$ factor comes about due to the choice of the constant used in the transformation. Although the waveforms of the ds and qs voltages, currents, etc., are dependent upon the angular velocity of the frame of reference, the waveform of the total power is independent of this frame. The waveform of the total power is the same regardless of the reference frame in which is evaluated.

All the quantities defined above are described in the static reference frame, i.e., the Cartesian plane. If a rotating reference frame, which synchronously rotates with a vector, is used, the so-called dq-components can be obtained.

$$\bar{f}_{dq}(t) \equiv f_d(t) + j \cdot f_q(t) = \bar{f}_{ds,qs}(t) \cdot e^{-j\omega t} \tag{A.14}$$

where

$$f_d(t) = f_{ds}(t) \cdot \cos(\omega t) + f_{qs}(t) \cdot \sin(\omega t) \tag{A.15}$$

$$f_q(t) = -f_{ds}(t) \cdot \sin(\omega t) + f_{qs}(t) \cdot \cos(\omega t) \tag{A.16}$$

A.4 Stationary Circuit Variables Transformed to the arbitrary Reference Frame

A.4.1 Resistive Elements

The voltage and current relationship for the resistance in dq frame is simply given by the following equations:

$$v_d(t) = R \cdot i_d(t) \tag{A.17}$$

$$v_q(t) = R \cdot i_q(t) \tag{A.18}$$

A.4.2 Inductive Elements

The voltage and current relationship for the inductance in dq frame is simply given by the following equations:

$$v_d(t) = L\frac{di_d(t)}{dt} - \omega L\, i_q(t) \tag{A.19}$$

$$v_q(t) = L\frac{di_q(t)}{dt} + \omega L\, i_d(t) \tag{A.20}$$

A.4.3 Capacitive Elements

The voltage and current relationship for the capacitance in dq frame is simply given by the following equations:

$$i_d(t) = C\frac{dv_d(t)}{dt} - \omega C\, v_q(t) \tag{A.21}$$

$$i_q(t) = C\frac{dv_q(t)}{dt} + \omega C\, v_d(t) \tag{A.22}$$

Appendix B

UPFC Modeling Using d-q- Transformation

The system shown in Figure B.1 can be described by the following equations, with voltages and currents in the d-q – coordinates (see Appendix A).

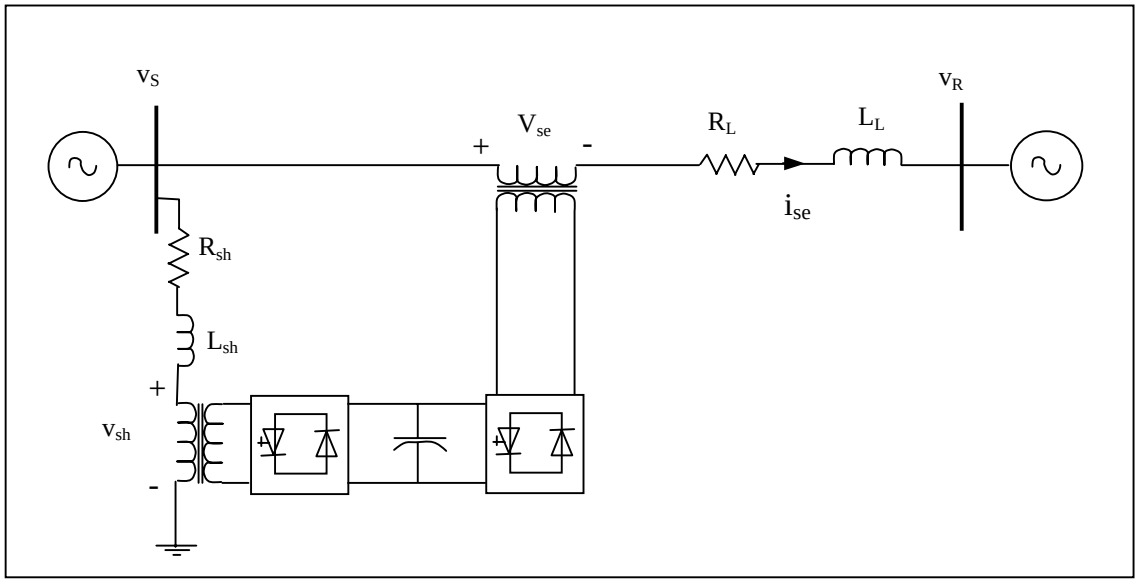


Figure B.1 – One line diagram of a two terminal system with a UPFC

Rsh and Rse represent the shunt and series transformer losses, respectively. Lsh and Lse represent the shunt and series transformer leakage inductances, respectively. The transmission line and series transformer parameters are included together, i.e. $R_{se}+R_{TL}=R_L$ and $L_{se}+L_{TL}=L_L$.

$$v_{sd} - v_{sed} - v_{rd} = L_L \frac{di_{sed}}{dt} - \omega L_L i_{seq} + R_L i_{sed} \qquad \text{(B.1)}$$

$$v_{sq} - v_{seq} - v_{rq} = L_L \frac{di_{seq}}{dt} + \omega L_L i_{sed} + R_L i_{seq} \qquad \text{(B.2)}$$

$$v_{sd} - v_{shd} = L_{sh}\frac{di_{shd}}{dt} - \omega L_{sh} i_{shq} + R_{sh} i_{shd} \tag{B.3}$$

$$v_{sq} - v_{shq} = L_{sh}\frac{di_{shq}}{dt} + \omega L_{sh} i_{shd} + R_{sh} i_{shq} \tag{B.4}$$

On the other hand, the active power balance equation states that:

$$p_{ac,shunt} + p_{ac,series} = p_{dc} \tag{B.5}$$

which in the d-q coordinates, can be written as:

$$\frac{3}{2}\left(i_{sed} v_{sed} + i_{seq} v_{seq} + i_{shd} v_{shd} + i_{shq} v_{shq}\right) = C v_{dc}\frac{dv_{dc}}{dt} \tag{B.6}$$

In steady state, i.e., $d/dt = 0$, and equations (B.1) through (B.6) become

$$v_{sdo} - v_{sedo} - v_{rdo} = -\omega L_L i_{seqo} + R_L i_{sedo} \tag{B.7}$$

$$v_{sqo} - v_{seqo} - v_{rqo} = \omega L_L i_{sedo} + R_L i_{seqo} \tag{B.8}$$

$$v_{sdo} - v_{shdo} = -\omega L_{sh} i_{shqo} + R_{sh} i_{shdo} \tag{B.9}$$

$$v_{sqo} - v_{shqo} = \omega L_{sh} i_{shdo} + R_{sh} i_{shqo} \tag{B.10}$$

$$\frac{3}{2}\left(i_{sedo} v_{sedo} + i_{seqo} v_{seqo} + i_{shdo} v_{shdo} + i_{shqo} v_{shqo}\right) = 0 \tag{B.11}$$

Equations for small disturbance stability analysis around a given operating point, can be written as follows by neglecting second order terms Δ^2 in (B.11):

$$\Delta v_{sd} - \Delta v_{sed} - \Delta v_{rd} = L_L\frac{d\Delta i_{sed}}{dt} - \omega L_L \Delta i_{seq} + R_L \Delta i_{sed} \tag{B.12}$$

$$\Delta v_{sq} - \Delta v_{seq} - \Delta v_{rq} = L_L \frac{d\Delta i_{seq}}{dt} + \omega L_L \Delta i_{sed} + R_L \Delta i_{seq} \tag{B.13}$$

$$\Delta v_{sd} - \Delta v_{shd} = L_{sh} \frac{d\Delta i_{shd}}{dt} - \omega L_{sh} \Delta i_{shq} + R_{sh} \Delta i_{shd} \tag{B.14}$$

$$\Delta v_{sq} - \Delta v_{shq} = L_{sh} \frac{d\Delta i_{shq}}{dt} + \omega L_{sh} \Delta i_{shd} + R_{sh} \Delta i_{shq} \tag{B.15}$$

$$\begin{aligned} \frac{3}{2}(\Delta i_{sed} v_{sedo} + i_{sedo} \Delta v_{sed} + \Delta i_{seq} v_{seqo} + i_{seqo} \Delta v_{seq} + \Delta i_{shd} v_{shdo} + \\ + i_{shdo} \Delta v_{shd} + \Delta i_{shq} v_{shqo} + i_{shqo} \Delta v_{shq}) = C v_{dco} \frac{d\Delta v_{dc}}{dt} \end{aligned} \tag{B.16}$$

Neglecting the voltage harmonic produced by the converter, and assuming that the phase shift angles between the reference voltage and the shunt v_{sh} and series converter output voltages v_{se} are α and β, respectively, the d-q components of the converter output voltages can be expressed as

$$v_{shd} = k_2 v_{dc} \cos(\alpha) \tag{B.17}$$

$$v_{shq} = k_2 v_{dc} \sin(\alpha) \tag{B.18}$$

$$v_{sed} = k_1 v_{dc} \cos(\beta) \tag{B.19}$$

$$v_{seq} = k_1 v_{dc} \sin(\beta) \tag{B.20}$$

where k_1 and k_2 represent factors that relate these voltage magnitudes to the dc voltage. In the case of small disturbances, equations (B.17) through (B.20) can be linearized as follows:

$$\Delta v_{shd} = k_2 \cos(\alpha_o) \Delta v_{dc} - k_2 v_{dco} \sin(\alpha_o) \Delta\alpha \tag{B.21}$$

$$\Delta v_{shq} = k_2 \sin(\alpha_o) \Delta v_{dc} + k_2 v_{dco} \cos(\alpha_o) \Delta\alpha \tag{B.22}$$

$$\Delta v_{sed} = k_1 \cos(\beta_o)\Delta v_{dc} - k_1 v_{dco} \sin(\beta_o)\Delta\beta \tag{B.23}$$

$$\Delta v_{seq} = k_1 \sin(\beta_o)\Delta v_{dc} + k_1 v_{dco} \cos(\beta_o)\Delta\beta \tag{B.24}$$

where the steady state angles α_o and β_o can be calculated as follows:

$$\alpha_o = \arctan\left(\frac{v_{shqo}}{v_{shdo}}\right) \tag{B.25}$$

$$\beta_o = \arctan\left(\frac{v_{seqo}}{v_{sedo}}\right) \tag{B.26}$$

For the following per-unit system:

$$i_x' = \frac{i_x}{i_B};\ v_x' = \frac{v_x}{v_B};\ v_{shx}' = \frac{v_{shx}}{v_B};\ v_{sex}' = \frac{v_{sex}}{v_B} \tag{B.27}$$

$$z_B = \frac{v_B}{i_B};\ L' = \frac{\omega_B L}{z_B};\ R' = \frac{R}{z_B};\ \frac{v_{dco}}{v_B} = \frac{1}{k_1} \tag{B.28}$$

where x stands for a, b, or c, equations (B.12) through (B.16) can be rewritten as state-space matrix equations:

$$\Delta\dot{\mathbf{x}} = \mathbf{A} \cdot \Delta\mathbf{x} + \mathbf{B} \cdot \Delta\mathbf{u} \tag{B.29}$$

where the state and input vectors are, respectively,

$$\Delta\mathbf{x} = \left[\Delta i_{sed}' \ \Delta i_{seq}' \ \Delta i_{shd}' \ \Delta i_{shq}' \ \Delta v_{dc}'\right]^T \tag{B.30}$$

$$\Delta\mathbf{u} = \left[\Delta\beta \ \Delta\alpha\right]^T \tag{B.31}$$

and the state or plant matrix **A** is given by:

$$\mathbf{A} = \begin{bmatrix} -\frac{\omega_B R'_L}{L'_L} & \omega & 0 & 0 & -\frac{\omega_B k_1 \cos(\beta_o)}{L'_L} \\ -\omega & -\frac{\omega_B R'_L}{L'_L} & 0 & 0 & -\frac{\omega_B k_1 \sin(\beta_o)}{L'_L} \\ 0 & 0 & -\frac{\omega_B R'_{sh}}{L'_{sh}} & \omega & -\frac{\omega_B k_2 \cos(\alpha_o)}{L'_{sh}} \\ 0 & 0 & -\omega & -\frac{\omega_B R'_{sh}}{L'_{sh}} & -\frac{\omega_B k_2 \sin(\alpha_o)}{L'_{sh}} \\ \frac{3\omega_B C v_{sedo}}{2} & \frac{3\omega_B C v_{seqo}}{2} & \frac{3\omega_B C v_{shdo}}{2} & \frac{3\omega_B C v_{shqo}}{2} & a_{55} \end{bmatrix}$$

where

$$a_{55} = \frac{\omega_B C}{v_{dco}}\left(k_1 \cos(\beta_o) i_{sedo} + k_1 \sin(\beta_o) i_{seqo} + k_2 \cos(\alpha_o) i_{shdo} + k_2 \sin(\alpha_o) i_{shqo}\right)$$

The input or control matrix **B** is given by the following equation:

$$\mathbf{B} = \begin{bmatrix} \frac{\omega_B k_1 v_{dco} \sin(\beta_o)}{L'_L} & 0 \\ -\frac{\omega_B k_1 v_{dco} \cos(\beta_o)}{L'_L} & 0 \\ 0 & \frac{\omega_B k_2 v_{dco} \sin(\alpha_o)}{L'_{sh}} \\ 0 & -\frac{\omega_B k_2 v_{dco} \cos(\alpha_o)}{L'_{sh}} \\ b_{15} & b_{25} \end{bmatrix} \qquad \text{(B.34)}$$

where

$$b_{15} = \omega_B C k_1\left(-\sin(\beta_o) i_{sedo} + \cos(\beta_o) i_{seqo}\right) \qquad \text{(B.35)}$$

$$b_{25} = \omega_B C k_2\left(-\sin(\alpha_o) i_{shdo} + \cos(\alpha_o) i_{shqo}\right) \qquad \text{(B.36)}$$

By taking the Laplace transform of equation (B.29), the state equation in the frequency domain becomes:

$$s\mathbf{\Delta x}(s) - \mathbf{\Delta x}(0) = \mathbf{A} \cdot \mathbf{\Delta x}(s) - \mathbf{B} \cdot \mathbf{\Delta u}(s) \tag{B.37}$$

where the state matrix **A** depends on the operating points as shown in equation (B.32). A solution of the state equation can be obtained by solving for $\mathbf{\Delta x}(s)$ as follows:

$$(s\mathbf{I} - \mathbf{A})\mathbf{\Delta x}(s) = \mathbf{\Delta x}(0) - \mathbf{B} \cdot \mathbf{\Delta u}(s) \tag{B.38}$$

Hence,

$$\begin{aligned} \mathbf{\Delta x}(s) &= (s\mathbf{I} - \mathbf{A})^{-1}\left[\mathbf{\Delta x}(0) - \mathbf{B} \cdot \mathbf{\Delta u}(s)\right] \\ &= \frac{\text{adj}(s\mathbf{I} - \mathbf{A})}{\det(s\mathbf{I} - \mathbf{A})}\left[\mathbf{\Delta x}(0) - \mathbf{B} \cdot \mathbf{\Delta u}(s)\right] \end{aligned} \tag{B.39}$$

The Laplace transform of $\mathbf{\Delta x}$ has two components, one dependent on the initial conditions and the other on the inputs, which correspond to the Laplace transforms of the free and zero state components of the state and outputs vectors [27]. The poles of $\mathbf{\Delta x}(s)$ are the roots of the equation

$$\det(s\mathbf{I} - \mathbf{A}) = 0 \tag{B.40}$$

which is the characteristic equation of matrix **A**, with the values of s that satisfies this equation being the eigenvalues of matrix **A**.

Appendix C

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Glossary

FACTS	Flexible AC Transmission System
STATCOM	Shunt Synchronous Static Compensator
SSSC	Series Synchronous Static Compensator
UPFC	Unified Power Flow Controller
EMTP	Electromagnetic Transient Program
TACS	Transient Analysis of Control Systems
EPRI	Electric Power Research Institute
GTO	Gate-Turn Off Thyristor
SVC	Static Var Compensator
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
VSC	Voltage Source Converter
CSC	Current Source Converter
TNA	Transient Network Analyzer
TVA	Tennessee Valley Authority
AEP	American Electric Power