

Conference and Workshop Publications with Manuscript

- [C74] M. Saad, M. Chaudhary, F. Karray and V. Gaudet, "Machine Learning Based Approaches for Imputation in Time Series Data and their Impact on Forecasting," *IEEE Int. Conf. on Systems, Man and Cybernetics*, Oct. 2020.
- [C73] M. Saad, L. Nassar, F. Karray and V. Gaudet, "Tackling Imputation Across Time Series Models Using Deep Learning and Ensemble Learning," *IEEE Int. Conf. on Systems, Man and Cybernetics*, Oct. 2020.
- [C72] T. Costa, V. Gaudet, E.R. Vrscay and Z. Wang, "Perceptual Colour Difference Uniformity in High Dynamic Range and Wide Colour Gamut," *IEEE Int. Conf. on Image Processing*, online, Oct. 2020.
- [C71] T. Costa, V. Gaudet, E.R. Vrscay, and Z. Wang, "Variation of Perceived Colour Difference Under Different Surround Luminance," *Int Conf. on Image Analysis and Recognition*, 5 pages, June 2020. (published in LNCS, see [B11])
- [C70] K. Zukotynski, V.C. Gaudet, P. Kuo, S. Adamo, M. Goubran, C. Scott, C. Bocti, M. Borrie, H. Chertkow, R. Frayne, R. Hsiung, R. Laforce Jr., M.D. Noseworthy, F.S. Prato, J.D. Sahlas, E.E. Smith, V. Sossi, A. Thiel, J.-P. Soucy, J.-C. Tardif, S.E. Black, "Non-Binary Approaches for Classification of Amyloid Brain PET," *IEEE Int. Symp. on Multiple-Valued Logic*, Fredericton, NB, pp. 206-211, May 2019.
- [C69] M. Faraj, B. Fidan, and V. Gaudet, "Multi-Module Range Anxiety for Battery-Powered Vehicles," *IEEE Intelligent Vehicles Symposium*, Changshu, China, pp. 904-909, June 2018.
- [C68] M. Yang, M. Faraj, A. Hussein and V. Gaudet, "Efficient Hardware Realization of Convolutional Neural Networks using Intra-Kernel Regular Pruning," *IEEE Int. Symp. on Multiple-Valued Logic*, Linz, Austria, pp. 180-185, May 2018.
- [C67] A. Hussein, M. Elmasry and V. Gaudet, "On the Fault Tolerance of Stochastic Decoders," *IEEE Int. Symp. on Multiple-Valued Logic*, Novi Sad, Serbia, pp. 219-223, May 2017.
- [C66] A. Hussein, V. Gaudet, H. Mostafa, and M. Elmasry, "A 16-bit High-Speed Low-Power Hybrid Adder," *Int. Conf. on Microelectronics*, pp. 313-316, Dec. 2016.
- [C65] D.L. Sloan, B. Martin, G. Hall, A. Hakman, P. Marshall, S. Martel, C. Backhouse, V. Gaudet, and D. Elliott, "HV-CMOS Single-Chip Electronics Platform for Lab-on-Chip DNA Analysis," *IEEE Int. Symp. on Circuits and Systems*, pp. 2427-2430, 2016.
- [C64] K.-L. Huang, V. Gaudet, and M. Salehi, "Trapping Sets in Stochastic LDPC Decoders," *IEEE ASILOMAR Conf. on Signals, Systems, and Computers*, Pacific Grove, CA, pp. 1601-1605, Nov. 2015.

- [C63] P. Chuang, M. Sachdev, and V. Gaudet, "VLSI Implementation of High-Throughput, Low-Energy, Configurable MIMO Detector," *IEEE Int. Conf. on Computer Design*, New York, NY, pp. 335-342, Oct. 2015.
- [C62] K.-L. Huang, V. Gaudet, and M. Salehi, "A Hybrid ARQ Scheme Using LDPC Codes with Stochastic Decoding," *Ann. Conf. on Information Sciences and Systems*, Baltimore, MD, 5 pages, 2015.
- [C61] K.-L. Huang, V. Gaudet, and M. Salehi, "Output Decisions for Stochastic LDPC Decoders," *Annual Conference on Information Sciences and Systems*, Princeton, NJ, 5 pages, 2014.
- [C60] C. Ceroici and V. Gaudet, "FPGA Implementation of a Clockless Stochastic LDPC Decoder," *IEEE Workshop on Signal Processing Systems*, Belfast, UK, 5 pages, Oct. 2014.
- [C59] R. Dodd, B. Cockburn, and V. Gaudet, "Neural Spike Compression Using Feature Extraction and a Fuzzy C-Means Codebook," *IEEE Int. Symp. on Multiple-Valued Logic*, Bremen, Germany, pp. 44-48, May 2014.
- [C58] R. Dodd, B. Cockburn, and V. Gaudet, "Adaptive Dual-Threshold Neural Signal Compression Suitable for Implantable Recording," *IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Florence, Italy, pp. 8346-8350, May 2014.
- [C57] N. Bahrani and V. Gaudet, "Measurements and Channel Characterization for In-Vehicle Power Line Communications," *IEEE Int. Symp. on Power Line Communication and Its Applications*, Glasgow, UK, pp. 64-69, April 2014.
- [C56] K.-L. Huang, V. Gaudet, and M. Salehi, "A Scaling Method for Stochastic LDPC Decoding Over the Binary Symmetric Channel," *Ann. Conf. on Information Sciences and Systems*, Baltimore, MD, 5 pages, 2013.
- [C55] N. Onizawa, S. Matsunaga, V. Gaudet, W. Gross, and T. Hanyu, "Probabilistic Search Schemes for High-Speed Low-Power Content-Addressable Memories," *Int. Conf. on Analog VLSI Circuits*, Montreal, QC, 6 pages, October 2013.
- [C54] N. Onizawa, W. Gross, T. Hanyu, and V. Gaudet, "Lowering Error Floors in Stochastic Decoding of LDPC Codes Based on Wire-Delay Dependent Asynchronous Updating," *IEEE Int. Symp. on Multiple-Valued Logic*, Toyama, Japan, pp. 254-259, May 2013.
- [C53] K. Jensen, P. Levine, and V. Gaudet, "Noise Analysis of CMOS Photodiode Integrator for Fluorescent Detection Applications," *Int. Conf. on Noise and Fluctuations*, 4 pages, Montpellier, France, June 2013.
- [C52] S.-Y. Li, T. Brandon, D. Elliott, and V. Gaudet, "Power Characterization of a Gbit/s FPGA Convolutional LDPC Decoder," *IEEE Workshop on Signal Processing Systems*, pp. 294-299, Québec, QC, Oct. 2012.

- [C51] N. Onizawa, W. Gross, T. Hanyu, and V. Gaudet, "Clockless Stochastic Decoding of Low-Density Parity-Check Codes," *IEEE Workshop on Signal Processing Systems*, pp. 143-148, Québec, QC, Oct. 2012.
- [C50] P. Marshall, V. Gaudet, and D. Elliott, "Effects of Varying Message Precision in Digit-Online LDPC Decoders," *IEEE Workshop on Signal Processing Systems*, pp. 7-12, Québec, QC, Oct. 2012.
- [C49] P. Chuang, D. Li, M. Sachdev, and V. Gaudet "A 148ps 135mW 64-bit Adder with Constant-Delay Logic in 65nm CMOS," *IEEE Custom Integr. Circuits Conf.*, 4 pages, San Jose, CA, Sept. 2012.
- [C48] R. Dodd, B. Crowley, V. Gaudet, V. Mushahwar, and B. Cockburn, "Microelectronics for In Vivo Neural Recording," *Int. Functional Electrical Stimulation Society Conf.*, 4 pages, Sept. 2012.
- [C47] N. Onizawa, V. Gaudet, T. Hanyu, and W. Gross, "Asynchronous Stochastic Decoding of LDPC Codes," *IEEE Int. Symp. on Multiple-Valued Logic*, Victoria, BC, pp. 92-97, May 2012.
- [C46] N. Onizawa, S. Matsunaga, V. Gaudet, and T. Hanyu, "High-Throughput Low-Energy Content-Addressable Memory Based on Self-Timed Overlapped Search Mechanism," *IEEE Int. Symp. on Asynchronous Circuits and Systems*, Copenhagen, Denmark, pp. 41-48, May 2012.
- [C45] K.-L. Huang, V. Gaudet, and M. Salehi, "A Markov Chain Model for Edge Memories in Stochastic Decoding of LDPC Codes," *45th Ann. Conf. on Information Sciences and Systems*, 4 pages, Baltimore, MD, 2011.
- [C44] C. Schlegel and V. Gaudet, "Hardware Implementation Challenges of Modern Error Control Decoders," *IEEE Int. Symp. on Circuits and Systems*, pp. 1788-1791, May 2011.
- [C43] R. Dodd, C. Schlegel, and V. Gaudet, "Implementation of Enhanced CDMA Utilizing Low Complexity Joint Detection with Iterative Processing," *IEEE Int. Symp. on Circuits and Systems*, pp. 1763-1766, June 2010.
- [C42] V. Gaudet and W. Gross, "Switching Activity in Stochastic Decoders," *IEEE Int. Symp. on Multiple-Valued Logic*, pp. 167-172, May 2010.
- [C41] E. Son, B. Crowley, C. Schlegel, and V. Gaudet, "Packet Detection for Wireless Networking with Multiple Packet Reception," *IEEE Military Communications Conf.*, 5 pages, Oct. 2009.
- [C40] A. Razib, S. Dick, and V. Gaudet, "Design of a High-Speed Fuzzy Logic Controller Based on Log-Domain Arithmetic," *IEEE Int. Symp. on Multiple-Valued Logic*, pp. 139-144, May 2009.
- [C39] T. Brandon, J. Koob, L. van den Berg, Z. Chen, A. Alimohammad, R. Swamy, J. Klaus, S. Bates, V. Gaudet, B. Cockburn, and D. Elliott, "A 600-Mb/s Encoder and Decoder for Low-Density Parity-Check Convolutional Codes," *IEEE Int. Symp. on Circuits and Systems*, pp. 3090-

3093, May 2008. Best Student Paper Award

[C38] R. Długosz and V. Gaudet, "Current-Mode Memory Cell with Power Down Phase for Discrete Time Analog Iterative Decoders," *IEEE Int. Symp. on Circuits and Systems*, pp. 748-751, May 2008.

[C37] M. Khorasani, L. van den Berg, P. Marshall, M. Zargham, V. Gaudet, D. Elliott, and S. Martel, "Low-Power Static and Dynamic High-Voltage CMOS Level-Shifter Circuits," *IEEE Int. Symp. on Circuits and Systems*, pp. 1946-1949, May 2008.

[C36] Y. Wang, B. Afshar, T. Cheng, V. Gaudet, and A. Niknejad, "A 2.5mW Inductorless Wideband VGA with Dual Feedback DC Offset Correction in 90nm CMOS Technology," *IEEE Radio-Frequency Integrated Circuits Symp. (RFIC)*, pp. 91-94, June 2008. Student Paper Contest Finalist

[C35] S. Dick, V. Gaudet, and H. Bai, "Bit-Serial Arithmetic: A Novel Approach to Fuzzy Hardware," *Ann. Meeting of the North American Fuzzy Inf. Processing Society (NAFIPS)*, 6 pages, May 2008.

[C34] Y. Wang, S. Kilambi, V. Gaudet, and K. Iniewski, "A Low-Power CMOS Transmitter Design for IR-UWB Communication Systems," *IEEE Int. Conf. on Ultra-Wideband*, pp. 823-827, Sept. 2007.

[C33] Y. Wang, S. Kilambi, K. Iniewski, and V. Gaudet, "A Fully-Integrated CMOS Transmitter for IR-UWB Communication Systems," *IEEE Midwest Symp. Circuits and Systems*, pp. 738-741, Aug. 2007.

[C32] K. Boyle, C. Winstead, P. Mercier, M. Kashyap, N. Sadeghi, and V. Gaudet, "Design and Implementation of an All-Analog Fast-Fourier Transform Processor," *IEEE Midwest Symp. on Circuits and Systems*, pp. 1532-1535, Aug. 2007.

[C31] N. Onizawa, T. Ikeda, T. Hanyu, and V. Gaudet, "A 3.2-Gb/s 1024-b Rate-1/2 LDPC Decoder Chip Using a Flooding-Type Update-Schedule Algorithm," *IEEE Midwest Symp. on Circuits and Systems*, pp. 217-220, Aug. 2007.

[C30] V. Gaudet, C. Schlegel, and R. Dodd, "LDPC Decoder Message Formatting Based on Activity Factor Minimization Using Differential Density Evolution," *IEEE Information Theory Workshop*, invited paper, pp. 571-576, June 2007.

[C29] Y. Wang, A. Ho, K. Iniewski, and V. Gaudet, "Inductive ESD Protection for Narrow Band and Ultra-Wideband CMOS Low Noise Amplifiers," *IEEE Int. Symp. on Circuits and Systems*, pp. 3920-3923, May 2007.

[C28] M. Zargham and V. Gaudet, "Noise Analysis for Ultrawideband Low Noise Amplifiers," *IEEE Canadian Conf. on Electrical and Computer Engineering*, pp. 1102-1105, May 2007.

- [C27] R. Długosz, V. Gaudet, and K. Iniewski, "Flexible Ultra Low Power Successive Approximation Analog-to-Digital Converter with Asynchronous Clock Generator," *IEEE Canadian Conf. on Electrical and Computer Engineering*, pp. 1649-1652, May 2007.
- [C26] K. Boyle, S. Kilambi, R. Długosz, K. Iniewski, and V. Gaudet, "An Examination of the Effect of Feature Size Scaling on Effective Power Consumption in Analog to Digital Converters," *IEEE Workshop on Signal Processing Systems*, pp. 194-199, Oct. 2006.
- [C25] N. Sadeghi, S. Howard, S. Kasnavi, K. Iniewski, V. Gaudet, and C. Schlegel, "Analysis of Error Control Code Use in Ultra-Low-Power Wireless Sensor Networks," *IEEE Int. Symp. on Circuits and Systems*, pp. 3558-3561, May 2006.
- [C24] W. Gross, A. Milner, and V. Gaudet, "Stochastic Implementation of LDPC Decoders," *IEEE ASILOMAR Conf. on Signals, Systems, and Computers*, invited paper, pp. 713-717, Nov. 2005.
- [C23] S. Howard, C. Schlegel, and V. Gaudet, "A Degree-Matched Check Node Approximation For LDPC Decoding," *IEEE Int. Symp. on Information Theory*, pp. 1131-1135, Sept. 2005.
- [C22] C. Winstead, A. Rapley, V. Gaudet, and C. Schlegel, "Stochastic Iterative Decoders," *IEEE Int. Symp. on Information Theory*, pp. 1116-1120, Sept. 2005.
- [C21] J. Ko, V. Gaudet, and R. Hang, "A Tier 3 Software Defined AM Radio," *IEEE Int. Workshop on Systems on Chip for Real-Time Applications*, pp. 257-261, July 2005.
- [C20] J. Ko, V. Gaudet, and R. Hang, "Implementation of Ideal Tier 3 Software Defined AM/Short Wave Radio Receivers," *Int. Conf. on Wireless Communications*, Calgary, AB, pp. 361-370, July 2005.
- [C19] S. Kasnavi, P. Berube, V. Gaudet, and N. Amaral, "A Hardware-Based Longest Prefix Matching Scheme for TCAMs," *IEEE Int. Symp. on Circuits and Systems*, pp. 3339-3342, May 2005.
- [C18] D. Haley, C. Winstead, A. Grant, V. Gaudet, and C. Schlegel, "An Analog/Digital Mode Switching LDPC Codec," *IEEE Int. Symp. on Circuits and Systems*, pp. 5790-5793, May 2005.
- [C17] M. Yiu, V. Gaudet, C. Schlegel, and C. Winstead, "Digital Built-In Self-Test of CMOS Analog Iterative Decoders," *IEEE Int. Symp. on Circuits and Systems*, pp. 2204-2207, May 2005.
- [C16] N. Onizawa, A. Mochizuki, T. Hanyu and V. Gaudet, "Multiple-Valued Duplex Asynchronous Data Transfer Scheme for Interleaving in LDPC Decoders," *IEEE Int. Symp. on Multiple-Valued Logic*, pp. 138-143, May 2005.
- [C15] D. Li, V. Gaudet, and A. Basu, "Test Results of Various CMOS Image Sensor Pixels," *IEEE Canadian Conf. on Electrical and Computer Engineering*, pp. 1963-1966, May 2005.
- [C14] A. Rapley, C. Winstead, V. Gaudet, and C. Schlegel, "On the Simulation of Stochastic

Iterative Decoders," *IEEE Canadian Conf. on Electrical and Computer Engineering*, pp. 1851-1854, May 2005.

[C13] A. Dabrowski, R. Długosz, P. Pawtowski, K. Iniewski, and V. Gaudet, "Analog Baseband Filtering Realized Using Switched Capacitor Finite Impulse Response Filter," *IEEE Int. Symp. on VLSI Design, Automation, and Test*, pp. 108-111, April 2005.

[C12] E. Fung, K. Leung, N. Parimi, M. Purnaprajna, and V. Gaudet, "ASIC Implementation of a High Speed WGNG for Communication Channel Emulation," *IEEE Workshop on Signal Processing Systems*, pp. 304-309, Oct. 2004.

[C11] S. Howard, S.S. Zeinoddin, C. Schlegel, and V. Gaudet, "Short-Cycle-Free Interleaver Design for Increasing Minimum Squared Euclidean Distance," *IEEE Int. Symp. on Inf. Theory*, p. 53, June 2004.

[C10] N. Nguyen, C. Winstead, V. Gaudet, and C. Schlegel, "A 0.8V CMOS Analog Decoder for an (8,4,4) Extended Hamming Code," *IEEE Int. Symp. on Circuits and Systems*, pp. 1116-1119, May 2004.

[C9] D. Gnaedig, E. Boutillon, M. Jézéquel, V. Gaudet, and G. Gulak, "On Multiple Slice Turbo Codes," *Int. Symp. on Turbo Codes & Related Topics*, pp. 343-346, Sept. 2003.

[C8] C. Berrou, Y. Saouter, and V. Gaudet, "Degenerated Turbo Codes for High Rate and Throughput Concatenated Schemes," *Int. Symp. on Turbo Codes & Related Topics*, pp. 339-342, Sept. 2003.

[C7] A. Rapley, C. Winstead, V. Gaudet, and C. Schlegel, "Stochastic Iterative Decoding on Factor Graphs," *Int. Symp. on Turbo Codes & Related Topics*, pp. 507-510, Sept. 2003.

[C6] C. Winstead, N. Nguyen, V. Gaudet, and C. Schlegel, "Low-Voltage CMOS Translinear Circuits for Analog Decoders," *Int. Symp. on Turbo Codes & Related Topics*, pp. 271-274, Sept. 2003.

[C5] D. Gnaedig, E. Boutillon, M. Jézéquel, G. Gulak, and V. Gaudet, "Turbo codes à roulettes," *19e Colloque GRETSI sur le traitement du signal et des images*, Paris, Sept. 2003.

[C4] C. Winstead, V. Gaudet, and C. Schlegel, "Analog Iterative Decoding of Error Control Codes," *IEEE Canadian Conf. on Electrical and Computer Engineering*, pp. 1539-1542, May 2003.

[C3] V. Gaudet and G. Gulak, "A 13.3Mbps 0.35 μ m CMOS Analog Turbo Decoder IC with a Configurable Interleaver," *IEEE Int. Solid-State Circuits Conf.*, pp. 148-149, Feb. 2003.

[C2] W. Gross, V. Gaudet and G. Gulak, "A VLSI Architecture for Soft-Output PR4 Detection," *IEEE Midwest Symp. on Circuits and Systems*, Vol. 1, pp. 416-419, Aug. 2000.

[C1] V. Gaudet, and G. Gulak, "CMOS Implementation of a Current Conveyor-Based Field-Programmable Analog Array," *IEEE ASILOMAR Conf. on Signals, Systems, and Computers*, Vol. 2, pp. 1156-1159, Nov. 1997.